

# ECEN620: Network Theory Broadband Circuit Design Fall 2012

---

## Lecture 11: Charge Pump Circuits



Sam Palermo

Analog & Mixed-Signal Center

Texas A&M University

# Announcements & Agenda

---

- Exam 1 is on Wed. Oct 3
  - One double-sided 8.5x11 notes page allowed
  - Bring your calculator
  - 2 reference exams posted on the website, but no solutions available ☹
- Charge pump circuits
  - Basic operation
  - Techniques to improve static and dynamic current source matching

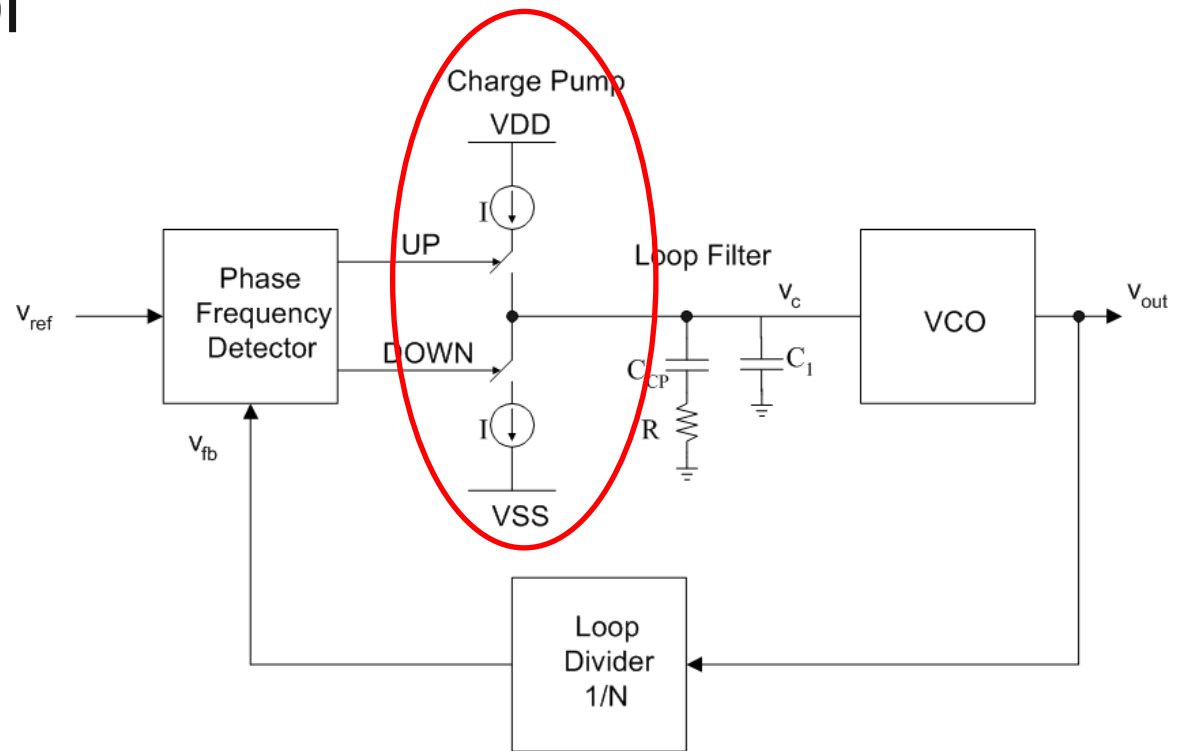
# References

---

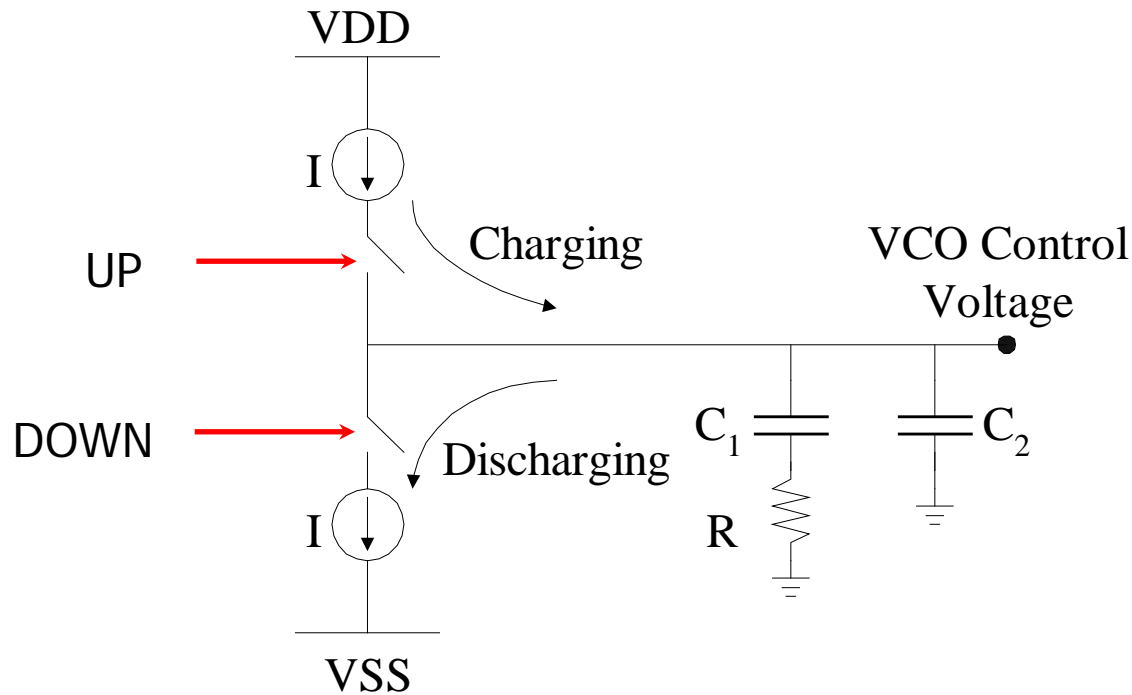
- *Design of Integrated Circuits for Optical Communications*, B. Razavi, McGraw-Hill, 2003.
- *First Time, Every Time – Practical Tips for Phase-Locked Loop Design*, D. Fischette, IEEE Tutorial, 2009.
- Additional PLL/charge-pump papers that I will post on the website

# Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider



# Charge Pump

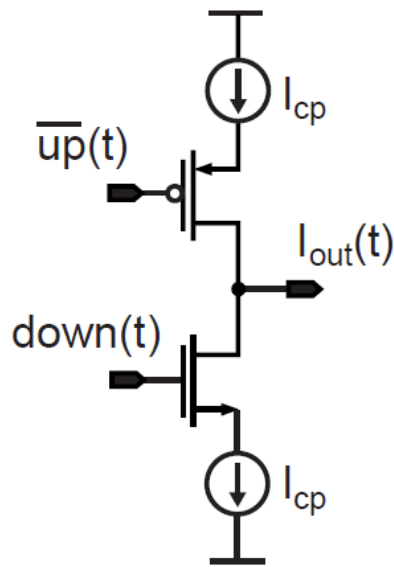


- Converts PFD output signals to charge
- Charge is proportional to PFD pulse widths

$$\text{PFD-CP Gain: } \left( \frac{1}{2\pi} \right) I_{CP}$$

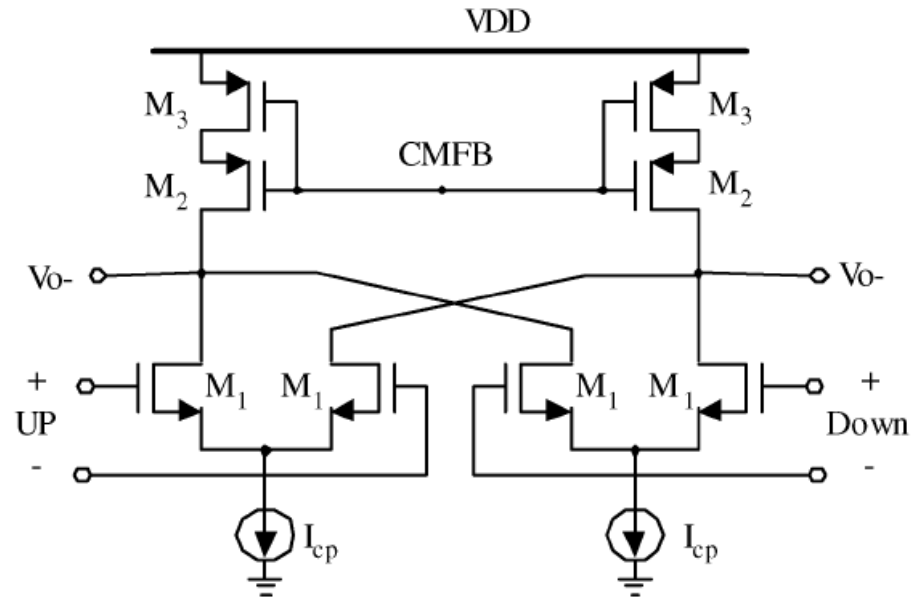
# Charge Pump Implementations

Single-Ended



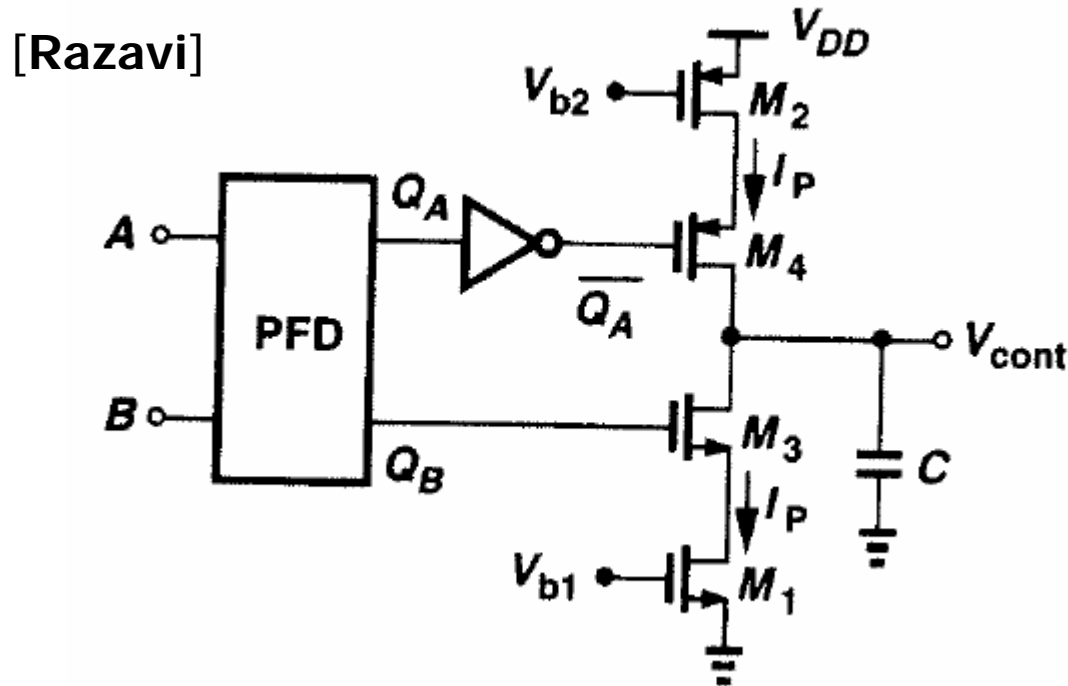
[Perrott]

Fully Differential



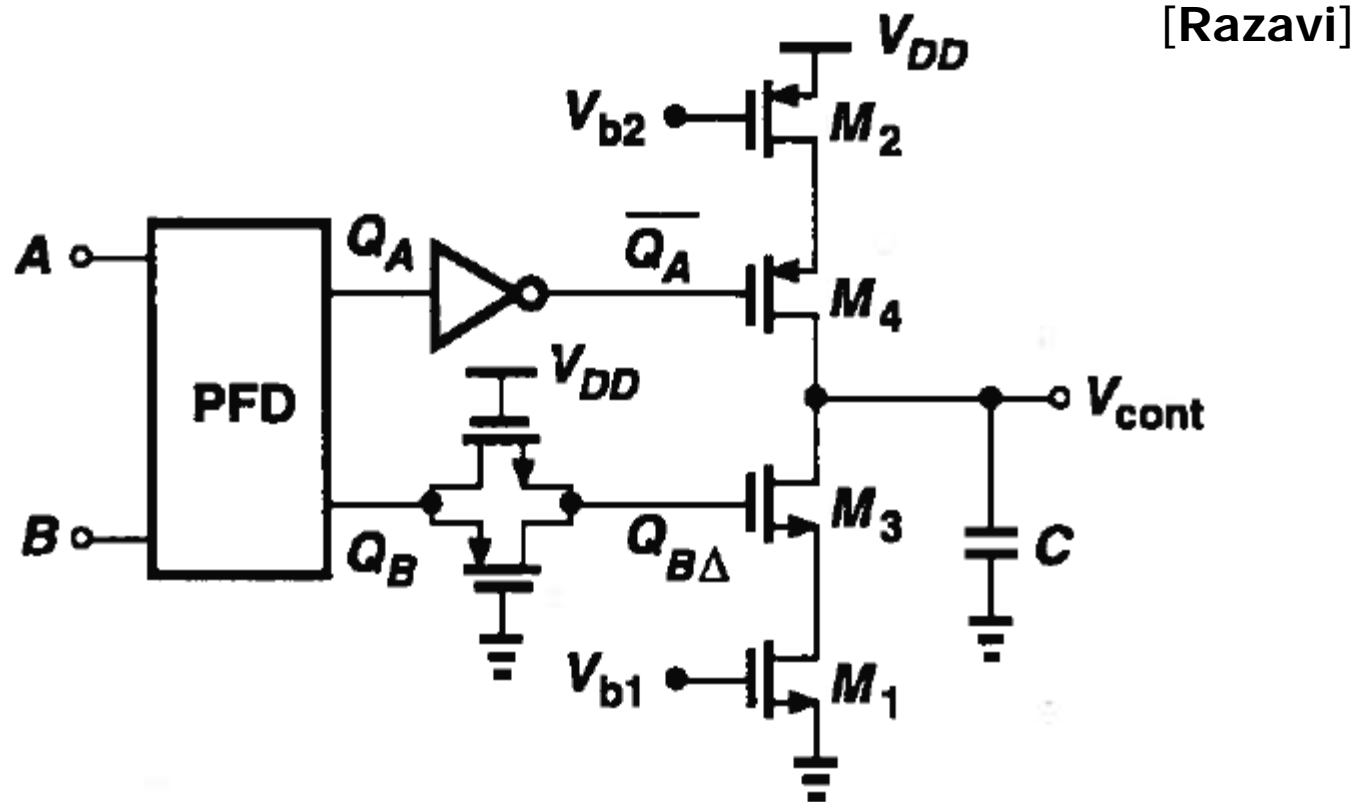
[Li TCAS1 2008]

# Simple Charge Pump



- Issues
  - Skew between UPB and DN control signals
  - Matching of UP/DN current sources
  - Clock feedthrough and charge injection from switches onto  $V_{ctrl}$
  - Charge sharing between current source drain nodes' capacitance and  $V_{ctrl}$

# Simple Charge Pump Skew Compensation



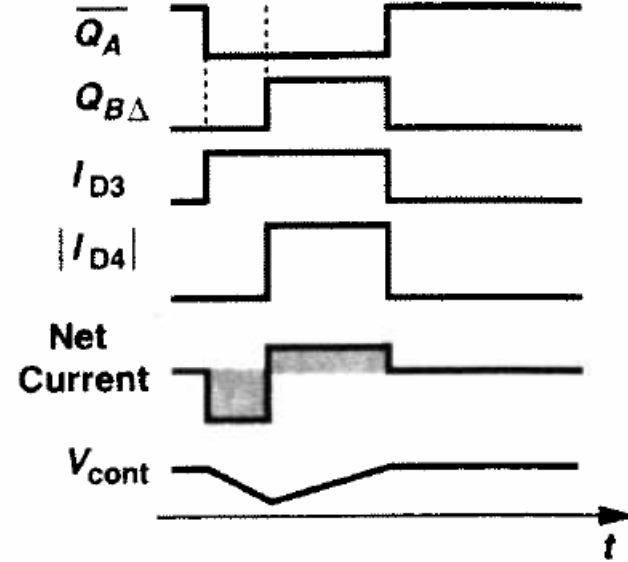
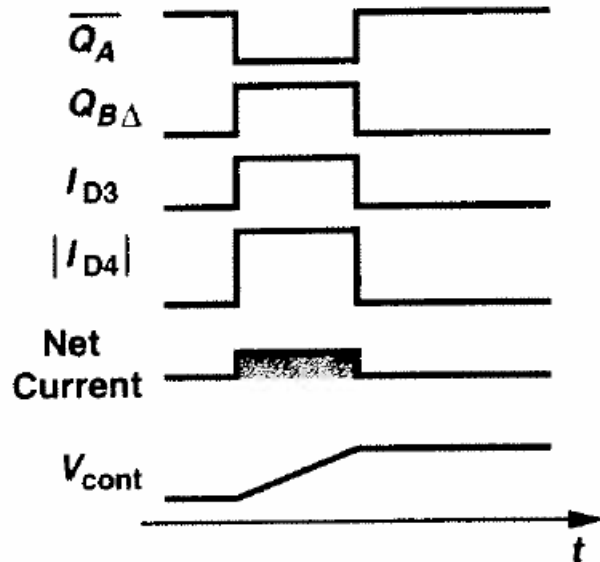
- Adding a transmission gate in the DN signal path helps to equalize the delay with the UPB signal for better overlap between the UP and DN current sources



# Charge Pump Mismatch

Ideal locked condition, but CP mismatch

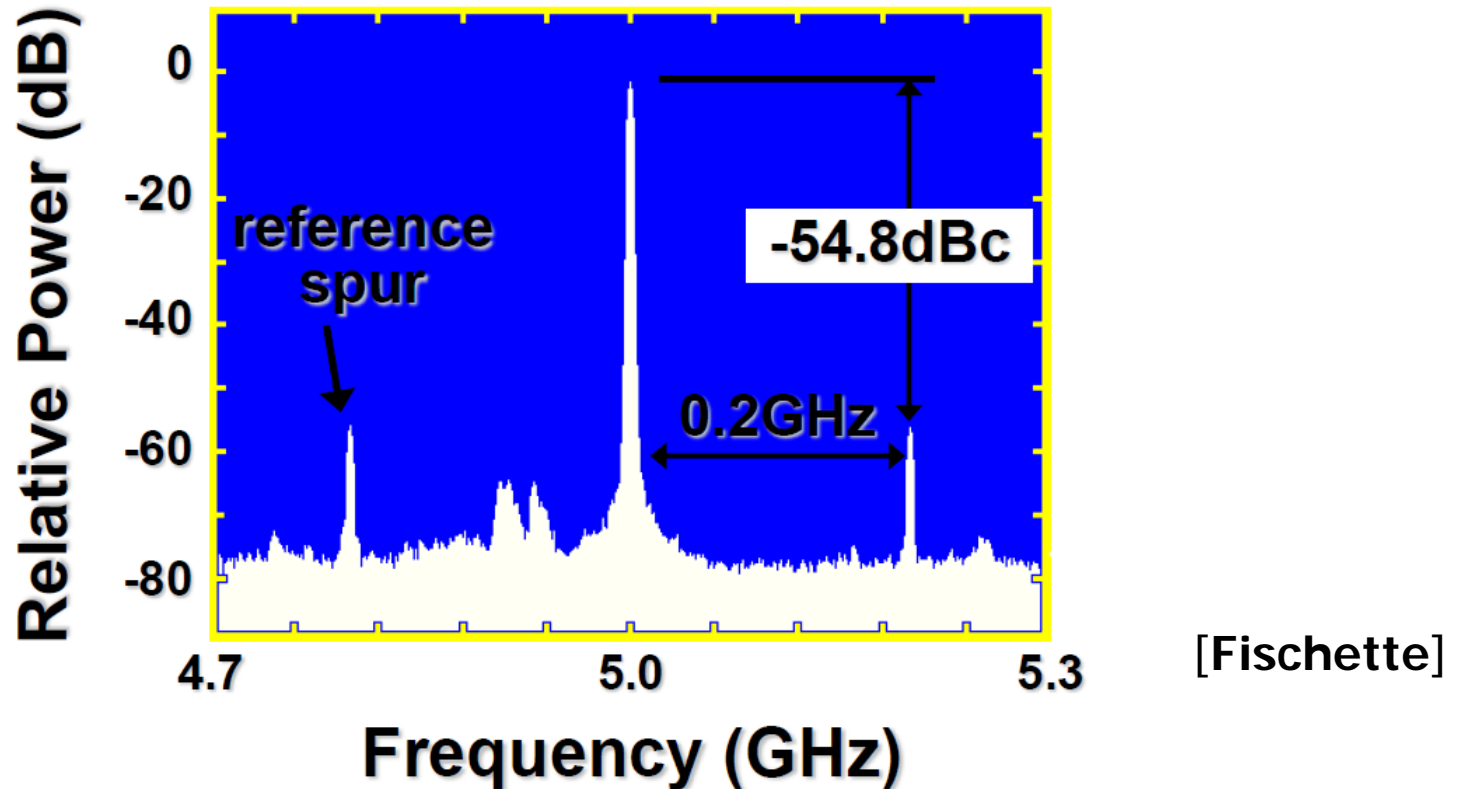
Actual locked condition w/ CP mismatch



[Razavi]

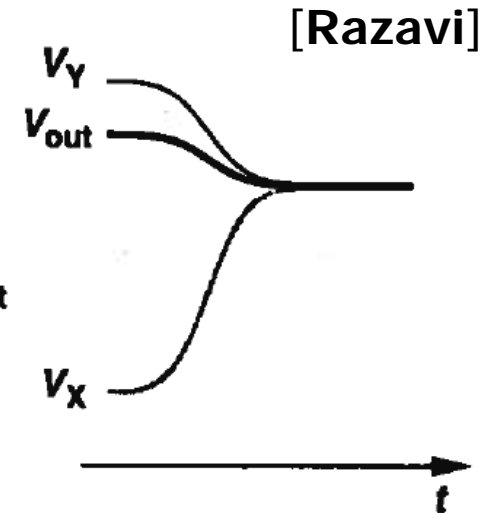
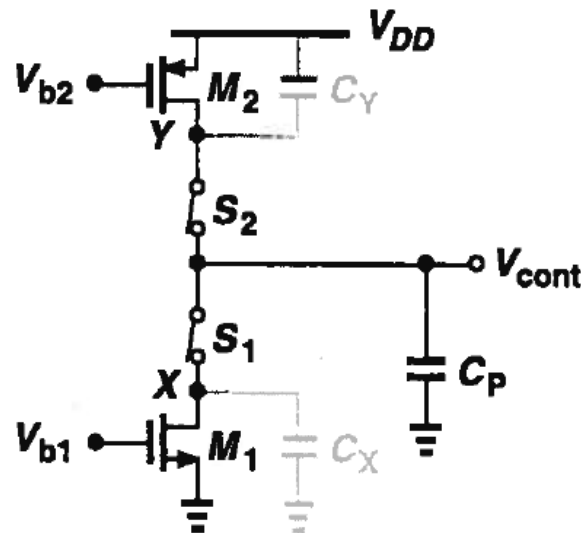
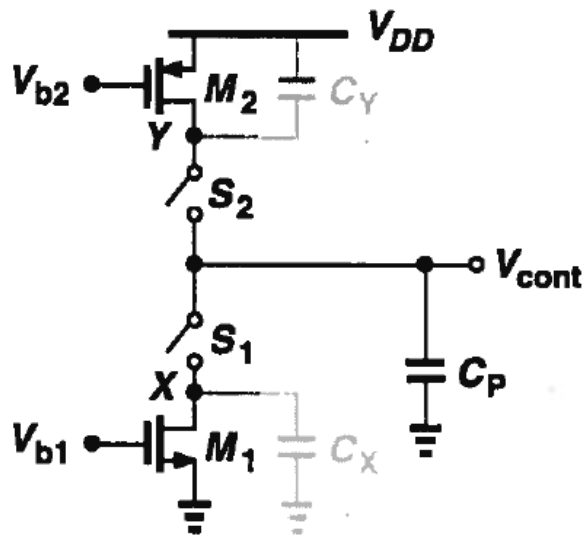
- Recall that in order to eliminate the PLL deadzone, both UP and DN current sources should be on for a minimum period
- PLL will lock with static phase error if there is a charge pump mismatch
- Extra "ripple" on  $V_{ctrl}$ 
  - Results in frequency domain spurs at the reference clock frequency offset from the carrier

# PLL Output Spectrum w/ Spurs



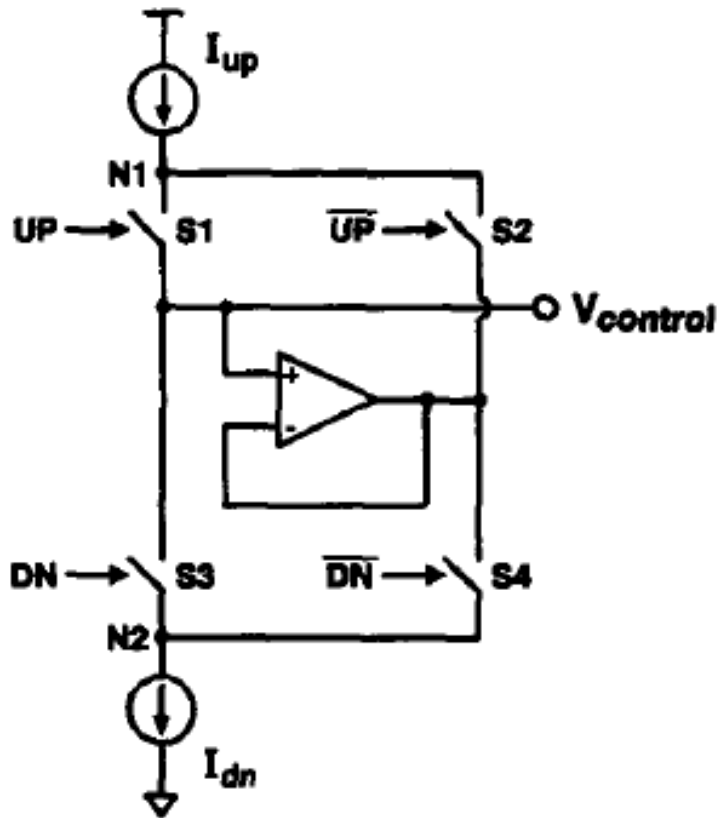
- A 5GHz clock synthesized with a PLL utilizing a 200MHz reference clock
- Spurs appear at  $\pm f_{\text{ref}}$  relative to the carrier frequency

# Charge Sharing on $V_{ctrl}$



- When switches are off, the PMOS current source drain discharges to  $V_{DD}$  and the NMOS current source drain discharges to  $GND$
- When switches are on, charge sharing occurs between the loop filter capacitance and these current source drain nodes, causing a level-dependent disturbance on  $V_{ctrl}$

# Charge Pump w/ Improved Matching

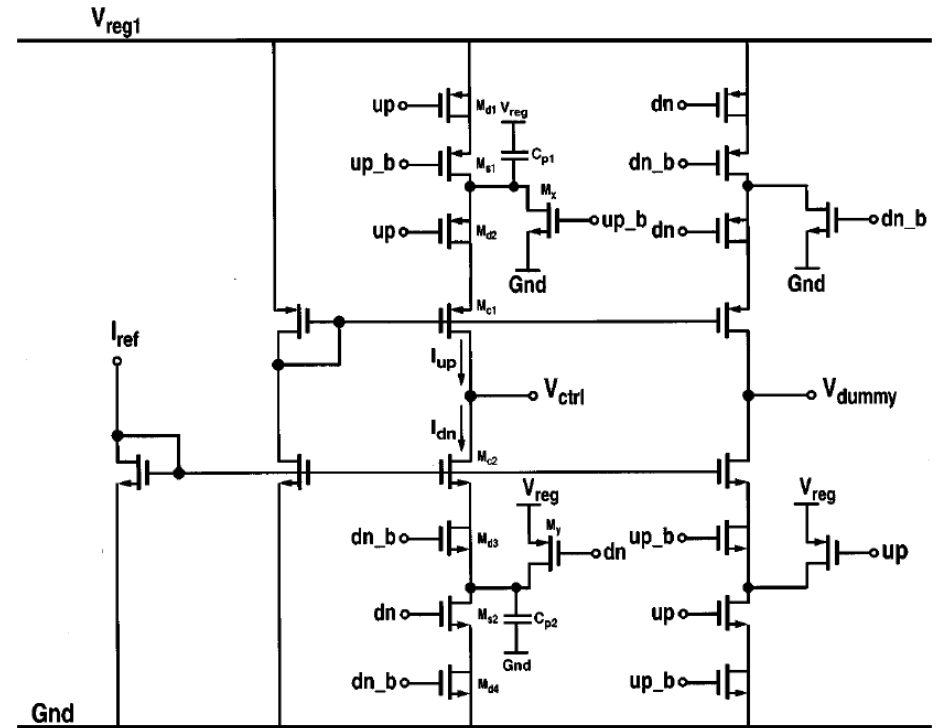


- Parallel path keeps current sources always on
- Amplifier keeps current source  $V_{ds}$  voltages constant resulting in reduced transient current mismatch (charge sharing)

[Young JSSC 1992]

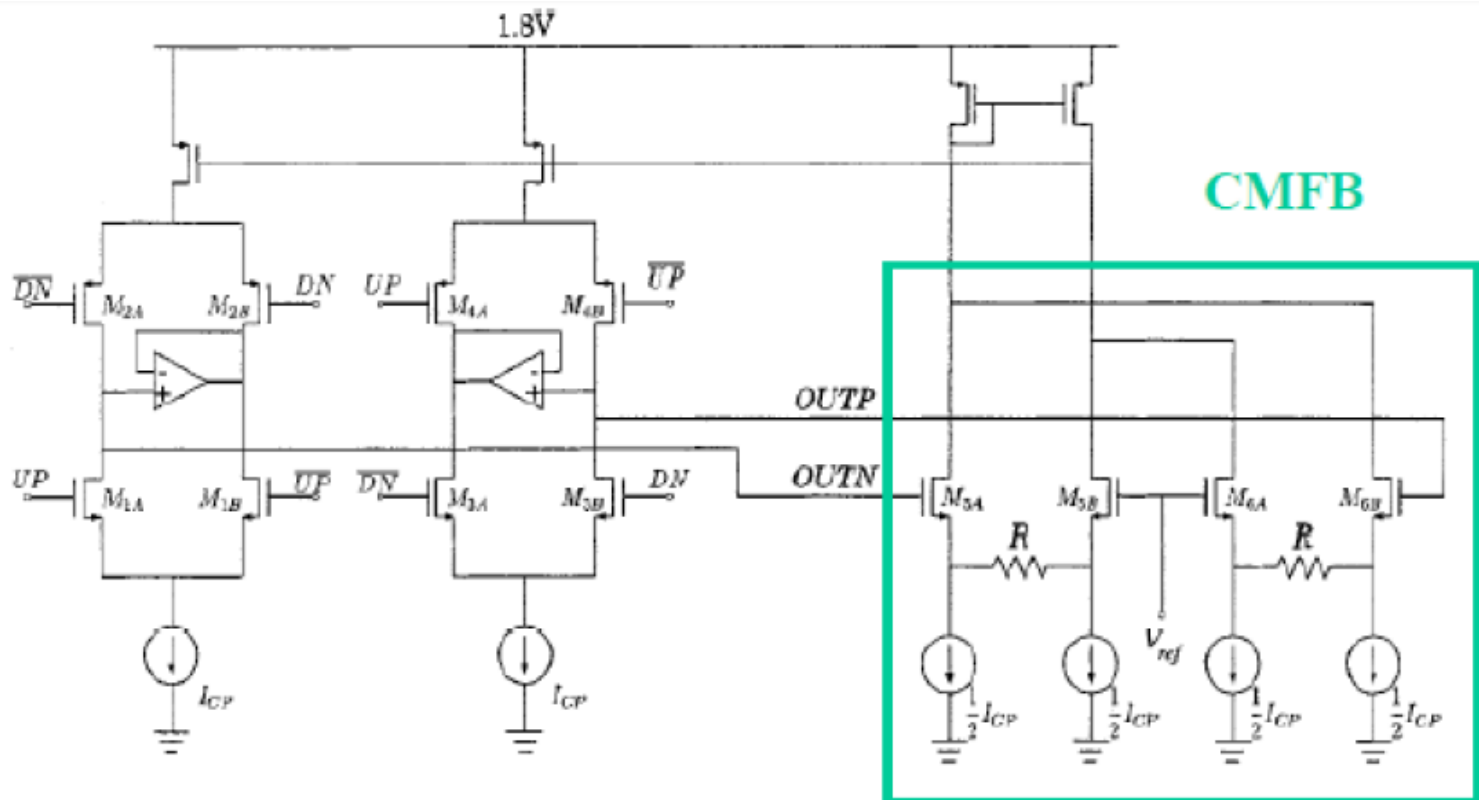
# Charge Pump w/ Reversed Switches

- Swapping switches reduces charge injection
  - MOS caps ( $M_{d1-4}$ ) provide extra charge injection cancellation
- Helper transistors  $M_x$  and  $M_y$  quickly turn-off current sources
- Dummy branch helps to match PFD loading
- Helps with charge injection, but charge sharing is still an issue



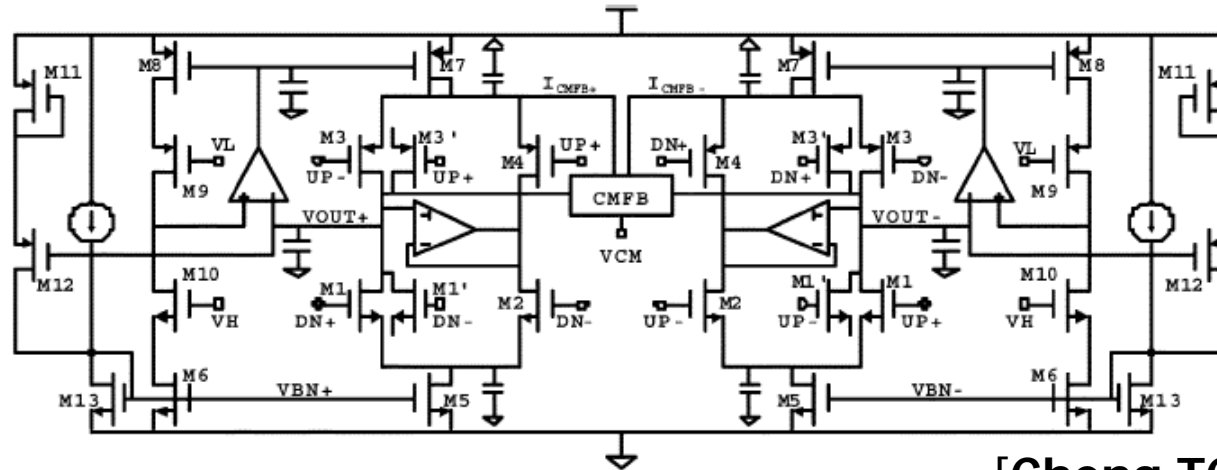
[Ingino JSSC 2001]

# Fully-Differential Charge Pump



- CMFB loop adjusts the top current sources to match  $I_{CP}$  at the differential loop filter common-mode level

# Everything But The Kitchen Sink



[Cheng TCAS2 2006]

- This fully-differential charge pump uses many techniques to match the UP/DN current sources and mitigate charge injection and charge sharing
  - Dummy path with feedback amplifiers to match current source  $V_{DS}$
  - Dummy switches M1' and M3' provide charge injection cancellation
  - CMFB circuit matches UP/DN current at the filter common-mode output
  - Left and right-most feedback loop improve matching considering the differential loop filter control voltage
  - Additional PMOS current sources M11 & M12 extend matching over a wide voltage range

# Improved Matching w/ Differential Output

[Cheng TCAS2 2006]

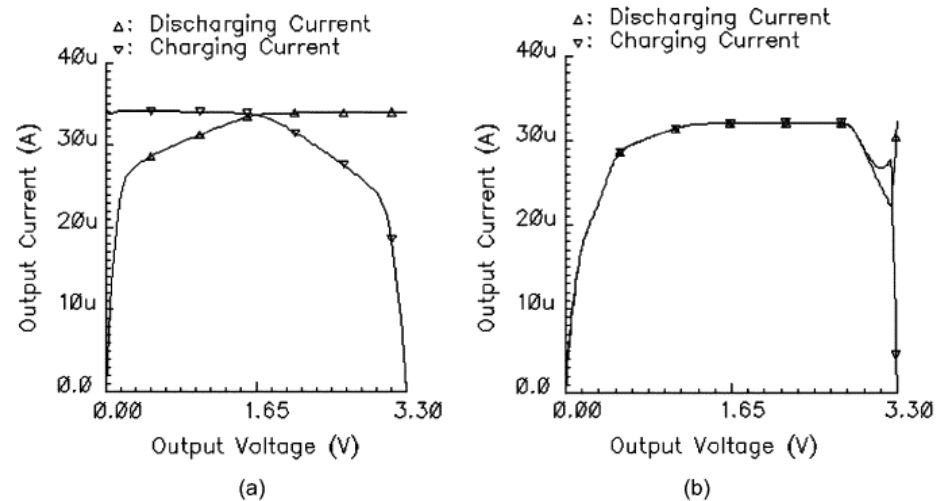
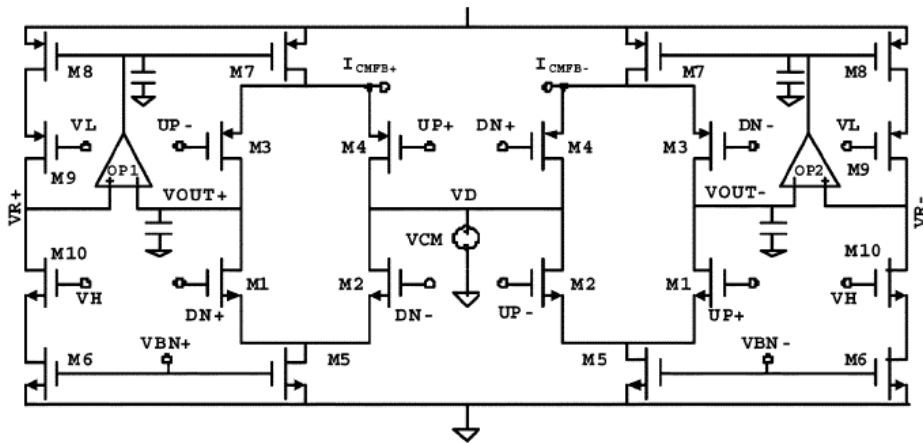


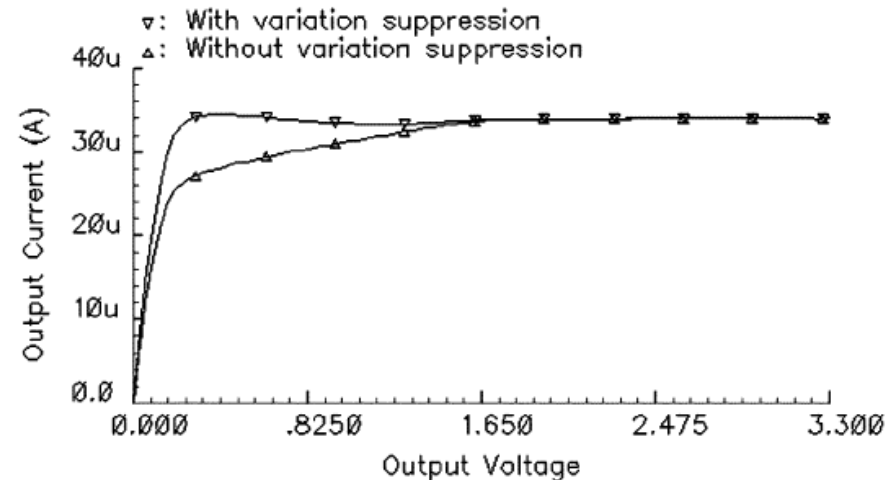
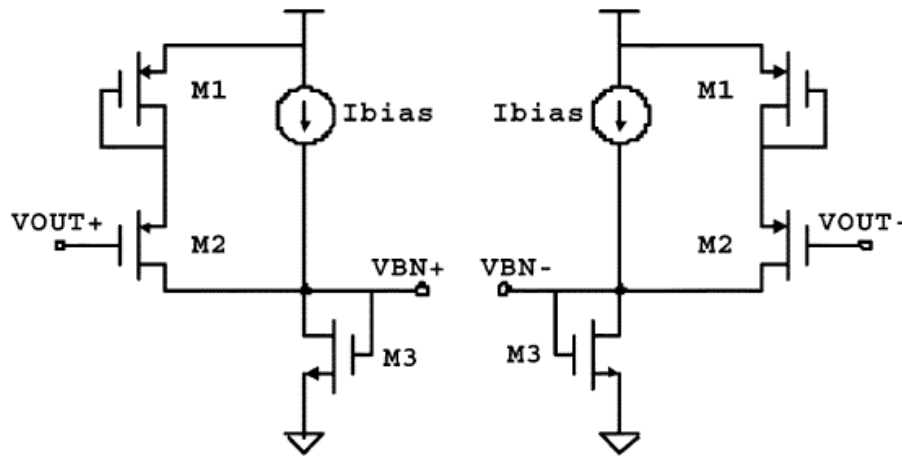
Fig. 4. Output currents with and without mismatch suppression.

- The CMFB loop compensates for current source mismatch at the common-mode level
- However, it cannot compensate for current source mismatch due to the differential control output voltage, as this voltage is symmetric with the common-mode
- Additional feedback networks (OP1 & OP2) provide for improved matching with the differential control output voltage



# Additional Current Variation Suppression

[Cheng TCAS2 2006]



- While matching is good at the control voltage extremes, the absolute current value falls due to finite current source output resistance
- Additional PMOS current sources M1 and M2 provide additional NMOS current when the single-ended control voltage is low, which the main PMOS current source then tracks via feedback
- This extends the voltage range over which the absolute charge pump current matches its nominal value

# Next Time

---

- Loop Filter Circuits