Announcements

• Next Week
  • Shan will give Monday lecture at normal time
  • **No class next Wednesday**
  • I’ll be back for Friday’s lecture

• Lab 4 posted on website

• Reading
  • Paper posted on sampler analysis
Agenda

• RX Circuits
  • RX parameters
  • RX static amplifiers
  • Clocked comparators
    • Circuits
    • Characterization techniques
  • Integrating receivers
  • RX sensitivity
    • Offset correction
  • Demultiplexing receivers
High-Speed Electrical Link System
Receiver Parameters

- RX sensitivity, offsets in voltage and time domain, and aperture time are important parameters.
- Minimum eye width is determined by aperture time plus peak-to-peak timing jitter.
- Minimum eye height is determined by sensitivity plus peak-to-peak voltage offset.

[Diagram showing sensitivity, aperture time, offset voltage, timing offset, skew, and jitter.]

[Dally]
RX Block Diagram

- RX must sample the signal with high timing precision and resolve input data to logic levels with high sensitivity.
- Input pre-amp can improve signal gain and improve input referred noise:
  - Can also be used for equalization, offset correction, and fix sampler common-mode.
  - Must provide gain at high-bandwidth corresponding to full data rate.
- Comparator can be implemented with static amplifiers or clocked regenerative amplifiers:
  - Clocked regenerative amplifiers are more power efficient for high gain.
- Decoder used for advanced modulation (PAM4, Duo-binary).
• CMOS inverter is one of the simplest RX pre-amplifier structures
• Termination voltage, $V_{TT}$, should be placed near inverter trip-point
• Issues:
  • Limited gain (<20)
  • High PVT variation results in large input referred offset
  • Single-ended operation makes it both sensitive to and generate supply noise
RX Static Differential Amplifiers

- Differential input amplifiers often used as input stage in high performance serial links
  - Rejects common-mode noise
  - Sets input common-mode for preceding comparator
- Input stage type (n or p) often set by termination scheme
- High gain-bandwidth product necessary to amplify full data rate signal
- Offset correction and equalization can be merged into the input amplifier

\[
A_v = g_{m1} \left( R_L \parallel r_{o1} \right) \approx g_{m1} R_L
\]

\[
A_v = \frac{g_{m1}}{g_{m3} + g_{o3} + g_{o4} + g_{o1}} \approx \frac{g_{m1}}{g_{m3}}
\]
RX Clocked Comparators

- Also called regenerative amplifier, sense-amplifier, flip-flop, latch
- Samples the continuous input at clock edges and resolves the differential to a binary 0 or 1

[J. Kim]
Important Comparator Characteristics

- Offset and hysteresis
- Sampling aperture, timing resolution, uncertainty window
- Regeneration gain, voltage sensitivity, metastability
- Random decision errors, input-referred noise
Dynamic Comparator Circuits

- To form a flip-flop
  - After strong-arm latch, cascade an R-S latch
  - After CML latch, cascade another CML latch
- Strong-Arm flip-flop has the advantage of no static power dissipation and full CMOS output levels

[J. Kim]

Strong-Arm Latch

CML Latch

[Toifl]
StrongARM Latch Operation
[J. Kim TCAS1 2009]

- 4 operating phases: reset, sampling, regeneration, and decision
StrongARM Latch Operation – Sampling Phase

[J. Kim TCAS1 2009]

- Sampling phase starts when clk goes high, \( t_0 \), and ends when PMOS transistors turn on, \( t_1 \)
- M1 pair discharges \( X/X' \)
- M2 pair discharges out+/−

\[
\frac{v_{out}(s)}{v_{in}(s)} = \frac{g_{m1}g_{m2}}{sC_{out}C_x \left( s + \frac{g_{m2}(C_{out} - C_x)}{C_{out}C_x} \right)}
\]

\[
\approx \frac{g_{m1}g_{m2}}{s^2C_{out}C_x} = \frac{1}{s^2\tau_{s1}\tau_{s2}}
\]

where \( \tau_{s1} \equiv C_x/g_{m1}, \tau_{s2} \equiv C_{out}/g_{m2} \)
• Regeneration phase starts when PMOS transistors turn on, $t_1$, until decision time, $t_2$

• Assume M1 is in linear region and circuit no longer sensitive to $v_{in}$

• Cross-coupled inverters amplify signals via positive-feedback:

\[
G_R = \exp\left(\frac{t_2 - t_1}{\tau_R}\right)
\]

\[
\tau_R = C_{out}/(g_{m2,r} + g_{m3,r})
\]
StrongARM Latch Operation – Diff. Output
[J. Kim TCASI 2009]
Conventional RS Latch

- RS latch holds output data during latch pre-charge phase

- Conventional RS latch rising output transitions first, followed by falling transition
Optimized RS Latch

- Optimizing RS latch for symmetric pull-up and pull-down paths allows for considerable speed-up.

- During evaluation, large driver transistors are activated to change output data and the keeper path is disabled.

- During pre-charge, large driver transistors are tri-stated and small keeper cross-coupled inverter activated to hold data.

Evaluation Mode (Clock High)  Driver Branches
Hold/ Precharge Mode (Clock Low)  Keeper Branches

[Nikolic J SSC 2000]
Delay Improvement w/ Optimized RS Latch

- Strong-Arm flip-flop delay improves by close to a factor of two
- Has better delay performance than other advanced flip-flop topologies

[Nikolic J SSC 2000]
Sampler Analysis

- Sampler analysis provides insight into comparator operation

\[ v_{\text{sample}} = \int_{-\infty}^{\infty} v_{\text{in}}(\tau) h(\tau) d\tau \]

Johansson JSSC 1998

- Switch can be modeled as a device which determines a weighted average over time of the input signal
- The weighting function is called the sampling function
Sampling Function Properties

- Sampling function should (ideally) integrate to 1
  \[ \int_{-\infty}^{\infty} h(\tau) d\tau = 1 \]

- Ideal sampling function is a delta function
  - Sampled value is only a function of exact sampling time

\[ \text{ideal } h(\tau) = \delta(t) \]

\[ v_{sample} = \int_{-\infty}^{\infty} v_{in}(\tau)h(\tau) d\tau \]
Sampling Function Example

- Practical sampling function will weight the input signal near the nominal sampling time

\[ v_{sample} = \int_{-\infty}^{\infty} v_{IN}(\tau) h(\tau) d\tau \]

Practical \( h(\tau) \)
Sampler Frequency Response

- Fourier transform of the sampling function yields the sampler frequency response
- Sampler bandwidth is a function of sample clock transition time

\[ h(\tau) \]

\[ F.T.\{h(-\tau)\} \]
Sampler Aperture Time

- Aperture time is defined as the width of the SF peak were a certain percentage (80%) of the sensitivity is confined.

\[ w_{80} = t_{90} - t_{10} \]

\[ 0.1 = \int_{-\infty}^{t_{10}} h(\tau) d\tau \]

\[ 0.9 = \int_{-\infty}^{t_{90}} h(\tau) d\tau \]
Clocked Comparator LTV Model

Comparator can be viewed as a noisy nonlinear filter followed by an ideal sampler and slicer (comparator).

Small-signal comparator response can be modeled with an ISF $\Gamma(\tau) = h(t, \tau)$.
Clocked Comparator ISF

- Comparator ISF is a subset of a time-varying impulse response \( h(t, \tau) \) for LTV systems:
  \[
y(t) = \int_{-\infty}^{\infty} h(t, \tau) \cdot x(\tau) d\tau
  \]
- \( h(t, \tau) \): system response at \( t \) to a unit impulse arriving at \( \tau \)
- For LTI systems, \( h(t, \tau) = h(t-\tau) \) (convolution)
- ISF \( \Gamma(\tau) = h(t_0, \tau) \)
  - For comparators, \( t_0 \) is before decision is made
  - Output voltage of comparator
    \[
    v_o(t_{obs}) = \int_{-\infty}^{\infty} v_i(\tau) \cdot \Gamma(\tau) d\tau
    \]
  - Comparator decision
    \[
    D_k = \text{sgn}(v_k) = \text{sgn}(v_o(t_{obs} + kT)) = \text{sgn}\left(\int_{-\infty}^{\infty} v_i(\tau) \cdot \Gamma(\tau) d\tau\right)
    \]
Clocked Comparator ISF

- ISF shows sampling aperture or timing resolution
- In frequency domain, it shows sampling gain and bandwidth

\[
\text{ISF } \Gamma(\tau) \quad \text{F.T. } \{ \Gamma(-\tau) \}
\]

[J. Kim]
Characterizing Comparator ISF

1. Find Metastable $V_{ms}(\tau) = V_{os}(t \to \infty, \tau)$ such that $V(\text{out}+) = V(\text{out}-)$

2. Measure $V_{MS}$ for varying $\tau$

3. Derive ISF

$$SSF_{norm}(\tau) = \frac{V_{MS}(\tau) - V_L}{V_H - V_L}$$

$$ISF_{norm}(\tau) = \frac{d}{d\tau}SSF_{norm}(\tau)$$

[Jeeradit VLSI 2008]
Comparator ISF Measurement Setup

**Strong-Arm Latch**

**CML Latch**

**Strong-Arm Comparator**

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<td>14.9</td>
<td>67.6</td>
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<td>Sim w Channel</td>
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<td>1.4</td>
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<tr>
<td>Lab</td>
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<td>1.4</td>
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**CML Comparator**

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<tbody>
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<td>6.8</td>
<td>88.8</td>
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<tr>
<td>Lab</td>
<td>280</td>
<td>1.4</td>
<td>N/A</td>
</tr>
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Note: the aperture time is defined as the width that contains 80% of the sensitivity similar to [1]
Comparison of SA & CML Comparator (1)

- CML latch has higher sampling gain with small input pair
- StrongARM latch has higher sampling bandwidth
  - For CML latch increasing input pair also directly increases output capacitance
  - For SA latch increasing input pair results in transconductance increasing faster than capacitance

[Jeeradit VLSI 2008]
• Sampling time of SA latch varies with VDD, while CML isn’t affected much
Low-Voltage SA – Schinkel ISSCC 2007

Advantages:
• Less stacking
• Wide tail for fast latching
• More isolation between input and output
• Small tail → input stage in weak inversion → less offset from latch

• Does require clk & clk_b
  • How sensitive is it to skew?
90nm CMOS simulations. ΔVin=50mV. Circuits designed for equal offset σos=10mV at V_cm=1.1V
Low-Voltage SA – Goll TCAS2 2009

- Similar stacking to conventional SA latch
- However, now P0 and P1 are initially on during evaluation which speeds up operation at lower voltages
- Does require clk & clk_b
  - How sensitive is it to skew?
Low-Voltage SA – Goll TCAS2 2009

![Graph showing the delay of OUT-OUT vs. supply voltage of comparator V_{Co} (V)]
Integrating RX & High-Frequency Noise

- A small aperture time is desired in most receiver samplers
- However, high-frequency noise can degrade performance at sampling time
  - Can be an issue in single-ended systems with excessive Ldi/dt switching noise
- Integrating the input signal over a sampling interval reduces the high-frequency noise impact
Integrating Amplifier

- Differential input voltage converted to a differential current that is integrated on the sense nodes’ capacitance
Windowed Integration

- Windowing integration time can minimize transition noise and maximize integration of valid data.

[Zerbe JSSC 2001]
RX Sensitivity

- RX sensitivity is a function of the input referred noise, offset, and minimum latch resolution voltage
  \[ v_{s}^{pp} = 2v_{n}^{rms} \sqrt{SNR} + v_{\text{min}} + v_{\text{offset}} \]

- Gaussian (unbounded) input referred noise comes from input amplifiers, comparators, and termination
  - A minimum signal-to-noise ratio (SNR) is required for a given bit-error-rate (BER)
    \[
    \text{For BER} = 10^{-12} \ (\sqrt{\text{SNR}} = 7)
    \]

- Minimum latch resolution voltage comes from hysteresis, finite regeneration gain, and bounded noise sources
  - Typical \( v_{\text{min}} < 5mV \)

- Input offset is due to circuit mismatch (primarily \( V_{\text{th}} \) mismatch) & is most significant component if uncorrected
RX Sensitivity & Offset Correction

- RX sensitivity is a function of the input referred noise, offset, and min latch resolution voltage

\[ v_{S}^{pp} = 2v_{n}^{rms} \sqrt{SNR} + v_{\min} + v_{\text{offset}}^{*} \]  

Typical Values: \( v_{n}^{rms} = 1mV_{rms} \), \( v_{\min} + v_{\text{offset}}^{*} < 6mV \)

For BER = 10^{-12} (\sqrt{SNR} = 7) \( \Rightarrow v_{S}^{pp} = 20mV_{pp} \)

- Circuitry is required to reduce input offset from a potentially large uncorrected value (>50mV) to near 1mV
Input Referred Offset

- The input referred offset is primarily a function of $V_{th}$ mismatch and a weaker function of $\beta$ (mobility) mismatch

\[ \sigma_{V_t} = \frac{A_{V_t}}{\sqrt{WL}}, \quad \sigma_{\Delta \beta/\beta} = \frac{A_\beta}{\sqrt{WL}} \]

- To reduce input offset 2x, we need to increase area 4x
  - Not practical due to excessive area and power consumption
  - Offset correction necessary to efficiently achieve good sensitivity

- Ideally the offset “A” coefficients are given by the design kit and Monte Carlo is performed to extract offset sigma

- If not, here are some common values:
  - $A_{Vt} = 1\text{mV}\mu\text{m per nm of } t_{ox}$
    - For our default 90nm technology, $t_{ox}=2.8\text{nm} \rightarrow A_{Vt} \sim 2.8\text{mV}\mu\text{m}$
  - $A_\beta$ is generally near $2\%\mu\text{m}$
Offset Correction Range & Resolution

• Generally circuits are designed to handle a minimum variation range of $\pm 3\sigma$ for 99.7% yield
• Example: Input differential transistors $W=4\mu m$, $L=150nm$

$$\sigma_{V_t} = \frac{A_{V_t}}{\sqrt{WL}} = \frac{2.8mV\mu m}{\sqrt{4\mu m \cdot 150nm}} = 3.6mV, \quad \sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{WL}} = \frac{2\%\mu m}{\sqrt{4\mu m \cdot 150nm}} = 2.6\%$$

• If we assume (optimistically) that the input offset is only dominated by the input pair $V_t$ mismatch, we would need to design offset correction circuitry with a range of about $\pm 11mV$
• If we want to cancel within $1mV$, we would need an offset cancellation resolution of 5bits, resulting in a worst-case offset of

$$1\text{LSB} = \frac{\text{Offset Correction Range}}{2^{\text{Resolution} - 1}} = \frac{22mV}{2^5 - 1} = 0.65mV$$
Current-Mode Offset Correction Example

- Differential current injected into input amplifier load to induce an input-referred offset that can cancel the inherent amplifier offset
  - Can be made with extended range to perform link margining
- Passing a constant amount of total offset current for all the offset settings allows for constant output common-mode level
- Offset correction performed both at input amplifier and in individual receiver segments of the 2-way interleaved architecture
Capacitive Offset Correction Example

- A capacitive imbalance in the sense-amplifier internal nodes induces an input-referred offset.
- Pre-charges internal nodes to allow more integration time for more increased offset range.
- Additional capacitance does increase sense-amp aperture time.
- Offset is trimmed by shorting inputs to a common-mode voltage and adjusting settings until an even distribution of “1”s and “0”s are observed.
- Offset correction settings can be sensitive to input common-mode.
**Demultiplexing RX**

- Demultiplexing allows for lower clock frequency relative to data rate.
- Gives extra regeneration and pre-charge time in comparators.
- Need precise phase spacing, but not as sensitive to duty-cycle as TX multiplexing.
1:4 Demultiplexing RX Example

- Increased demultiplexing allows for higher data rate at the cost of increased input or pre-amp load capacitance
- Higher multiplexing factor more sensitive to phase offsets in degrees
Next Time

• Equalization theory and circuits
  • Equalization overview
  • Equalization implementations
    • TX FIR
    • RX FIR
    • RX CTLE
    • RX DFE
  • Setting coefficients
  • Equalization effectiveness
  • Alternate/future approaches