Texas A&M University
Department of Electrical and Computer Engineering

ECEN 720 – High-Speed Links

Spring 2013

Exam #1

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are 6 pages in your exam
- You may use one double-sided page of notes and equations for the exam
- Good Luck!

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Name: ________ SAM PALERMO ________

UIN: ____________________________
Problem 1 (30 points)
a) A 1V step is launched onto the channel below at t=0ns. (20 points)
   i. Calculate the reflection coefficient at the source, \( k_S \), and the end termination, \( k_T \)
   ii. Fill in the lattice diagram below until the source voltage, \( V_S \), has reached to within 10mV
       of its final value.
   iii. Also plot the source voltage, \( V_S \), and make sure to label the voltage values in the transient
        plot.

\[
\text{Initial Voltage} = \frac{50}{80+50} = 0.385 \text{V}, \quad \text{Final Voltage} = \frac{20}{80+20} = 0.2 \text{V}
\]

\[
k_S = \frac{80-50}{80+50} = 0.23 \quad k_T = \frac{80-50}{20+50} = -0.429
\]

b) An ideal TDR (\( t_c=0 \)) measurement of an unknown channel displays the following waveform
below. Sketch the channel model and give values for any lumped elements and transmission
line characteristic impedance and length (in time). Assume all transmission lines are lossless. (10 points)
Problem 2 (20 points)
A channel has the pulse response, \( y^{(1)} \), below for a "1" bit.

a. Find the channel's worst-case eye height at this bit rate.
b. Give the channel's worst-case bit pattern at this bit rate.

\[
y^{(1)} = [0.05 \ -0.1 \ 0.5 \ 0.15 \ -0.15 \ 0.05]
\]

W.C. Eye Height = \( 2(0.5 - 0.25 - 0.25) = 0 \)

To find W.C. Bit Pattern:

Flip about cursor and invert all but cursor

\[
[0.05 \ -0.1 \ 0.05 \ 0.15 \ -0.15 \ 0.05] \Rightarrow [-0.05 \ 0.15 \ -0.15 \ 0.5 \ 0.1 \ -0.05]
\]

Then take sign

\[
[-0.05 \ 0.15 \ -0.15 \ 0.5 \ 0.1 \ -0.05] \Rightarrow [-1 \ 1 \ -1 \ 1 \ 1 \ -1]
\]

Worst-Case Eye Height = \(0\)

Worst-Case Bit Pattern = \([-1 \ 1 \ -1 \ 1 \ -1 \ 1]\) (worst-case
\[-1 \ -1 \ 1 \ -1 \ 1 \ -1\] (worst-case
\[\text{by linearity}\]
Problem 3 (25 points)

For the circuit below, use the following NMOS parameters
\[ K_{P_N} = \mu_n C_{ox} = 600 \mu A/V^2, \; V_{TN} = 0.35 V, \; \lambda_n = 0 V \]

and the following PMOS parameters
\[ K_{P_P} = \mu_p C_{ox} = 150 \mu A/V^2, \; V_{TP} = -0.35 V, \; \lambda_p = 0 V \]

For the current-mode driver below

i. Calculate the tail current \( I_{out} \) to generate a peak-to-peak differential voltage output swing of \( 400 mV \). Here assume that the NMOS termination transistors are perfectly linear.

ii. Give the common-mode value of the output voltage with the \( 400 mV \) output swing. Again, assume that the NMOS termination transistors are perfectly linear.

iii. Give the NMOS termination transistors aspect ratios for proper termination. Include \( V_{DS} \) effects and optimize the termination at the ideal output common-mode level of part (ii). Assume that the PMOS switch transistors remain in saturation.

\[ I_{out} = \frac{V_{PPD}}{R} = \frac{400 mV}{50 \Omega} = 8 mA \]

\[ V_{out}^{+} = 4 mA (50 \Omega) = 0.2 V \]

\[ V_{out}^{-} = 0 V \]

\[ V_{out}^{+} = 0 V \]

\[ V_{out}^{-} = 4 mA (50 \Omega) = 0.2 V \]

\[ V_{out,CM} = \frac{0.2 V - 0 V}{2} = 0.1 V \]

* Sizing NMOS termination at common-mode level

Looking into drain of NMOS in deep triode

\[ R_N = \frac{1}{g_o} = \frac{1}{K N \mu W (V_{gs} - V_T - V_{os})} \]

\[ \frac{W}{L} = \frac{1}{R_N K N (V_{gs} - V_T - V_{os})} = \frac{1}{(50 \Omega)(600 \mu A/V^2)(1V - 0.25V - 0.1 W)} \]

\[ \frac{W}{L} = 60.6 \]

\[ I_{out} = 8 mA \]

\[ V_{out,CM} = 0.1 V \]

(W/L) = 60.6

* PMOS Transistors remain in saturation so shouldn't impact output termination
Problem 4 (25 points)
This problem involves analyzing the maximum performance of the comparator below. Assume that the Sample Time = 50ps, $C_{out} = C_x = 10\text{ff}$, and that all capacitors are represented by the explicitly drawn capacitors.

i. Assume that in sampling mode the effective transconductance of M1 and M2 are equal, i.e. $g_{m1} = g_{m2} = g_{m,samp}$. What is the required effective sampling transconductance to realize a small-signal sampling gain of 2 for a constant differential input voltage over the 50ps sampling time?

Hint: During sampling-mode the small-signal transfer function can be approximated as

$$\frac{v_{out}(s)}{v_{in}(s)} \approx \frac{g_{m1}g_{m2}}{s^2C_{out}C_x} = \frac{g_{m,samp}^2}{s^2C_{out}C_x}$$

ii. Given the effective total regeneration transconductance $g_{mr} = 500\mu\text{A/V}$, a sampling gain of 2, and it is required to amplify a constant 10mV differential input voltage to 500mV for a reliable decision, what is the minimum time required to make a decision ($t_2 - t_0$)?

\[\text{In sampling mode}\]

\[\frac{V_{out}(s)}{V_{in}(s)} \approx \frac{g_{m,samp}^2}{s^2C_{out}C_x} \]

\[\text{For sampling gain of 2}\]

\[\frac{g_{m,samp}^2}{C_{out}C_x} = 2 \Rightarrow g_{m,samp} = \sqrt{\frac{4C_{out}C_x}{2}} = \frac{4\text{loff}C_{off}}{(10\text{fs})^2}\]

\[g_{m1} = g_{m2} = g_{m,samp} = 400\mu\text{A/V} \]

Given a sampling gain of 2, the comparator will need to regenerate $2(10\text{mV}) = 20\text{mV}$ to make a decision.

\[\text{Regen Time} = \frac{C_{out}}{g_{m}} \ln \left( \frac{500\text{mV}}{20\text{mV}} \right) = \left( \frac{10\text{fs}}{500\mu\text{A/V}} \right) \ln \left( \frac{500\text{mV}}{20\text{mV}} \right)\]

\[\text{Decision Time} = \text{Sample Time} + \text{Regen Time} = 50\text{ps} + 64.4\text{ps} = 114.4\text{ps}\]
Key MOS Equations & Scratch Paper

Saturation: \( NMOS \quad I_{DS} = \frac{1}{2} K_P \frac{W}{L} (V_{GS} - V_{TN})^2 \)

Saturation: \( PMOS \quad I_{SD} = \frac{1}{2} K_P \frac{W}{L} (V_{SG} - |V_{TP}|)^2 \)

Triode: \( NMOS \quad I_{DS} = K_P \frac{W}{L} (V_{GS} - V_{TN} - \frac{V_{DS}}{2}) V_{DS} \)

Triode: \( PMOS \quad I_{SD} = K_P \frac{W}{L} (V_{SG} - |V_{TP}| - \frac{V_{SD}}{2}) V_{SD} \)

\( NMOS \quad g_m = \frac{\partial I_{DS}}{\partial V_{GS}}, \quad PMOS \quad g_m = \frac{\partial I_{SD}}{\partial V_{SG}} \)

\( NMOS \quad g_o = \frac{\partial I_{DS}}{\partial V_{DS}}, \quad PMOS \quad g_o = \frac{\partial I_{SD}}{\partial V_{SD}} \)