Texas A&M University
Department of Electrical and Computer Engineering

ECEN 689 – High-Speed Links

Spring 2012

Exam #1

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are 7 pages in your exam
- You may use one double-sided page of notes and equations for the exam
- Good Luck!

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Name: SAM PALERMO

UIN: 
Problem 1 (30 points)

a) A 1V step is launched onto the channel below at \( t=0 \) ns. (15 points)
   i. Calculate the reflection coefficient at the source, \( k_{rs} \), and the end termination, \( k_{rt} \).
   ii. Fill in the lattice diagram below until the source voltage, \( V_s \), has reached to within \( 20 \) mV of its final value.
   iii. Also plot the source voltage, \( V_s \), and make sure to label the voltage values in the transient plot.

\[
\begin{align*}
\text{Initial Voltage} & = \frac{50}{75} \times 1V = 0.667V \\
\text{Final Voltage} & = \frac{200}{225} \times 0.814V = 0.88V
\end{align*}
\]

\[
k_{rs} = \frac{25 - 50}{25 + 50} = -0.333 \quad k_{rt} = \frac{200 - 50}{200 + 50} = 0.6
\]

b) An ideal TDR (\( t_r=0 \)) yields the following response with a channel consisting of a 50Ω trace, a 1 inch trace with \( Z_x \) impedance, and ends in an open termination. Calculate \( Z_x \) and the equivalent \( L/\text{in} \) and \( C/\text{in} \) of the 1 inch trace. (15 points) Assume all traces are lossless.

\[
Z_x \text{ impedance discontinuity is detected aT TDR at } +t = 0.5 \text{ ns}
\]

\[
\tau = \frac{V(0.5 \text{ ns})}{V(0.5 \text{ ns}) - V(0 \text{ ns})} = 50 \text{Ω}
\]

\[
z_x = 75 \Omega
\]

\[
\tau = \frac{1}{2f} = \frac{1}{2(10^9)} = 500 \text{ ps}
\]

\[
z = \frac{V(t)}{I(t)} = \frac{500 \text{ ps}}{2 \text{ (in)}} = 150 \text{ ps/in}
\]

\[
L/\text{in} = \frac{1}{2z} = \frac{1}{2 \times 75 \Omega} = 2.67 \times 10^{-10} \text{ H/in}
\]

\[
C/\text{in} = \frac{2}{2 \pi f} = \frac{2}{2 \pi \times 10^9} = 2 \times 10^{-10} \text{ F/in}
\]
Problem 2 (20 points)
A channel has the pulse response, \(y^{(1)}\), below for a “1” bit.

a. Find the channel’s worst-case eye height at this bit rate.
b. Give the channel’s worst-case bit pattern at this bit rate.

\[
y^{(1)} = [-0.1 \ 0.6 \ 0.2 \ -0.1]
\]

\[
y_0^{(1)} = 0.6
\]

\[
\sum_{k \neq 0} y^{(1)}_{y < 0} = -0.1 - 0.1 = -0.2
\]

\[
\sum_{k \neq 0} y^{(1)}_{y > 0} = 0.2
\]

W.C. Eye Height = \(2(0.6 - 0.2 - 0.2) = 0.4\)

To find W.C. Bit Pattern:

Flip about cursor and invert all but cursor

\[
[-0.1 \ 0.6 \ 0.2 \ -0.1] \Rightarrow [0.1 \ -0.2 \ 0.6 \ 0.1]
\]

Then take sign

\[
[0.1 \ -0.2 \ 0.6 \ 0.1] \Rightarrow [1 \ -1 \ 1 \ 1]
\]

Worst-Case Eye Height = \(0.4\)

Worst-Case Bit Pattern =

\[
\begin{bmatrix}
1 & -1 & 1 & 1 \\
-1 & 1 & -1 & -1
\end{bmatrix}
\]

(Worst-case “1”)

\[
\begin{bmatrix}
1 & -1 & 1 & 1 \\
-1 & 1 & -1 & -1
\end{bmatrix}
\]

(Worst-case “1”)

by linearity
Problem 3 (15 points)

For the circuit below, use the following NMOS parameters
\[ K_{P_N} = \mu_n C_{ox} = 600 \mu A/V^2, \quad V_{TN} = 0.35V, \quad \lambda_N = 0V^{-1} \]

and the following PMOS parameters
\[ K_{P_P} = \mu_p C_{ox} = 150 \mu A/V^2, \quad V_{TP} = 0.35V, \quad \lambda_P = 0V^{-1} \]

For the current-mode driver below

i. Calculate the tail current \( I_{out} \) to generate a peak-to-peak differential voltage output swing of 500mVppd.

ii. Give the common-mode value of the output voltage with the 500mVppd output swing.

iii. Give the PMOS termination transistors aspect ratios for proper termination. Include \( V_{SD} \) effects and optimize the termination at the output common-mode level.

\[ I_{out} = \frac{V_{PPD}}{R} = \frac{500mV}{50\Omega} = 10mA \]

\[ V_{out^+} = 1V \]
\[ V_{out^-} = 1V - 5mA (50\Omega) = 0.75V \]

\[ V_{out^+} = 0.75V \]
\[ V_{out^-} = 1V \]

\[ V_{out, CM} = \frac{1 + 0.75V}{2} = 0.875V \]

* Sizing PMOS termination at common-mode level

Looking into drain of PMOS in deep triode

\[ R_P = \frac{1}{g_o} = \frac{1}{K_{P_P} \frac{W}{L} (V_{SG} - V_{TP} - V_{SD})} \]

\[ \frac{W}{L} = \frac{1}{R_P K_{P_P} (V_{SG} - V_{TP} - V_{SD})} = \frac{1}{(50\Omega) (150\mu A/V^2) (1V - 0.35V - 0.125V)} \]

\[ I_{out} = 10mA \]
\[ V_{out, CM} = 0.875V \]
\[ (W/L)_P = 254 \]
Problem 4 (15 points)

For the circuit below, use the following NMOS parameters

\[ K_{PN} = \mu_n C_{ox} = 600 \mu A/V^2, V_{TN} = 0.35 V, \lambda_n = 0 V^{-1} \]

and the following PMOS parameters

\[ K_{PP} = \mu_p C_{ox} = 150 \mu A/V^2, V_{TP} = -0.35 V, \lambda_p = 0 V^{-1} \]

Design the voltage-mode driver below to meet a 1V peak-to-peak differential output voltage swing. Give the output stage supply, and give the output stage transistors aspect ratios (W/L) to implement proper source termination. Include V_{DS} (or V_{SD}) effects and assume that it is sufficient to optimize the source termination for transmitting a static “1” or “-1” bit and that the predrive buffers swing from 0 to 1V.

For pull-up path:

Looking into PMOS drain in deep triode:

\[ R_P = \frac{1}{g_0} = \frac{1}{K_{PP} \left( \frac{W}{L} \right) (V_{GS} - V_{TP} - V_{SD})} \]

For pull-down path:

Looking into NMOS drain in deep triode:

\[ R_N = \frac{1}{g_0} = \frac{1}{K_{PN} \left( \frac{W}{L} \right)_0 (V_{GS} - V_{TN} - V_{DS})} \]

\[ \left( \frac{W}{L} \right)_0 = \frac{R_N K_{PN} (V_{GS} - V_{TN} - V_{DS})}{20 \Omega (600 \mu A/1 - 0.35)} \]

\[ (W/L)_0 = 128 \]

\[ (W/L)_1 = 741 \]
Problem 5 (20 points)
This problem involves analyzing the maximum performance of the comparator below. Assume that the Sample Time=50ps and the Sample Gain=1.

i. If the regeneration time constant $\tau_R=20\text{ps}$ and it is required to amplify a 10mV differential input voltage to 500mV for a reliable decision, what is the minimum time required to make a decision $(t_2 - t_0)$?

ii. Given the effective total regeneration transconductance $g_{m_e}=300\mu\text{A/V}$, what is the maximum total output capacitance that the comparator can drive and maintain the 20ps $\tau_R$?

In order to amplify 10mV to 500mV need a regeneration time $= \tau_R \ln \left( \frac{500\text{mV}}{10\text{mV}} \right) = 78.2\text{ps}$

Decision Time = Sample Time + Regeneration Time

$= 50\text{ps} + 78.2\text{ps} = 128\text{ps}$

Max $C_{out} = g_{m_e} \tau_R = (300\mu\text{A/V})(20\text{ps}) = 6\text{fF}$

Min $(t_2 - t_0) = 128\text{ps}$

Max $C_{out} = 6\text{fF}$
Key MOS Equations & Scratch Paper

Saturation: \( NMOS \quad I_{DS} = \frac{1}{2} K P_N \frac{W}{L} (V_{GS} - V_{TN})^2 \)

Saturation: \( PMOS \quad I_{SD} = \frac{1}{2} K P_P \frac{W}{L} (V_{SG} - |V_{TP}|)^2 \)

Triode: \( NMOS \quad I_{DS} = K P_N \frac{W}{L} \left( V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right) V_{DS} \)

Triode: \( PMOS \quad I_{SD} = K P_P \frac{W}{L} \left( V_{SG} - |V_{TP}| - \frac{V_{SD}}{2} \right) V_{SD} \)

\( NMOS \quad g_m = \frac{\partial I_{DS}}{\partial V_{GS}}, \quad PMOS \quad g_m = \frac{\partial I_{SD}}{\partial V_{SG}} \)

\( NMOS \quad g_o = \frac{\partial I_{DS}}{\partial V_{DS}}, \quad PMOS \quad g_o = \frac{\partial I_{SD}}{\partial V_{SD}} \)