ECEN620: Network Theory
Broadband Circuit Design
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Lecture 12: Loop Filter Circuits

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Announcements & Agenda

- HW2 is due Friday Oct. 12

- Loop filter circuits
  - Voltage-mode filters
  - Charge-Pump PLL PI filter
  - Filter with capacitive multiplier
The lowpass loop filter extracts the average of the phase detector error pulses in order to produce the VCO control voltage.
Passive Lag-Lead Filter

- Dimensionless voltage-mode filter used in Type-1 PLLs
- Called lag-lead because the pole is at a lower frequency than the zero
- Ideally, the passive filter displays no nonlinearity
Active Lag-Lead Filter

- Dimensionless voltage-mode filter used in Type-1 PLLs
- Active filter allows for potential gain in the loop filter
- Opamp noise and linearity can impact PLL performance

\[ F(s) = K_a \frac{1 + s \tau_2}{1 + s \tau_1} \]

\[ \tau_1 = R_1 C \quad \tau_2 = R_2 C \quad K_a = -\frac{C_1}{C_2} \]
Active Proportional-Integral (PI) Filter

- Dimensionless voltage-mode filter used in Type-2 PLLs
- Opamp noise and linearity can impact PLL performance
- Opamp open loop gain limits the low-frequency gain and ideal transfer function

\[ F(s) = -\frac{1 + s\tau_2}{s\tau_1} \]

\[ \tau_1 = R_1C \quad \tau_2 = R_2C \]
Closed-Loop Transfer Functions

Passive Lag - Lead Filter

\[ F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \rightarrow H(s) = \frac{K_{pp}K_{VCO}\tau_2}{\tau_1 + \tau_2} \left( s + \frac{1}{\tau_2} \right) \]

\[ \omega_n = \sqrt{\frac{K_{pd}K_{VCO}}{N(\tau_1 + \tau_2)}} \]

\[ \zeta = \frac{\omega_n}{2} \left( \frac{\tau_2 + N}{K_{pd}K_{VCO}} \right) \]

Active Lag - Lead Filter  (Assuming Overall Negative Feedback)

\[ F(s) = K_a \frac{1 + s\tau_2}{1 + s\tau_1} \rightarrow H(s) = \frac{K_{pd}K_aK_{VCO}\tau_2}{\tau_1} \left( s + \frac{1}{\tau_2} \right) \]

\[ \omega_n = \sqrt{\frac{K_{pd}K_aK_{VCO}}{N\tau_1}} \]

\[ \zeta = \frac{\omega_n}{2} \left( \frac{\tau_2 + N}{K_{pd}K_aK_{VCO}} \right) \]

Active PI Filter  (Assuming Overall Negative Feedback)

\[ F(s) = \frac{1 + s\tau_2}{s\tau_1} \rightarrow H(s) = \frac{K_{pd}K_{VCO}\tau_2}{\tau_1} \left( s + \frac{1}{\tau_2} \right) \]

\[ \omega_n = \sqrt{\frac{K_{pd}K_{VCO}}{N\tau_1}} \]

\[ \zeta = \frac{\omega_n}{2} \tau_2 \]
Charge Pump PLL Passive PI Loop Filter

- Simple passive filter is most commonly used
- Integrates low-frequency phase errors onto C1 to set average frequency
- Resistor (proportional gain) isolates phase correction from frequency correction
- Primary capacitor C1 affects PLL bandwidth
- Zero frequency affects PLL stability
- Resistor adds thermal noise which is band-pass filtered by PLL
Loop Filter Transfer Function

- Neglecting secondary capacitor, $C_2$

$$F(s) = \frac{V_c(s)}{I_e(s)} = \frac{R \left( s + \frac{1}{RC_1} \right)}{s}$$
Loop Filter Transfer Function

- With secondary capacitor, $C_2$

$$Z(s) = \frac{\frac{1}{C_2} \left( \frac{1}{s + \frac{1}{RC_1}} \right)}{s^2 + \frac{s(C_1 + C_2)}{RC_1C_2}}$$

VCO Control Voltage

![Diagram with components and transfer function equation]

Layout Extracted Loop Filter Frequency Response

- Pole at 0Hz
- Zero at $f = \frac{1}{2\pi RC_1} = 80.5$kHz
- Second Pole at $f = \frac{C_1 + C_2}{2\pi RC_1C_2} = 915$kHz
Why have C2?

- Secondary capacitor smooths control voltage ripple
- Can’t make too big or loop will go unstable
  - \( C_2 < C_1/10 \) for stability
  - \( C_2 > C_1/50 \) for low jitter

![PLL Synthesizing a 380MHz Signal](image)
Loop Filter Resistors

- Poly, diffusion, and N-well resistors are commonly used
- MOSFET resistors can be used if the resistor is placed “below” the C1 cap
  - This ensures a constant $V_{GS}$ voltage on the transistor
- Programmable R value possible with switches
  - Switches should be CMOS transmission gates to minimize parasitic switch resistance variation with control voltage level
  - Good practice is to make $R_{switch} < 10\%$ of the main filter $R$ to minimize the impact of switch resistance variations
R or C on Top?

• Ideally, the loop filter has the same transfer function and transient response independent of the RC order.
• In reality, the bottom-plate capacitance and switch resistance variation will impact this ideal transfer function.
• If the cap is on top, the bottom-plate capacitance will introduce another high frequency pole.
• If the resistor is on top, any switch resistance will have increased variation with the control voltage level.

[Fischette]
Loop Filter Capacitors

• To minimize area, we would like to use highest density caps

• Thin oxide MOS cap gate leakage can be an issue
  • Similar to adding a non-linear parallel resistor to the capacitor
  • Leakage is voltage and temperature dependent
  • Will result in excess phase noise and spurs

• Metal caps or thick oxide caps are a better choice
  • Trade-off is area

• Metal cap density can be < 1/10 thin oxide caps

• Filter cap frequency response can be relatively low, as PLL loop bandwidths are typically 1-50MHz
Third-Order Loop Filter

To suppress the VCO (inductor Q~2) noise, a PLL loop bandwidth = 270kHz. Phase margin is around 51 degree.

The 160pF capacitance in TSMC 0.35um CMOS takes about 0.2mm^2. To reduce its area, it is implemented via a 10pF capacitor scaled up by a factor of 16.
capacitor multiplier

Current ratio $M = 15$

Capacitance $\times 16$
capacitor multiplier & simulation

\[
y_{\text{in}} = \frac{i_{\text{in}}}{v_{\text{in}}} = g_{0A} + s \left[ C_{p2} + (M + 1)C_i \frac{1 + s}{1 + s \frac{C_p1}{g_{m1}}} \right].
\]

(7)

Current ratio \( M = 15 \)

Capacitance \( \times 16 \)

\[ \omega_{c1} = \frac{g_{0A}}{C_{p2} + (M + 1)C_i} \approx \frac{g_{0A}}{C_1} \]

\[ \omega_{c2} = \frac{g_{m1}}{(C_i + C_{p1})} \approx \frac{(M + 1)g_{m1}}{C_1} \]

\[ \omega_{c3} = \frac{(M + 1)g_{m1}}{C_{p1}}. \]

\( \omega_1 \) and \( \omega_3 \) are poles, \( \omega_2 \) is a zero
Simulation of loop filter with capacitance scaling

- It shows that with capacitance scaling the large capacitor in the loop filter can be easily integrated on chip within small area.
- This approach is simple and the leakage is very small.
Next Time

- More Advanced Loop Filters
- VCOs