ECEN 474: (Analog) VLSI Circuit Design

Fall 2012
MWF 9:10-10:00, ETB 1037
http://www.ece.tamu.edu/~spalermo/ecen474.html

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Office Hours: MW 3:00-4:30
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Prerequisite: ECEN 326

(Optional)

References:
3. Technical Papers

Class Notes: Posted on the web and will hand out hard copies in class

Objectives: At the end of this course, students be able to
1. To discuss basic transistor models and layout techniques for design and characterization of analog integrated circuits.
2. To study the most important building blocks in CMOS technologies and understand their advantages and limitations.
3. To design basic analog IC circuits considering practical parameters.
4. To use the IC design tools, especially Cadence, Spectre, Spice, and Matlab.
5. We expect to design and fabricate some projects at the end of the semester.

Grading:
- Exams 60%
  o Three Midterm Exams (20% each)
  o Closed book
  o One double sided 8.5x11 note sheet allowed
  o No make-up exams except for university excused absences
  o No Final Exam
- Homework 10%
  o You are encouraged to work together with your colleagues on the homework. However, each student must turn in an independent write-up.
  o No late homework will be graded
- Laboratory 20%
- Final Project 10%
  o Report and PowerPoint presentation required
Grading Policy*:

<table>
<thead>
<tr>
<th>Letter Grade</th>
<th>x = Your Average</th>
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<tbody>
<tr>
<td>A</td>
<td>≥ 90.00</td>
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<tr>
<td>B</td>
<td>89.99 ≥ x ≥ 80.00</td>
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<tr>
<td>C</td>
<td>79.99 ≥ x ≥ 70.00</td>
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<td>D</td>
<td>69.99 ≥ x ≥ 60.00</td>
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<tr>
<td>F</td>
<td>59.99 ≥ x</td>
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*This is the lowest grade that you are guaranteed for your raw average, x. Depending on the relative performance of the class, your grade MAY be adjusted higher. Undergraduate and graduate students’ performance will be judged independently.

Outline

I. Introduction and MOS models
   - Basis of CMOS Technology
   - Basic equations for the MOS transistor
   - Model level 3
   - Second order effects
   - SPICE parameters
   - Technology characterization

II. CMOS Technologies and Layouts
   - CMOS technology
   - CMOS Layout and Design Rules
   - Layout considerations (transistors, capacitors, resistors and inductors)
   - Latch-up considerations
   - Advanced technologies: design examples

III. Current Mirrors and Differential Pairs
   - Basic amplifier
   - Ideal and Basic current mirror
   - Basic amplifiers using current mirrors (design considerations, and evaluation techniques)
   - High-output impedance current mirrors
   - High dc gain amplifiers (cascode, folded-cascode, triple cascode, and regulated cascode)
   - Current mirror characterization techniques (DC and AC)
   - Differential pair
   - Frequency response
   - Noise considerations
   - Class AB amplifiers
   - Design examples

IV. Voltage References and Differential Pairs (* most of this material is taken from Gray’s book)
   - Supply independent current sources (*)
   - Bootstrap Biasing (*)
   - Temperature coefficient (*)
   - Bandgap references (*)
• Differential Pair (large signal characteristics)
• Differential Pair (small signal characteristics)
• Frequency response (dc gain, poles and zeros)
• Node impedances, low-frequency and high-frequency poles
• Design examples

V. OTA Design
• First stage
• DC considerations
• AC considerations
• Noise considerations: Output and input referred noise
• Global design strategy
• Three Current Mirror OTA
• Cascode output stages
• Telescopic amplifier
• Folded-cascode OTA
• OTA characterization

VI. Design of a Miller OPAMP
• First stage
• Output stage
• DC considerations
• Stability considerations
• Settling time and slew-rate
• DC offset and PSRR
• Noise considerations
• Design strategy

VII. Advanced Techniques
• Enhanced output stages
• Fully-differential structures
• Common-mode feedback: limitations and design techniques
• Phase compensation techniques
• Linear OTAs: Continuous-time circuits
• Linearization techniques: IM3 and Source degeneration
• Tuning techniques
• Design examples
<table>
<thead>
<tr>
<th>Topic</th>
<th>Week</th>
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<tr>
<td>I. Introduction and MOS models</td>
<td>Week 1-4</td>
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<tr>
<td>II. CMOS Technologies and Layouts</td>
<td>Sep. 26</td>
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<tr>
<td>Review Session</td>
<td>Sep. 24</td>
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<tr>
<td>I. CMOS Technologies and Layouts</td>
<td>Sep. 26</td>
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<tr>
<td>Review Session</td>
<td>Sep. 24</td>
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<tr>
<td>III. Current Mirrors and Differential Pairs</td>
<td>Week 5-9</td>
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<tr>
<td>IV. Voltage References and Differential Pairs</td>
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<td>V. OTA Design (Part 1)</td>
<td>Oct. 29</td>
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<tr>
<td>Review Session</td>
<td>Oct. 29</td>
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<td>VI. OTA Design (Part 2)</td>
<td>Oct. 31</td>
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<td>VII. Miller OpAmp Design</td>
<td>Week 10-14</td>
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<td>VIII. Advanced Topics</td>
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<td>Review Session</td>
<td>Nov. 28</td>
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<td>3rd Exam</td>
<td>Nov. 30</td>
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<td>Project Report Due</td>
<td>Dec. 4</td>
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<td>Project Presentation</td>
<td>Dec. 10</td>
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*Exam dates are approximate and subject to change with reasonable notice.

Laboratory safety guidelines will be distributed at the beginning of the semester, they are to be reviewed, filled out, and turned back to the department.

Americans with Disabilities Act (ADA) Policy Statement:
The Americans with Disabilities Act (ADA) is a federal anti-discrimination statute that provides comprehensive civil rights protection for persons with disabilities. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe you have a disability requiring an accommodation, please contact the Department of Student Life, Services for Students with Disabilities, in Room 126 of the Koldus Building or call 845-1637.

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Build the Hell Outta Analog VLSI Circuits!