Lecture 14: Folded Cascode OTA
Announcements & Agenda

- HW4 Due Wednesday 10/31
- Exam 2 Friday 11/2
- Single-Stage Cascode OTA
- Folded Cascode OTA
**Simple OTA**

- **Gain is limited by single-transistor output resistance**

DC Gain \( A_v = G_m R_{out} = g_m \left( r_{o2} \parallel r_{o6} \right) \)
Single-Stage Cascode OTA

DC Gain \( A_v = G_m R_{out} \approx g_{m1} \left( g_{m4} r_{o2} r_{o4} \parallel g_{m6} r_{o8} r_{o6} \right) \)

- Gain is larger by a \( g_m r_o \) factor
- Output swing range is limited due to large compliance voltage of cascode current source load

[Razavi]
Single-Stage Cascode OTA

Unity Gain Feedback Voltage Range

Maximum $V_{\text{out}}$ set by M2 saturation

$$V_{\text{out}} \leq V_x + V_{TH2}$$

Minimum $V_{\text{out}}$ set by M4 saturation

$$V_{\text{out}} \geq V_b - V_{TH4}$$

As $V_b = V_x + V_{GS4}$ and plugging $V_x$ into M2 sat condition

Output (& Input) Range = $V_{TH4} - (V_{GS4} - V_{TH2})$

Less than a $V_{TH}$ !!!

- Cascode configuration constrains output & unity-gain swing
Folded Cascode Circuits

- “Folding” about the cascode node will increase input and output swing range

[Razavi]

PMOS Input & NMOS Cascode

NMOS Input & PMOS Cascode
Folded Cascode OTA

[Razavi]
Folded Cascode OTA
Unity Gain Feedback Voltage Range

- Maximum $V_{\text{out}}$ set by $MP$ saturation
  \[ V_{\text{out}} \leq V_{b2} + |V_{THP}| \]

- Minimum $V_{\text{out}}$ set by output NMOS cascode or tail current source saturation
  \[ V_{\text{out}} \geq V_{\text{DSATNC}} + V_{\text{DSATN}} \quad \text{OR} \quad V_{\text{out}} \geq V_{\text{DSATI_{tail}}} + V_{GS1} \]

- With proper (high-value) choice of $V_{b2}$, a decent output and input swing range can be achieved
Folded-Cascode OTA: gm, rout and poles?

\( V_{B1} \) and \( V_{B2} \) must keep \( M_1 \)

- \( M_5 \) in saturation region

\[ V_{B2} > V_{sat,4} + V_{GS3} \quad \text{(for M4 sat)} \]

\[ V_{B1} < V_{DD} - V_{sat,5} - V_{SG2} \quad \text{(for M5 sat)} \]

Notice that \( I_{D5} \) biases both \( M_2 \) and \( M_1 \)

\[ G_m = g_{m1} \quad ; \quad r_{out} \approx (r_{ds2} g_{m2} r_{ds1}) || (r_{ds3} g_{m3} r_{ds4}) \]
Example: Folded-Cascode OPAMP

Find the gain and the phase from input to output and from input to node 2.

The low frequency gain is 77 dB and the unity gain frequency is around 80 MHz.

The behavior of the gain from the input to node 2 is interesting: above the dominant pole.

\[ \omega_{z2} \approx \left( \frac{g_{m2}}{g_{o1} + g_{o5}} \right) \left( \frac{1}{r_{out} C_L} \right) \]
TYPICAL FOLDED CASCODE (One of the most popular circuit in ADCs)

- There is a limitation due the non-dominant pole

- $I_{BIAS} \uparrow \implies A_{DC} \downarrow$

- $W_{casc} \downarrow \implies V_{DSAT} \uparrow$

$$\frac{V_o}{V_{in}} = -\frac{g_{md}}{g_{o}} \left( \frac{1}{1 + s \frac{C_p}{g_{mc}}} \right) \left( \frac{1}{1 + s \frac{C_L}{g_{o}}} \right)$$
FOLDED-CASCODE OTA

Frequency response:

Righ hand side

- Righ hand side: 2 poles (at V\textsubscript{W} and V\textsubscript{out})
- Left hand side: 4 poles !!! (at V\textsubscript{X}, V\textsubscript{Y}, V\textsubscript{Z} and V\textsubscript{out})

The poles at Vy and Vz are associated to N-type transistors \(\Rightarrow\) higher frequencies

\[
A_V(s) \approx g_{m1}R_{out} \cdot \frac{1}{sC_{out}} \cdot \frac{1}{sC_{PC}}
\]

\[
1 + \frac{1}{g_{out}} \cdot \frac{1}{g_{mp}}
\]
Output referred noise

- M1 produces an output current given by
  \[ i_{01} = g_{m1} v_{n1} \]

- Each transistor M2 generates a differential output current
  \[ i_{02} = g_{m2} v_{n2} \]

- Similarly, for each transistor M5
  \[ i_{05} = g_{m5} v_{n5} \]

- At low and medium frequencies, noise contribution of the cascode transistors can be neglected (M3 and M4)

Remember

\[ i_{eq}^2 = \frac{8}{3} kT g_m \]

\[ i_{out}^2 = 2(i_{eq1}^2 + i_{eq2}^2 + i_{eqn}^2) \]
FOLDED-CASCODE OTA

Noise density and noise level

⇒ The output referred current spectral density is

\[ i_{0T}^2 = 2\left(g_{m1}^2 v_{n1}^2 + g_{m2}^2 v_{n2}^2 + g_{m5}^2 v_{n5}^2\right) \]

⇒ And the input referred noise density becomes

\[ v_{eq,\text{in}}^2 = 2\frac{g_{m1}^2 v_{n1}^2 + g_{m2}^2 v_{n2}^2 + g_{m5}^2 v_{n5}^2}{g_{m1}^2} \]

⇒ The noise level is

\[ v_{\text{noise}} = \sqrt{\int_{BW} v_{eq,\text{in}}^2 df} = \sqrt{\int_{BW} 2\left(v_{n1}^2 + \frac{g_{m2}^2 v_{n2}^2}{g_{m1}^2} + \frac{g_{m5}^2 v_{n5}^2}{g_{m1}^2}\right) df} \]
Noise level for the folded-cascode OTA

\[ V_{\text{noise}} = \sqrt{\int_{BW} 2 \left( \frac{v_{n1}^2 + g_{m2}^2 v_{n2}^2 + g_{m5}^2 v_{n5}^2}{g_{m1}^2} \right) df} \]

\( \approx \left( \frac{8kT}{g_{m1}} (BW) \right) \left( \sqrt{1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m5}}{g_{m1}}} \right) \]

Low-noise is associated with large \( g_{m1} \) and relatively small \( g_{m2} \) and \( g_{m5} \)

Or for a dominant (single) pole system with \( NBW = (\pi/2)BW \)

\[ V_{\text{noise}} = \sqrt{\int_{BW} \frac{16}{3} kT \left( \frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2} + \frac{g_{m5}}{g_{m1}^2} \right) df} \]

Let's consider thermal noise \( (v_n^2 = (8/3)K\tau)/(g_m) \)

Noise of diff pair
Noise Factor
(due to other transistors)
Next Time

- Two Stage Miller OTA