ECEN 474: (Analog) VLSI Circuit Design
Fall 2012

Lecture 8: Current Mirrors

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Announcements & Agenda

• HW2 due Monday

• Reading
  • Razavi Chapter 5

• Biasing in ICs

• Simple Current Mirror

• Transistor Small-Signal Impedances
  • Simple Amplifiers

• Other Current Mirror Topologies
Current Source Properties

• Output Resistance

Finite output resistance degrades current source accuracy and amplifier gain

• Other important properties:
  • Voltage headroom (compliance voltage)
  • Accuracy
  • Noise
How Should We Bias Our Circuits?

- Resistive Biasing
  - Assuming saturation

\[
I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( V_G - V_{Tn} \right)^2
\]

\[
= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( \frac{R_{G2}}{R_{G1} + R_{G2}} V_{dd} - V_{Tn} \right)^2
\]

- \( I_D \) is sensitive to
  - Supply (Vdd)
  - Process (\( V_{Tn} \) and \( \mu_n C_{ox} W/L \))
  - Temperature (\( V_{Tn} \) and \( \mu_n \))
IC Biasing

• In IC design we often assume that we have **one** precise current source and we copy its value to our circuits
Simple Current Mirror

- That copy circuit is a current mirror
- Simple Current Mirror

\[ I_D = I_{\text{REF}} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_G - V_Tn)^2 \]

\[ V_G = \sqrt{\frac{2I_{\text{REF}}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1}} + V_{Tn} \]

- If \( V_G \) is applied to another transistor

\[ I_{\text{out}} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 \left(\sqrt{\frac{2I_{\text{REF}}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1}} + V_{Tn} - V_{Tn}\right)^2 \]

\[ I_{\text{out}} = \left(\frac{W}{L}\right)_2 I_{\text{REF}} \]
Ideal Current Mirror Example

- This bias scheme reduces sensitivity to process, voltage, and temperature variations.

\[ I_1 = 1 \text{mA} \]
\[ I_2 = 1 \text{mA} \]
\[ I_3 = 0.5 \text{mA} \]
\[ I_4 = 1.5 \text{mA} \]
What is $I_D$?

- Need to insure that M3 remains in saturation

$$V_s = V_G - (V_{ovl} + V_{Th}) = \left(\frac{R_{G2}}{R_{G1} + R_{G2}}\right)V_{dd} - \left(\frac{2I_D}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1} + V_{Th}\right)$$
Current Mirrors: Accuracy limitations

In general \((W/L)_2 = N(W/L)_1\), most probably \(V_{T1} \neq V_{T2}\), then

\[
I_{D2} = \frac{\mu_n C_{OX}}{2} \left( \frac{W}{L}_2 \right)^2 (V_{GS} - V_T)^2 (1 + \lambda_2 V_{DS2})
\]

\[
I_{D2} = \frac{\mu_n C_{OX}}{2} \left( \frac{W}{L}_2 \right)^2 (V_{GS} - V_{T2})^2 (1 + \lambda_2 V_{DS2})
\]

\[
I_{D1} = \frac{K_{P2} (V_{GS} - V_{T2})^2 (1 + \lambda_2 V_{DS2})}{K_{P1} (V_{GS} - V_{T1})^2 (1 + \lambda_1 V_{DS1})} I_{D1}
\]

\[
\lambda \propto \frac{1}{L}
\]

Long devices reduce the error; make \(V_{DS1} = V_{DS2}\)

Errors can be reduced (but not eliminated) by using replicas of the main device and good layout!

Effective mobility and threshold voltages are sensitive to \(V_{DS}\) and \(V_{dsat}\)

Good solution ==> use cascode structures

\[
\text{Error} \approx \lambda_2 V_{DS2} \neq \lambda_1 V_{DS1}
\]

\[
\text{Error} \approx K_{P2} \neq K_{P1}
\]

\[
\text{Error} \approx V_{T2} \neq V_{T1}
\]
DC Current Mirrors: Second-Order Effects

After good layout: Tolerances in N are in the range of 0.5-2 %. Usually mismatches are inversely proportional to gate area!

\[
\frac{I_{D2}}{I_{D1}} = \frac{\mu_n 2 (V_{GS} - V_{T2})^2 (1 + \lambda 2 V_{DS2})}{\mu_n 1 (V_{GS} - V_{T1})^2 (1 + \lambda 1 V_{DS1})} N
\]

Mobility degradation

Error \approx \mu_2 - \mu_1

Error is minimized by using replicas of the basic device

Intra-die \( V_T \) mismatches are inversely proportional to gate area!
Small-Signal Impedance: Simple Current Source

\[ r_{out} = \frac{1}{g_o} \]
Small-Signal Impedance: “Diode” Load

\[ r_{out} = \frac{1}{g_m + g_o} \approx \frac{1}{g_m} \]
Small-Signal Impedance:
Looking Into Source

\[ i_o = (g_m + g_{mb})v_o + \frac{v_o}{r_o} = (g_m + g_{mb} + g_o)v_o \]

\[ r_{out} = \frac{1}{g_m + g_{mb} + g_o} \approx \frac{1}{g_m} \]
Small-Signal Impedance: Looking Into Source w/ Drain Resistor

\[ r_{out} = \frac{1}{g_m + g_{mb} + g_o \left(1 + \frac{R_D}{r_o}\right)} \]
Small signal analysis: Common-source amplifier

Small signal equivalent

If \( V_{\text{OUT}} > V_{\text{DSAT1}} \), \( V_{\text{OUT}} < V_{\text{DD}} - V_{\text{SAT2}} \)

\[ A_v = -\frac{g_{m1}}{g_{01} + g_{02}} \]

Operating point

\( g_{m1}, g_{01}, \) and \( g_{02} \) are function of Q
Small signal analysis: Common-drain (source follower) amplifier

How this is done? Why?

\[ \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{mb} + g_{01} + g_{02}} \]
Small signal analysis: Common-gate amplifier (cascode)

\[ V_{\text{out}} = \frac{g_{m1} + g_{mb} + g_{01}}{g_{01} + g_{02}} \]

Impedance seen at Vin and Vout? Are they relevant?
Precise Current Mirrors: Cascode structure

Error \approx \lambda_2 V_{DS2} - \lambda_1 V_{DS1}

FUNDAMENTAL PRINCIPLE:

Error can be reduced if and only \( \lambda_2 = \lambda_1 \) and \( V_{DS2} = V_{DS1} \)

⇒ Transistors M1 and M2 are used as current mirrors

⇒ Transistors M3 and M4 are used to have \( V_{DS1} = V_{DS2} \).

⇒ L1 = L2 and \( ID1 = ID2 \Rightarrow \lambda_1 = \lambda_2 \)

⇒ If M1 = M2 then \( \mu_1 = \mu_2 \), and \( VT1 = VT2 \)
Output impedance: Cascode structure

Output impedance

\[ Z_{out} = \frac{v_{02}}{i_{d2}} \]

\[ i_{d2} = (v_{02} - v_{s4})g_{04} - g_{m4}v_{s4} \]

\[ Z_{out} = r_{02} + r_{04} + g_{m4} r_{02} r_{04} \]

Notice that most of the AC current re-circulate within the cascode device and only \( i_{d2} \) is extracted from \( v_{02} \) !!

Compare \( g_{m4} \) with \( g_{02} \)!
Comparison of current sources: output impedance and headroom

\[ r_{\text{out}} = r_{02} \]

\[ V_0 > V_{\text{DSAT2}} \]

\[ V_0 > V_{\text{GS1}} + V_{\text{DSAT4}} = V_{T1} + V_{\text{DSAT1}} + V_{\text{DSAT4}} \]

\(~ 100-400 \text{ mV}~

\(~ 0.9-1.5 \text{ V!}~

\(~ 100-400 \text{ mV}~

\(~ 1 - 1.5 \text{ V!}~\)
Double Cascode Structure: Advantages and drawbacks!

Small signal output resistance:

\[ r_{out} \approx g_m (r_{eq31})r_{04} \approx g_m (g_{m3} r_{02} r_{03}) r_{04} \]

\[ V_0 > V_{DS2} + V_{DSAT3} + V_{DSAT4} \]

Output resistance is increased

Voltage swing is reduced

Parasitic poles could be an issue

Usually this section is more complex to ensure VDS is similar in both transistors M1 and M2

How VG3 and VG4 can be generated????
Voltage references (biasing cascode structures)

Let's consider the case: \( V_{DS2} = V_{DSAT2} \)

\[ V_{G3} \text{ must be } V_{GS3} + V_{DSAT2} = V_{T3} + V_{DSAT3} + V_{DSAT2} \]

\[ V_{GSR} = V_{TR} + \frac{2}{\mu_n C_{OX}} \frac{L_R}{W_R} I_{D1} \]

**Increasing L/W by 4, VDSAT increases by 2**

According to \((W/L)_1\), the gate dimensions for MR \((W/L)_R\) must be designed

Problem: \( V_{TR} \neq V_{T3} \) due to body effect
Partial solution: \((W/L)_1 > 4(W/L)_R \Rightarrow 9(W/L)_R\)
Improved (self regulated) current source

\[ r_{out} \approx g_{m4}(1 + A_v)r_{02}r_{04} \]

Similar to double cascode

Key issue: Please understand the concept!!
Other current sources

Wilson Current Source

\[ r_{out} \approx g_m \left( 1 + A_v \right) \left( r_{eq} \right) r_{04} \]

"\( r_{eq} \)" = \( \frac{1}{g_m} \)

Output resistance similar to cascode

M1, M3 in triode region
M2, M4 are saturated

\[ r_{out} = ?? \]

\[ V_{out,\min} = ?? \]
Other current sources

\[ i_D = \mu C_{OX} \frac{W}{L_{eff}} \left[ V_{GS} - V_T - 0.5 V_{DS} \right] V_{DS} \]

\[ r_{ds 3} = \frac{L_{eff}}{\mu C_{OX} W \left[ V_{GS 3} - V_T - V_{DS 3} \right]} \]

\[ r_{out} \approx g_m 4 r_{04} \left( r_{ds 3} \right) \approx \]

\[ V_0 > V_{DS 3} + V_{DSAT 4} \]

\[ r_{out} \approx g_m 4 r_{04} \left( \sum r_{dsi} \right) \]
Low-Voltage Cascode Current Mirror

- M2 and M4 should be sized such that
  - \( V_{GS2} = V_{GS4} \)
- M1 and M3 biased near edge of saturation
  - \( V_{DS1} \approx V_{DS3} \approx V_{DSAT} \)
  - \( V_b = V_{GS2} + (V_{GS1} - V_{T1}) = V_{GS4} + (V_{GS3} - V_{T3}) \)

- Improved \( V_b \) generation circuit
  - M5 sized such that \( V_{GS5} \approx V_{GS2} \)
  - Some body effect error here
  - Size M6 and \( R_b \) such that
    - \( V_{DS6} = V_{GS6} - R_b I_1 \approx V_{GS1} - V_{T1} \)
Next Time

• Single-Stage Amplifiers