ECEN 326
Fall 2017 Lab Policy

Section 501: TH 8AM – 10:50AM (CVLB 423)
Section 502: TH 11:10AM - 2PM (CVLB 423)

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Office: WERC 015F
Office Hours: T 10AM – 12PM
Email: hwyang@tamu.edu

Grading:
  Pre-labs 40%
    • One report per person
    • SPICE simulation verification takes 50% of the Pre-lab grade
    • Due at the beginning of the lab. Pre-lab will be quickly reviewed by TA as the lab starts.
    • No late pre-labs will be accepted without a valid excuse (24 hrs in advance)

  Lab Reports 50%
    • One report per group/person
    • Double-side printing is highly recommended
    • Due at the beginning of the following lab sessions. For late submission, there will be deduction of -0.5dB/hr from full credit.

  Lab Performance 10%
    • Punctuality - Lab experiments get started and finished on time
    • Violation of the Safety Rules such as bringing in food/drink in the lab is NOT taken lightly

Policies
  • Pre-labs may be hand written but they need to be legible and understandable.
  • Pre-labs must be:
    ➢ Clean sheet of paper (do not use paper that has been previously used for printing unrelated text)
    ➢ Clear handwriting (consider typing the text part of your pre-labs)
    ➢ Follow the same components labeling as in the lab manual
    ➢ Numbered equations
    ➢ Boxed final results
  • Reports must be TYPED, please do not cut-and-paste from the lab manual. Make sure all plots/schematics have white background by inverting colors if necessary. If the grader cannot read scale from result or circuit diagram. The figure will be invalidated.
  • Plots/Pictures need to have captions, axis names, and annotations if needed.
  • No food or drink in the lab
<table>
<thead>
<tr>
<th>Lab No.</th>
<th>Lab Time</th>
<th>Report Due</th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Sep 14, TH 8AM-10:50AM&lt;br&gt;Sep 14, TH 11:10AM-2PM</td>
<td>Beginning of next lab</td>
<td>Design of a Common-Emitter BJT Amplifier</td>
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<td>2</td>
<td>Sep 21, TH 8AM-10:50AM&lt;br&gt;Sep 21, TH 11:10AM-2PM</td>
<td>Beginning of next lab</td>
<td>Design of a Three-Stage BJT Amplifier</td>
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<td>3</td>
<td>Sep 28, TH 8AM-10:50AM&lt;br&gt;Sep 28, TH 11:10AM-2PM</td>
<td>Beginning of next lab</td>
<td>Design of a Common-Source MOSFET Amplifier with a Source Follower</td>
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<td>4</td>
<td>Oct 5, TH 8AM-10:50AM&lt;br&gt;Oct 5, TH 11:10AM-2PM</td>
<td>Beginning of next lab</td>
<td>Design of a BJT Differential Amplifier</td>
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<td>5</td>
<td>Oct 12, TH 8AM-10:50AM&lt;br&gt;Oct 12, TH 11:10AM-2PM</td>
<td>Beginning of next lab</td>
<td>Design of a MOS Differential Amplifier</td>
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<td>6</td>
<td>Oct 19, TH 8AM-10:50AM&lt;br&gt;Oct 19, TH 11:10AM-2PM</td>
<td>Beginning of next lab</td>
<td>Design of Current Mirrors</td>
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<td>7</td>
<td>Oct 26, TH 8AM-10:50AM&lt;br&gt;Oct 26, TH 11:10AM-2PM</td>
<td>Beginning of next lab</td>
<td>Design of a BJT Operational Transconductance Amplifier</td>
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<td>8</td>
<td>Nov 2, TH 8AM-10:50AM&lt;br&gt;Nov 2, TH 11:10AM-2PM</td>
<td>Beginning of next lab</td>
<td>Frequency Response of a Common-Emitter BJT Amplifier</td>
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<tr>
<td>9</td>
<td>Nov 9, TH 8AM-10:50AM&lt;br&gt;Nov 9, TH 11:10AM-2PM</td>
<td>Beginning of next lab</td>
<td>Frequency Response of a Cascode BJT Amplifier</td>
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<tr>
<td>10</td>
<td>Nov 16, TH 8AM-10:50AM&lt;br&gt;Nov 16, TH 11:10AM-2PM</td>
<td>Beginning of next lab</td>
<td>Design of a BJT Shunt-Series Feedback Amplifier</td>
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<tr>
<td>11</td>
<td>Nov 30, TH 8AM-10:50AM&lt;br&gt;Nov 30, TH 11:10AM-2PM</td>
<td>By Dec 7 @ TA’s office</td>
<td>Design of a Two-Stage Amplifier with Miller Compensation (Extra credit)</td>
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