A Millimeter-Wave (23–32 GHz) Wideband BiCMOS Low-Noise Amplifier

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Abstract—This paper presents a 23–32 GHz wideband BiCMOS low-noise amplifier (LNA). The LNA utilizes coupled-resonators to provide a wideband load. To our knowledge, the proposed LNA achieves the widest bandwidth with minimum power consumption using 0.18 μm BiCMOS technology in K-band. Analytical expressions for the wideband input matching, gain, noise figure and linearity are presented. The LNA is implemented using 0.18 μm BiCMOS technology and occupies an area of 0.25 mm². It achieves a voltage gain of 12 dB, 3-dB bandwidth of 9 GHz, noise figure between 4.5–6.3 dB, linearity higher than −6.4 dBm with a power consumption of 13 mW from a 1.5 V supply.

Index Terms—BiCMOS, coupled-resonators, low-noise amplifier, millimeter-wave, wideband.

I. INTRODUCTION

The growing demand for high data rate wireless communications is one of the main drivers of the semiconductor industry. For example, receivers that target the wireless metropolitan area network standard (IEEE-802.16) for the 10–66 GHz frequency range and the ultra-wideband radar for 22–29 GHz are necessary to address this growing demand [1]. Expensive GaAs-based MMICs have been commonly used for implementing front-ends at these frequencies. Implementing low-cost silicon-based integrated circuits is a challenging problem due to low quality factor of passive components, the coupling between various elements, parasitics that limit the frequency of operation, and high noise figure and power consumption at millimeter-wave (mm-wave) frequencies. Wideband circuit architectures are also an important challenge at these frequencies. Hence, novel circuit ideas need to be developed to overcome all these limitations.

Wideband low-noise amplifiers (LNAs) using silicon were implemented for low-GHz frequencies [2]. For frequencies above 20 GHz (for example K-band within 20–40 GHz), the parasitics limit the wideband operation and increase the overall noise figure of the LNA. In addition, the low cut-off frequency ($f_T$) of the active devices on silicon limits the upper operating frequency. Also, passive components and interconnections between various devices and building blocks must be individually modeled using electromagnetic simulators to take into account all parasitic effects and achieve the targeted specification after fabrication. All of the above limitations make the design of a wideband LNA within K-band challenging: especially using silicon-based technologies with lower $f_T$, and hence higher power consumption is a necessity.

Several silicon-based narrowband LNA architectures have been shown in the literature within K-band [3]–[11]. A common-gate LNA, operating at 24 GHz, with resistive feedthrough is proposed using 0.18 μm CMOS technology in [3]. This architecture utilizes an inductor and resistor between the drain and source of the input device to reduce the effect of parasitics and noise figure of the common gate topology. The inductor makes this topology narrowband and a 6 dB noise figure is obtained. Utilizing spiral or transmission line-based inductors for the commonly used narrowband inductively degenerated cascode LNA is another approach implemented in [4]–[6]. All the techniques in [3]–[6] rely on resonance-based loads for narrowband operation, which is not suitable for the targeted wideband operation. Another narrowband technique is to utilize stub matching using transmission lines for input and output matching [7]. Stub matching technique also consumes larger area compared to lumped element matching. As can be seen, most of the presented techniques on silicon are suitable for narrowband operation within K-band.

A wideband LNA for the frequency range of 18–26 GHz was reported using 0.13 μm CMOS technology in [8]. The wideband operation is achieved by utilizing a wideband input matching circuit. Wideband interstage matching was also used to provide the wideband load. Extending this approach to higher frequencies using the same technology may not be suitable because the parasitic capacitance of the second stage has to be decreased which results in reducing the overall gain. The same technique is applied using an advanced 0.13 μm SiGe:C HBT BiCMOS technology to increase the operating frequency and bandwidth [9]. Recently, a wideband LNA for 21–27 GHz using 0.18 μm CMOS technology was reported in [10]. The wideband response is achieved using inductive peaking techniques in the load to extend the bandwidth. For higher bandwidths, the value of the load resistance has to be decreased, and the gain is lowered. For higher gain and bandwidth, the number of stages and the power consumption have to be increased. Employing a third-order Cauer BPF for input matching along with shunt peaking as the load is another technique introduced in [11]. This technique demonstrates a gain of 18 dB for 22–29 GHz operating bandwidth. This survey shows that there is a tradeoff between the bandwidth (BW), gain ($G$) and power consumption ($P$) of the amplifier.

In this paper, a wideband LNA with coupled-resonators as wideband loads is presented for 23–32 GHz frequency range using 0.18 μm SiGe BiCMOS technology ($f_{T,BiCMOS}$/$f_{max,BiCMOS}$ =...
The proposed wideband mm-wave LNA architecture is shown in Fig. 1. In this architecture, a wideband input matching network is designed using inductors $L_e$ and $L_b$. The input matching network is similar to the one employed in narrowband approach at low-GHz range [12]; however as demonstrated later, the same components can be used for wideband matching at mm-wave frequencies using BiCMOS technology. The wideband gain is obtained using a proposed coupled-resonator as the load of each amplifier stage. Coupled-resonators can result in two peaks depending on their coupling coefficient. Cascading two of these coupled-resonators, with unequal peaking frequencies, results in a wideband response as discussed later. Two gain stages with two different coupled-resonator loads are implemented to provide the wideband response for the proposed LNA. In addition, these two stages increase the voltage gain across the desired wideband frequency range. Finally, the noise due to the cascode transistor is reduced by adding the inductor $L_m$ to resonate with the parasitic capacitance at the emitter of $Q_2$, $c_{pm}$ [13]–[15]. Hence, the emitter of $Q_2$ is degenerated with a high impedance, and the noise current of $Q_2$ is not injected to the output of the first stage. Instead, the noise current circulates within $Q_2$. All the above techniques enable the design of an LNA with a larger BW and higher gain, low wideband input-referred noise and low power consumption.

### II. THE PROPOSED LNA ARCHITECTURE

The proposed wideband LNA architecture is shown in Fig. 1. The schematic of the proposed wideband mm-wave LNA is shown in Fig. 1.

![Fig. 1. The schematic of the proposed wideband mm-wave LNA.](image)

The proposed approach enables increasing the gain and bandwidth of the amplifier compared to the ones reported in [8]–[11], while minimizing the power consumption (higher $G \cdot BW/P$). In addition, a noise reduction technique is employed for the LNA cascode transistor at the first stage to reduce the overall noise figure by resonating out the effect of the parasitic capacitance at the source of the cascode transistor for a wide frequency range. The LNA is targeted for multi-band mm-wave receivers using IEEE802.16 wireless standard working in the 23–32 GHz frequency range. Also, it can be used for 22–29 GHz UWB short-range radars. The paper is organized as follows: Section II demonstrates the basic circuit architecture. Section III discusses the design and implementation of lumped and transmission line based inductors, and Section IV shows simulation and measurement results.

#### A. Input Matching Network

The input matching network consists of the pad, inductors $L_e$ and $L_b$, and the base-emitter capacitance, $c_{be}$, of $Q_1$. The input matching network is similar to the narrowband one at low-GHz frequencies. However, due to operation within K-band, it has a lower quality factor suitable for wideband matching at this frequency range. This effect is investigated using schematic-level simulations by only changing the inductance value of $L_b$ using Spectre. The simulated return loss of the matching network in Fig. 1 for different values of $L_b$ is demonstrated in Fig. 2, where a sharper bandwidth is demonstrated for lower inductance values of $L_b$ using Spectre.

![Fig. 2. Simulated input return loss of the matching network in Fig. 1 for different values of $L_b$.](image)

1Spectre 6.2, Cadence 2008.
The equivalent circuit model of the wideband input matching network at the base of $Q_1$ is shown in Fig. 3, where the resistance $R_q$ is equal to $\omega T \cdot L_e$. The transistor $Q_1$ is sized such that $C_{\text{in}}$ and $L_e$ resonate at the midband of interest. $C_{\text{pad}}$ and $C_p$ are the capacitances due to the pad and miller reflected base-collector capacitance of $Q_1$, respectively. The emulated resistance $R_q$ provides the required 50 $\Omega$ input matching without increasing the overall NF. The wideband operation of the input matching network is explained by dividing it into two sections. The first section, consisting of $L_e$, $C_{\text{in}}$, and $R_q$, forms a very low-Q ($Q < 1$) series $RLC$ resonant circuit because of the large base-emitter capacitance of $Q_1$ and the operation at 23–32 GHz frequency range ($Q = (1)/(\omega C_{\text{in}} R_q)$). Inductors $L_e$ and $L_b$ should have high-$Q$ to keep the overall NF low. Fig. 4 shows the simulated return loss of the first section. As depicted, matching better than $-15$ dB is achievable using $L_e$, $C_{\text{in}}$, and $R_q$ across the band of interest. However without $L_b$, the parasitic capacitance $C_p + C_{\text{pad}}$ changes the effective input impedance considerably, and poor matching is achieved as shown in Fig. 4. Finally, the inductor $L_b$ recovers the matching by forming a low-Q pi-matching network with capacitors $C_d$ and $C_{\text{pad}}$ as shown in Fig. 3. The low quality factor of pi-matching network is because of the 50 $\Omega$ impedance seen at $Z_{\text{in,1}}$ and the operation within K-band.

The input impedance of the proposed LNA is then approximated by

$$Z_{\text{in}}(s) \approx \frac{1 + sR_qC_{\text{in}} + s^2(L_e + L_b)C_{\text{in}} + s^3R_qL_bC_{\text{in}}C_p}{sC_T(1 + s\frac{C_p}{C_T} R_q C_b + s^2\frac{C_p}{C_T^2}(L_e C_p + L_b C_{\text{pad}}))}$$

$$C_b = C_p + C_{\text{pad}}$$

$$C_T = C_p + C_{\text{pad}} + C_{\text{in}}.$$  (1)

For the low-GHz case, the coefficients of $s^2$ and higher are neglected. However at mm-wave frequencies, these coefficients are comparable to the first-order term, and cannot be neglected. Equation (1) also shows that $L_b$ increases the magnitude of $s^2$ and $s^3$ coefficients in the numerator, therefore, zeros are moved to a lower frequency to cancel the effect of poles allowing wider input matching bandwidth. This effect along with the lower quality factor enables the design of a wideband input matching network.

**B. Wideband Load**

The wideband load is achieved using coupled-resonator structure, shown in Fig. 5(a). The input impedance of the coupled-resonator, $Z_{\text{load}}$, is found by considering the equivalent circuit model shown in Fig. 5(b). Assuming a tank circuit with high quality factor and resonators with similar component values, the input impedance, $Z_{\text{load}}$, is approximated as follows [16]:

$$Z_{\text{load}}(\omega) \approx \frac{N(\omega)}{D(\omega)}$$

$$N(\omega) = \left\{1 - 2 \left(\frac{\omega}{\omega_0}\right)^2\right\} + j \left\{Q_{\text{ld}} \left(\frac{\omega}{\omega_0}\right) \left(1 - (1 - k_d^2) \left(\frac{\omega}{\omega_0}\right)^2\right)\right\}$$

$$D(\omega) = \left\{1 - \left(\frac{\omega}{\omega_0}\right)^2\right\} - \frac{(\omega/\omega_0)^2}{Q_{\text{ld}}^2} - k_d^2 \left(\frac{\omega}{\omega_0}\right)^4 - j \left\{\frac{2(\omega/\omega_0)}{Q_{\text{ld}}} \left(1 - \left(\frac{\omega}{\omega_0}\right)^2\right)\right\}.$$  (2)

where $k_d$ is the coupling coefficient between two resonators, $\omega_0$ is the resonant frequency of a single resonator defined as $\omega_0 = $
1/\sqrt{L_0 C_d}$, and $Q_{LD}$ is the quality factor of a single tank circuit defined as $Q_{LD} = (\omega_0 Q_{LD})/(R_{LD})$. Equation (2) shows that the load impedance has two peaks as demonstrated by Fig. 6(a). These two peaks are found by solving $\text{Im}((1)/(Z_{\text{load}})) = 0$ for the parallel resonant circuit, and are located at

$$\frac{\omega_{HL}}{\omega_0} = \sqrt{1 \pm k_d}. \quad (3)$$

Hence, the two peak frequencies are separated by

$$\Delta \omega_{HL} = (\sqrt{1 + k_d} - \sqrt{1 - k_d})\omega_0 \approx k_d \omega_0. \quad (4)$$

The approximation in (4) is valid for a wide range of $k_d$ (for $k_d \leq 0.7$ the error in $\Delta \omega_{HL}$ calculation is less than 5%). The resonator impedance values at peak frequencies, $\omega_L$ and $\omega_H$, are given by

$$Z_{\text{load}}(\omega_{HL}) = R_{LD}Q_{LD}\frac{(k_d^2 + k_d - 1)^2(1 + k_d)}{k_d^2 + 2k_d + 2}. \quad (5)$$

Equation (5) shows that the impedance at the high peak frequency, $\omega_H$, is lower than the one at $\omega_L$ as demonstrated in Fig. 6(a). Dual-band and wideband loads can be obtained using the coupled-resonator circuit architecture as shown in Fig. 6. Using a single coupled-resonator, the two peak frequencies could be adjusted to resonate at the targeted frequencies leading to dual-band response. On the other hand, wideband operation is achieved by cascading two coupled-resonators as demonstrated in Fig. 6(b). The two coupled-resonators are tuned at two different center frequencies ($\omega_{c1}$ and $\omega_{c2}$) to provide the required wideband operation.

To minimize the in-band ripples, the maximum to minimum in-band load variations should be reduced. The minimum in-band load of a single coupled-resonator is found by evaluating (2) at $\omega = \omega_0$ yielding

$$|Z_{\text{load}}(\omega_0)| = \frac{R_{LD}Q_{LD}^2}{1 + k_d^2 Q_{LD}^2}. \quad (6)$$

Therefore, the maximum to minimum overall gain variations across the band is found from (5) and (6) as follows

$$\frac{|Z_{\text{load}}(\omega_L)|}{|Z_{\text{load}}(\omega_0)|} \approx \frac{(k_d^2 + k_d - 1)^2(1 + k_d)}{k_d^2 + 2k_d + 2} \cdot (1 + k_d^2 Q_{LD}^2). \quad (7)$$

Typically, $|Z_{\text{load}}(\omega_0)|/|Z_{\text{load}}(\omega_L)|$ should be limited to a value lower than 6 dB to reduce the ripples. For a specific value of the coupling coefficient, the maximum variation imposes an upper value for the quality factor as depicted by (7). Increasing $Q_{LD}$ increases the maximum to minimum load variations as demonstrated in Fig. 7 using circuit-level simulations. For $k_d = 0.19$, $Q_{LD}$ should be lower than 8 to reduce the variations. It is important to note that increasing $k_d$ places the two resonant frequencies further apart, however lower value of $Q_{LD}$ (lower gain) is necessary to reduce the in-band variations. Therefore, there is a trade-off between flat bandwidth extension and overall gain of the amplifier. As an example, increasing $k_d$ by 50% increases the bandwidth by the same amount (according to (4)), however this increase requires reducing $Q_{LD}$ to 5, hence reducing the gain by almost 50%.

Fig. 8 demonstrates the simulated gain of two cascaded amplifiers with coupled-resonator loads shown in Fig. 1. The total gain, $G_T$, of the cascaded amplifier is given by

$$G_T = (G_{\text{eff},1} Z_{\text{load},1}) \cdot (G_{\text{eff},2} Z_{\text{load},2}) \quad (8)$$

where $G_{\text{eff},1}$ and $G_{\text{eff},2}$ are the effective transconductance of each gain stage. In this simulation, a coupling coefficient of 0.19 is assumed to cover the required band. The first and second coupled-resonators are designed with $\omega_{c1}$, $\omega_{c2}$ of 26 and 28 GHz, respectively. The two center frequencies are selected such that the overall response leads to the desired wideband response to cover the 23–32 GHz frequency band. As discussed earlier, the
in-band ripples are reduced by selecting $Q_{Ld}$ to be lower than 8. In addition, $G_{\text{eff,1}}$ smoothens the gain through the inductor $L_m$ in Fig. 1. Inductor $L_m$ forms a wideband parallel RLC resonant circuit with its peak frequency adjusted at the highest operating frequency. This resonant circuit boosts the gain at higher frequencies, leading to a spectrally wideband gain.

C. Noise Analysis

The total input-referred noise of the proposed LNA is mainly dominated by the first stage according to Friis equation [17]. As a result, it is assumed that the overall noise figure is mainly due to the first stage in the following analysis. Fig. 9 shows the equivalent noise circuit of the first amplifier stage. The base and collector noise currents of $Q_1$, noise due to parasitic base resistances of $Q_1$, $R_b$, and noise due to losses of $L_b$, $R_{lb}$, and $L_e$, $R_{le}$, are considered in this equivalent model. The noise due to the cascode transistor, $Q_2$, is considerably reduced by adding the inductor $L_m$, and as a result, it can be neglected in the following analysis.

1) Noise of $Q_1$: The equivalent input-referred noise due to the base and collector noise currents of $Q_1$ are given by (9) and (10), shown at the bottom of the page, where $R_n$ is the source resistance, $g_m$ is the transconductance of $Q_1$, and $v_{n,b}$ and $v_{n,c}$ are the base and collector noise currents of $Q_1$, and are given by

$$v_{n,b}^2 = 2qI_{B1}$$

$$v_{n,c}^2 = 2qI_{C1}$$

where $q$ is the electron charge constant, $I_{B1}$ is the constant base current, and $I_{C1}$ is the collector current of $Q_1$.

Higher order coefficients of $s$ are not neglected in (9) and (10) because these terms are effective across the band of interest. Equations (9) and (10) show that the input-referred noise of $Q_1$ increases proportionally with the value of $L_b$ at higher frequencies. This is because the voltage gain between the input and the base-emitter junction of $Q_1$ is inversely proportional to $I_b$. Due to the matching requirements, shown in (1), $I_b$ cannot be set to zero to lower the noise. Therefore, there is a tradeoff between the input matching and noise figure for this amplifier. In this design, $I_b$ is selected such that the input return loss is better than $-12$ dB across the band of interest.

The total input-referred noise voltage due to $Q_1$, $v_{n,1 Q_1}^2$, is given by adding the two expressions in (9) and (10). The resultant total input-referred noise normalized to the noise voltage of the source resistance can be approximated by

$$\frac{v_{n,1 Q_1}^2}{4kTR_n f} \approx \frac{\eta_1(\omega)}{g_{m1}} + \frac{\eta_2(\omega)g_{m1}}{2R_s}$$

\[
\eta_1(\omega) = \frac{1 - \left(\frac{\omega}{\omega_1}\right)^2 + j\frac{\omega}{\omega_1} \left(1 - \left(\frac{\omega}{\omega_1}\right)^2\right)}{2R_s}
\]

\[
\eta_2(\omega) = \frac{1 - \left(\frac{\omega}{\omega_2}\right)^2 + j\frac{\omega}{\omega_2} \left(1 - \left(\frac{\omega}{\omega_2}\right)^2\right) (R_s + R_b)^2}{2\beta R_s}
\]

\[
\omega_1 = \sqrt{\frac{1}{(c_{oc} + c_{ce})(L_b + L_e + R_s R_b C_{pad})}}
\]

\[
\omega_2 = \sqrt{\frac{R_s + R_b}{C_{pad} (L_b + L_e) R_s}}
\]

\[
\omega_3 = \sqrt{\frac{1}{(c_{oc} + c_{ce} + C_{pad})(R_s + R_b)}}
\]

\[
\omega_4 = \sqrt{\frac{R_s + R_b}{L_e + L_b + R_s R_b C_{pad}}}.
\]

where $k$ is Boltzmann constant, $T$ is the temperature in kelvin, $\omega$ is the operating frequency in radian/s, and $\beta$ is the current gain of BJT. Equation (13) shows that the total input-referred noise voltage due to the collector noise current can be decreased by increasing the value of $g_{m1}$. However, increasing $g_{m1}$ increases the contribution of the base noise current. Hence, there is an optimum value for $g_{m1}$ to minimize the total input-referred noise due to $Q_1$. By differentiating (13) with respect to $g_{m1}$ and equating the resultant expression to zero, $g_{m1,\text{opt}}$ is given by

$$g_{m1,\text{opt}} = \sqrt{\frac{\eta_1(\omega)}{\eta_2(\omega)}}$$

The minimum input-referred noise voltage due to $Q_1$ is then as follows:

$$\frac{v_{n,1 Q_1}^2}{4kTR_n f} \mid_{\text{min}} = 2\sqrt{\eta_1(\omega)\eta_2(\omega)}$$
Fig. 9. Main noise sources of the proposed wideband LNA.

Eq. (14) shows that $g_{m1,\text{opt}}$ depends on the operating frequency because $\eta_1$ and $\eta_2$ are both frequency dependent. Fig. 10 shows the value of $g_{m1,\text{opt}}$ versus the operating frequency. As depicted, $g_{m1,\text{opt}}$ varies from 0.4–0.5 S for 23–32 GHz frequency range, which means that $g_{m1,\text{opt}}$ does not vary significantly across the band of interest.

The input-referred noise voltage due to $Q_1$, defined in (13), is drawn versus $g_{m1}$ in Fig. 11. At $g_{m1,\text{opt}} \approx 0.45$ S the noise voltage is minimum, as given by (15). In addition, the noise voltage slightly changes from a transconductance value of 0.15 S when compared to the optimum value at 0.45 S. Choosing a value for $g_{m1}$ lower than optimum reduces the power consumption with a slight increase in the input-referred noise voltage due to $Q_1$. In this design, $g_{m1}$ is selected to be 0.18 S to reduce the power consumption of the LNA.

2) Noise of Cascode Transistor: At low GHz frequencies the noise contribution of the cascode transistor, $Q_2$, is neglected because of the high degeneration resistance at the emitter of $Q_2$. However at mm-wave frequencies, the parasitic capacitance at the emitter of $Q_2$ reduces the degeneration impedance. As a result, most of the noise due to $Q_2$ appears at the output of the first stage and increases the overall noise figure (NF). To overcome this problem, the inductor, $L_m$, is added to resonate with the parasitic capacitance to increase the degeneration impedance of $Q_2$ [13]–[15]. As a result, the noise of $Q_2$ does not appear at the output of the first stage.

Also, the current source, consisting of $M_{p2}$ in Fig. 1, is added to control the quality factor of the tank circuit ($L_m$ and parasitic capacitance) to provide a wideband noise reduction of $Q_2$ at mm-wave frequencies. The quality factor is adjusted by changing the current passing through $Q_2$, and hence its transconductance, $g_{m2}$. The resonant frequency and quality factor of this tank circuit are adjusted to be 29 GHz and 3, respectively, to cover the entire bandwidth.

3) Overall Noise Figure: The total noise figure, $\text{NF}_{\text{tot}}$, of the proposed LNA is mainly due to the noise of the first stage as discussed earlier in this section, and is given by

$$\text{NF}_{\text{tot}}(\omega) = 1 + \frac{R_{Lb}}{R_b} (1 + \omega^2 C_{\text{pad}} R_b) + \frac{\eta_1(\omega)}{g_{m1}} + \eta_2(\omega) g_{m1}$$

Equation (16) shows that the input-referred noise of the base resistance of $Q_1$, $R_b$, and loss resistance of $L_b$, $R_{Lb}$, increase...
as the frequency increases due to the presence of the pad capacitance, $C_{pad}$. This capacitance produces a pole at the input of the LNA and increases the noise contributed by $R_b$ and $R_{Lb}$ at higher frequencies, as shown in (16). In this design, the pole ($1/C_{pad}R_b$) exists around 31 GHz, which increases the input-referred noise due to $R_b$ and $R_{Lb}$ by 3 dB at 31 GHz. It is difficult to increase this pole because the source resistance is fixed and pad size is limited by the minimum size provided by the technology. Equation (16) also demonstrates that $NF_{tot}$ increases with increasing the value of $I_b$ as well as $R_{Lb}$, therefore $L_b$ cannot be increased freely to provide better matching.

### D. Linearity Analysis

According to Friis equation [17], the input-referred third-order intercept point (IP3) of the wideband LNA is defined as follows:

$$\frac{1}{IP3_{3,tot}} = \frac{1}{IP3_{3,1}} = \frac{G_1}{IP3_{3,2}}.$$  \hspace{1cm} (17)

where $G_1$ is the gain of the first stage, and IP3$_{3,tot}$, IP3$_{3,1}$, and IP3$_{3,2}$ are the total, first, and second stage input-referred third-order intercept point, respectively. For cascaded amplifiers, IP3$_{3,tot}$ is mainly determined by the last stage. However in the proposed LNA, the first stage is implemented using a bipolar transistor (BJT), while the second stage is implemented using MOS transistor. The linearity of the MOS transistor is higher than the BJT, and therefore, the linearity is determined by both stages. This is demonstrated by noting that the linearity of the first stage is around $-2$ dBm, and it provides a maximum gain of ($G_1 = 9$ dB). The linearity of the second stage is higher than 7 dBm. Hence, the second term in (17) is comparable to the first term, and therefore the linearity of both stages is considered. In case of replacing the MOS transistor with a BJT one, IP3$_{3,tot}$ will be reduced.

### E. Design for Stability

Stability is one of the important design targets at mm-wave frequencies. For a single transistor the feedback gate-drain capacitance may lead to instability for the case of having a tank circuit at the input and output of the amplifier. The first stage of the LNA is implemented using a cascode architecture to solve this problem [18]. However, a common source configuration is used for the second stage, which may lead to instability if not carefully designed. Stability puts an upper limit for the gain to avoid the unnecessary oscillations. Fig. 12 shows the equivalent circuit used for studying the stability, where $v_{inL}$ and $v_{outL}$ are the input and output voltages of the loop, and $Z_{d1}$ and $Z_{d2}$ are the coupled resonators of the first and second stage, respectively. The loop gain, $G_L$, for this architecture is given by

$$G_L = \frac{v_{outL}}{v_{inL}} = -\frac{1}{Z_{d1}} + \frac{1}{Z_{d2}} + \frac{Z_{gdl}}{Z_{d1}Z_{d2}}.$$ \hspace{1cm} (18)

where $g_{m,N1}$ is the transconductance of MOS transistor, and $Z_{gdl}$ is the impedance of gate-drain capacitance, $c_{gd,N1}$ of MOS transistor. The condition at which the oscillation may happen is obtained by placing the imaginary part in (18) to zero, i.e.,

$$Im\left\{\frac{1}{Z_{d1}} + \frac{1}{Z_{d2}} + \frac{Z_{gdl}}{Z_{d1}Z_{d2}}\right\} = 0.$$ \hspace{1cm} (19)

Equation (19) gives the frequency at which the oscillation may happen. Based on circuit-level simulations, the oscillation may occur at a frequency around 18 GHz in this design. To guarantee that the oscillation will not start, the loop gain has to be lower than one at this frequency, hence placing an upper limit for the value of $g_{m,N1}$ in (18). Fig. 13 shows the loop gain versus the value of $g_{m,N1}$ at the unstable frequency. In this simulation, it is assumed that $c_{gd,N1}$ scales proportionally with $g_{m,N1}$. As depicted, for values of $g_{m,N1}$ lower than 50 mS the second stage is stable. In this design, $g_{m,N1}$ is selected to be 20 mS to reduce the input capacitance of $M_{N1}$, and therefore the second stage provides a peak gain of 5 dB at the lower peak frequency of the coupled resonator.

![Fig. 12. Equivalent model of the second stage demonstrating the input/output tuned loads.](image)

![Fig. 13. Loop gain, $G_L$, versus $g_{m,N1}$ at the resonance frequency of tuned input/output second stage in Fig. 12.](image)
III. INDUCTOR LAYOUT

The performance of the mm-wave integrated circuits mainly depends on the parasitics of routing paths and the quality factor of the passive components. Poor quality factor and the parasitic inductance introduced by routing paths can greatly limit the performance. An electromagnetic simulator, SONNET,\(^2\) is used to model the various non-ideal passive effects. Inductors \(L_b\) and \(L_{cr}\) are implemented using microstrip transmission line (MTL) structures, while the coupled inductor \(L_d\) is implemented using a center-tapped differential inductor. The inductor \(L_m\) is implemented using the conventional spiral inductor structures. All the inductors are realized with the top metal layer which is the thickest metal layer and farthest from the substrate to reduce losses.

Microstrip structures are used for \(L_b\) (and \(L_{cr}\)) implementation, as shown in Fig. 14(a), because they are characterized by their high quality factor compared to the normal spiral inductors. Higher quality factor reduces the noise introduced by the input matching network. The width of the transmission line is increased to reduce the loss of the inductor. The self resonant frequency of the inductor limits the width of the MTL structure. Electromagnetic simulations using SONNET show that a line width of 20 \(\mu m\) increases the NF only by 0.2–0.3 dB compared to a lossless line while providing maximum quality factor in the band of interest. Fig. 14(b) shows the simulated inductance and quality factor of the designed MTL inductor \(L_b\). An inductance of 160 pH with a quality factor higher than 28 is obtained within the desired frequency band.

The coupled inductors, \(L_d\), is implemented using a center-tapped differential inductor as shown in Fig. 15(a). The line width and spacing between the two inductors are optimized to achieve a coupling coefficient of 0.19. According to (4) this coupling coefficient separates the two peak frequencies of each load by 4.9 and 5.3 GHz for a center frequency of 26 and 28 GHz, respectively. Hence, the resultant 3-dB bandwidth is around 9 GHz. The simulated inductance value and coupling coefficient for the coupled inductor are shown in Fig. 15(b). Both values are almost constant along the frequency band of interest. This is because the self resonant frequency of the differential inductor is placed at a higher frequency.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The wideband LNA is fabricated using 0.18 \(\mu m\) BiCMOS technology provided by Jazz Semiconductor. The die micrograph is shown in Fig. 16, where the total area is 0.25 mm\(^2\), excluding pads and output buffer. The mm-wave input, output and DC biasing signals are applied and monitored using on-wafer probing to reduce the losses and mismatches introduced by the measurement setup. Ground-Signal-Ground (GSG) probes are used to apply and measure the mm-wave signals, and an 8 pin DC probe is used to apply the required DC biasings. The effect of the output buffer is de-embedded from the LNA+Buffer measurements. The buffer is added at the output of the LNA to drive the 50 \(\Omega\) input impedance of the network analyzer.

The circuit S-parameters are measured using Agilent N5230A network analyzer. Fig. 17 shows the simulated and measured $S_{11}$ of the amplifier. Measured $S_{11}$ is lower than $-12$ dB for the entire 23–32 GHz frequency range. The simulated and measured voltage gain after de-embedding the buffer effect are also shown in Fig. 17. The buffer was designed to drive the 50 Ω impedance of network analyzer and a measured $S_{22}$ better than $-14$ dB across the band of interest is obtained as shown in Fig. 18. The effect of buffer is de-embedded from measurements by simulating its introduced loss and subtracting results from measured $S_{21}$. The measured voltage gain is 12 dB with a 3-dB bandwidth of 9 GHz (Fig. 17). The simulated bandwidth is 11.5 GHz. The difference between the simulated bandwidth and measured one could be due to the non-accurate models of the transistors that may lead to extra capacitance, and/or the effect of process variation. The measured reverse isolation, $S_{12}$, is less than $-35$ dB over the entire band (Fig. 18).

The measured noise figure versus the frequency is shown in Fig. 19, where the noise figure varies from 4.5 to 6.3 dB. A two-tone $\text{IP}_3$ measurement is performed for the LNA and the results are shown in Fig. 20 for the 23–32 GHz frequency range. The two tones are applied with the same amplitude and a frequency offset of 10 MHz. The measured $\text{IP}_3$ changes from $-4.5$ to $-6.3$ dBm across the entire frequency range. The measured $\text{IP}_3$ has two minima at 25 and 29 GHz. These two minima appear at the peak frequencies of the first stage coupled-resonator load. The measured phase and group delay are shown in Fig. 21. The LNA consumes 13 mW from a 1.5 V supply, and each gain stage consumes the same amount of power. The performance of the proposed wideband LNA and comparison with other existing wideband LNAs around the same frequency range are summarized in Table I. The proposed LNA achieves the highest bandwidth, comparable NF, $\text{IP}_3$ and gain, while consuming less amount of power and operating at a higher frequency range. To compare different topologies and remove the technology dependency, the figure of merit (FOM) in [19] is modified and is given by

$$FOM = \frac{\text{IP}_{3,\text{av}}[\text{mW}] \cdot \text{Gain}[\text{dB}] \cdot \text{BW}[\text{GHz}] \cdot f_{\text{center}}[\text{GHz}]}{(\text{NF}_{\text{av}} - 1)[\text{dB}] \cdot P_{\text{DC}}[\text{mW}] \cdot f_T^{-2}[\text{GHz}]^2}$$

(20)
where $IP_{3,\text{uv}}$ is the average input-referred third-order intercept point, $NF_{\text{av}}$ is the average noise figure, $P_{\text{DC}}$ is the DC power, $BW$ is the bandwidth, and $f_{\text{center}}$ is the center frequency.

The proposed FOM exhibit a factor of 2.4 better than the best previously reported results in [10] for low-cost CMOS/BiCMOS technologies.

V. CONCLUSION

A wideband BiCMOS LNA for the 23–32 GHz frequency band was implemented in this paper. The LNA utilizes coupled-resonator structures as the load to extend the bandwidth of the amplifier at mm-wave frequencies. The noise of the cascode transistor is removed through an additional wideband resonant circuit. Analytical expressions for the wideband input matching, gain, noise figure and linearity at mm-wave frequencies were developed to highlight the design tradeoffs. The LNA designs were implemented using 0.18 μm BiCMOS technology with an area of 0.25 mm². Measurements showed that the LNA is able to operate across a wideband while keeping the power consumption low. A voltage gain of 12 dB, 3-dB bandwidth of 9 GHz, noise figure between 4.5–6.3 dB, linearity higher than $-6.3$ dBm with a power consumption of 13 mW from a 1.5 V supply are achieved for the proposed LNA.

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REFERENCES


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