ECEN 326 LAB 3
Design of a Common-Source MOSFET Amplifier with a Source Follower

1 Circuit Topology and Design Equations

The following figure shows the two-stage dual-supply MOSFET amplifier circuit that will be designed in this lab.

![Circuit Diagram]

DC drain currents of $M_1$ and $M_4$ are set by the two current mirrors as follows:

$$I_{D1} = I_{D2} = I_{D3} = \frac{V_{SS} - V_{GS3}}{R_{B1}} = \frac{k'_n W}{2 L} (V_{GS3} - V_{tn})^2$$  \hspace{1cm} (1)

$$I_{D4} = I_{D5} = I_{D6} = \frac{V_{SS} - V_{GS6}}{R_{B2}} = \frac{k'_n W}{2 L} (V_{GS6} - V_{tn})^2$$  \hspace{1cm} (2)

For $M_1$, $M_2$ and $M_5$, the following should be satisfied for the active operation:

$$V_{DS} \geq V_{ov} = V_{GS} - V_{tn}$$  \hspace{1cm} (3)

The signal swing at the drain of $M_1$ is limited by $V_{DD}$ and $-V_{SS} + V_{ov2} + V_{ov1}$, provided that the gate bias of $M_1$ is arranged to have the maximum possible swing. However, the minimum value at $V_{D1}$ is usually limited by $-V_{SS} + V_{ov5} + V_{GS4}$, which is typically higher than $-V_{SS} + V_{ov2} + V_{ov1}$. In order to maximize the symmetrical swing, the DC bias at $V_{D1}$ may be centered between the upper and the lower limit. However, centering the DC bias is not always necessary, since it may conflict with other specifications. Nevertheless, the difference between $V_{D1}$ and the upper or lower limit should be greater than the desired swing at that node.

As in the case of BJT emitter-follower, MOS source follower bias current can be determined from

$$I_{D5} \geq \frac{0\text{-to-peak output swing}}{R_L}$$  \hspace{1cm} (4)

AC small-signal parameters can be obtained as:

$$A_v = \frac{v_{out}}{v_{in}} \approx -\frac{R_D}{g_{m1}} \frac{R_L}{g_{m4}} = -g_{m1} R_D \frac{R_L}{g_{m4}}$$  \hspace{1cm} (5)

where

$$g_m = k'_n \frac{W}{L} V_{ov} = \sqrt{2 k'_n \frac{W}{L} I_D}$$  \hspace{1cm} (6)

CD4007 transistor array will be used for the implementation of the amplifier. Transistor symbols N4007 and P4007 (NMOS and PMOS, respectively) are available within the CMOS library for PSPICE. Device parameters of CD4007 are approximately given as follows:
Connection diagram of the CD4007 chip (top view) is shown below.

Note that all P-channel substrates are connected to $V_{DD}$ and all N-channel substrates are connected to $-V_{SS}$.

### 2 Pre-Lab

Design a common-source MOSFET amplifier with a source follower using the following specifications:

- $V_{DD} = V_{SS} = 5\, V$
- $R_L = 5\, k\Omega$
- Operating frequency: $5\, kHz$
- $R_{in} \geq 100\, k\Omega$
- $|A_v| = 30$
- Zero-to-peak un-clipped swing at $V_{out} \geq 2.5\, V$
- $I_{supply} \leq 1.5\, mA$

1. Show all your calculations, design procedure, and final component values.

2. Verify your results using PSPICE. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.

3. Using PSPICE, perform Fourier analysis and determine the input and the output signal amplitudes resulting in 5% total harmonic distortion (THD) at the output. Submit transient and Fourier plots, and the distortion data from the output file.

4. Be prepared to discuss your design at the beginning of the lab period with your TA.

### 3 Lab Procedure

1. Construct the amplifier you designed in the pre-lab.

2. Measure $I_{D1}$, $I_{D4}$, $V_{D1}$, $V_{D2}$ and $V_{D5}$. If any DC bias value (especially $I_D$) is significantly different than the one obtained from Pspice simulations, modify your circuit (i.e. change $R_{B1}$, $R_{B2}$, $R_{G1}$, or $R_{G2}$) to get the desired DC bias before you move onto the next step.

3. Measure $A_v$, $R_{in}$, and $I_{supply}$ (for both $V_{DD}$ and $-V_{SS}$).

4. Measure the maximum un-clipped output signal amplitude.

5. Apply the input signal level resulting in 5% THD at the output, and measure the input and output signal amplitudes.

6. Prepare a data sheet showing your simulated and measured values.

7. Be prepared to discuss your experiment with your TA. Have your data sheet checked off by your TA before leaving the lab.