

Low-Power Area-Efficient High-Speed I/O Circuit Techniques

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Abstract—We present a 4-Gb/s I/O circuit that fits in 0.1-mm² of die area, dissipates 90 mW of power, and operates over 1 m of 7-mil 0.5-oz PCB trace in a 0.25- μ m CMOS technology. Swing reduction is used in an input-multiplexed transmitter to provide most of the speed advantage of an output-multiplexed architecture with significantly lower power and area. A delay-locked loop (DLL) using a supply-regulated inverter delay line gives very low jitter at a fraction of the power of a source-coupled delay line-based DLL. Receiver capacitive offset trimming decreases the minimum resolvable swing to 8 mV, greatly reducing the transmission energy without affecting the performance of the receive amplifier. These circuit techniques enable a high level of I/O integration to relieve the pin bandwidth bottleneck of modern VLSI chips.

Index Terms—Delay-locked loops, equalization, I/O circuits, offset-cancellation, serial links.

I. INTRODUCTION

THE PERFORMANCE of many digital systems is limited by the interconnection bandwidth between chips, boards, and cabinets. Today, most CMOS chips drive unterminated lines with full-swing CMOS drivers and use CMOS gates as receivers. Such full-swing CMOS interconnect must ring-up the line, and hence has a bandwidth that is limited by the length of the line rather than the performance of the semiconductor technology. Thus, as VLSI technology scales, the pin bandwidth does not scale with the technology, but rather remains limited by board and cable geometry, making off-chip bandwidth an even more critical bottleneck.

Recently described I/O circuits have increased the absolute I/O bandwidth by an order of magnitude [1]–[4]. More importantly, they have put this bandwidth back on the semiconductor technology-scaling curve by signaling with the incident wave from the transmitter rather than ringing up the line. To achieve incident-wave signaling, these circuits use point-to-point interconnect over terminated transmission lines. Differential current-mode signaling is often used to reject common mode noise, minimize EMI, reduce ground/supply bounce, isolate the system from noisy ground/supply, and double the slew rate. Simultaneous bidirectional signaling is sometimes incorporated to increase the bandwidth per pin [5]. On the receive side,

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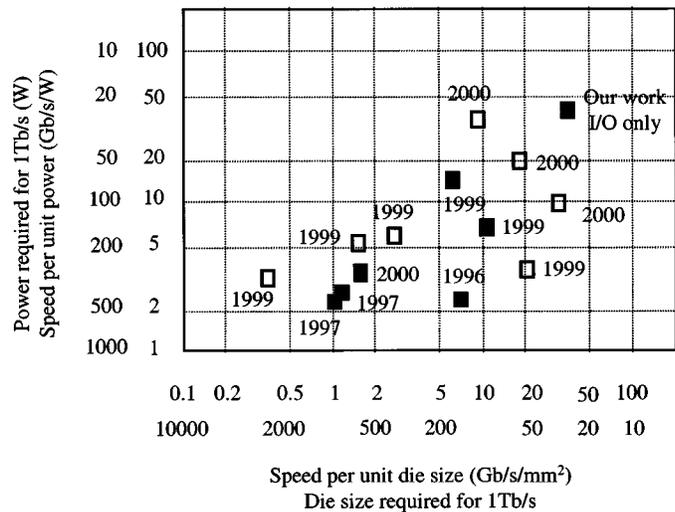


Fig. 1. Link performance trend.

inverters are replaced by sensitive receive amplifiers to reduce the required receiver signal levels, and hence the transmission energy. Precision timing circuits based on delay-locked loops (DLLs) or phase-locked loops (PLLs) are employed in these systems since a critical limitation of the achievable speed is the timing accuracy. In cases where significant cable loss occurs, signaling rate is still restricted by the media. Equalization is incorporated in such cases to cancel the loss and remove this restriction [1], [2], [4].

A key remaining problem with high-speed I/Os is reducing the area and power of these circuits to enable very high levels of integration. To relieve the pin-bandwidth bottleneck of modern VLSI chips used for network switching fabrics, multi-computer routers, telecommunication switches, and CPU-memory interfaces, hundreds of these high-speed I/Os must be integrated on a single chip. A substantial number of the pins on such chips need to use high-speed signaling, not just a few special pins. Fig. 1 shows the trend in published I/O link performance in terms of speed per unit power and speed per unit die size (normalized to 0.25 μ m) [14]. Also shown on the axes are the power consumption and die area required to achieve 1 Tb/s/chip bandwidth (both into and out of a chip). As can be seen, achieving 1 Tb/s/chip bandwidth is rather costly with modern I/O technologies. Speed per unit power and speed per unit die size do not tell the complete story because power grows more than linearly with speed. In particular, as the bit time is reduced below $4T_d$, simple transmitter circuits no longer operate and more power hungry circuits using finely spaced clock phases and heavily

multiplexed transmitters must be employed¹ [1], [3], [6]. For this reason, we use solid squares in Fig. 1 to denote links operating at a bit time $< 4\tau_4$.

In this paper, we introduce several circuit techniques that reduce the area and power consumption of high speed I/Os by factors of 6.9 and 2.6 respectively compared to the previous best published result. These techniques are general and can be applied to any signaling system to improve the existing design. They are particularly relevant to designs targeted at bit times less than $4\tau_4$. The demonstration chip, which incorporates current-mode differential unidirectional signaling, achieves 4 Gb/s over 1 m of printed circuit board (PCB) trace or 15-m of 24 American Wire Gauge (AWG) cable with 90 mW of power and 0.1 mm^2 of area. This corresponds to 44 Gb/s/W and 40 Gb/s/ mm^2 . The best published designs to date with similar speed (3.5 Gb/s), signaling setup (current-mode differential unidirectional signaling) and equalization capability requires 250 mW and 0.6 mm^2 , equivalent to 16.7 Gb/s/W and 5.8 Gb/s/ mm^2 [7].

To achieve this small area and low power, our prototype chip employs three key circuit techniques. An input-multiplexed transmitter reduces clock load by an order of magnitude by multiplexing signals before rather than after amplification. It also reduces area by requiring only a single copy of the output driver rather than one copy for each multiplexer input. Voltage swing in the signal path is optimized to attain speed significantly higher than previously achieved with similar architecture. A DLL based on supply-regulated inverters gives very low jitter at a fraction of the power of a conventional source-coupled delay line. Finally, a sensitive capacitively trimmed receiver enables reliable operation at very low signal levels, further reducing area and power.

Section II describes the system architecture of the I/O link and the reasons behind it. Section III discusses the circuit details. Experimental results of the 4-Gb/s test link are presented in Section IV, followed by concluding remarks in Section V.

II. SYSTEM ARCHITECTURE

A. Overall Architecture

The overall I/O link architecture is shown in Fig. 2. To operate with a bit time of $2\tau_4$ (250 ps), we employ 4 : 1 multiplexing in the transmitter and 1 : 4 demultiplexing in the receiver. On the transmit side, an on-chip inverter-based DLL (TxDLL) generates four evenly spaced 1-GHz clock phases to sequence 1-GHz 4-bit wide data on-chip into a 4-Gb/s bit stream off-chip. This is achieved by first resynchronizing the 1-GHz data from a single clock domain to per-phase clock domains. Then a fast multiplexer, driven by the four phases, serializes the data. Both the transmitter and receiver terminate the line into a digitally-trimmed matched impedance. The receiver is a mirror image of the transmitter. The serial bit stream is sampled and de-serialized by a 4-phase 1-GHz receive clock generated by a receiver DLL (RxDLL). The data are then resynchronized from the per-phase clock domains to a single clock domain to be processed further by other digital logic. A 20-bit pseudo-random

¹ τ_4 is the delay of an inverter with a fanout of four, about 125 ps in an $0.25\text{-}\mu\text{m}$ technology [11].

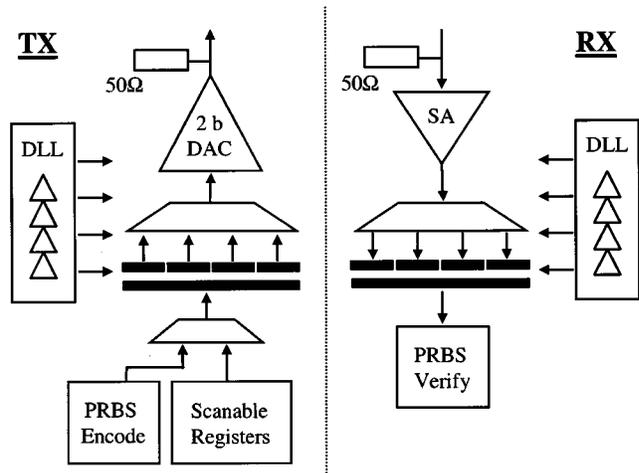


Fig. 2. System architecture of the test link.

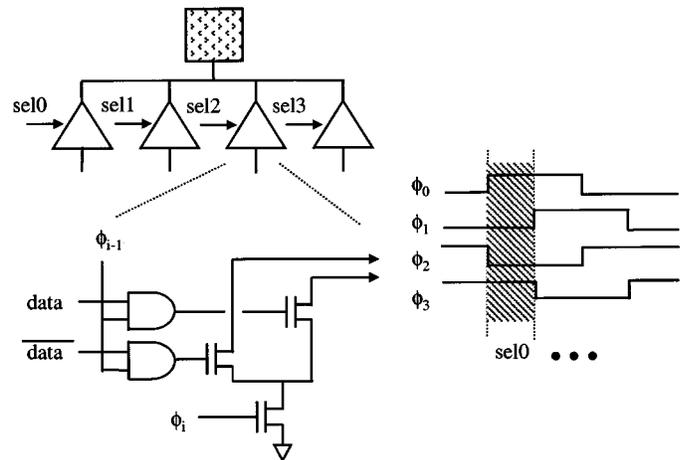


Fig. 3. Output-multiplexed transmitter architecture.

bit sequence (PRBS) generator is integrated with the transmitter and a PRBS verifier with the receiver.

B. Transmitter

The shortest achievable clock period in a given technology is limited to be no less than about $8\tau_4$ (roughly 1 ns in $0.25 \mu\text{m}$). Thus, a fast multiplexer is needed to take a parallel signal with this clock period and multiplex it into a serial signal with a shorter bit time, $2\tau_4$ in the present case. As shown in Fig. 3, previously published transmitter designs achieve high bandwidth by multiplexing directly at the output pin where both a low time constant ($25\text{--}50 \Omega$ impedance and a $1\text{--}2 \text{ pF}$ load) and small swings are present. Two adjacent clock phases are used to generate a short differential current pulse equal to a bit time. The minimum bit time achievable with this architecture can be less than τ_4 [1], [3].

The output-multiplexed architecture is very costly in terms of power and area. This architecture requires multiple copies of the output driver, each sized to drive signals off-chip. The clock load of the multiplexer is very large since it is switching the signal after it has been fully amplified to drive off-chip. This combination of duplicate circuitry and multiplexing amplified signals results in significant clock load, clock jitter, die area, and

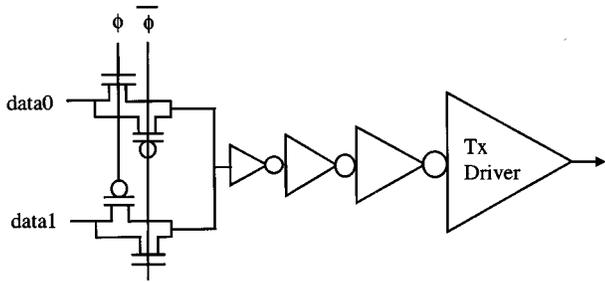


Fig. 4. Input multiplexing with static gates.

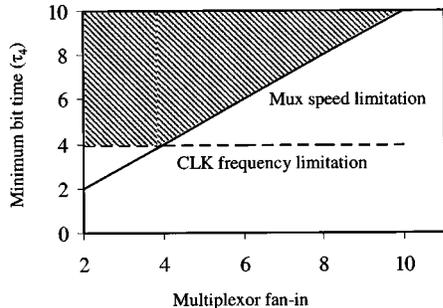


Fig. 5. Minimum achievable bit time for the configuration in Fig. 4.

power consumption, making it unsuitable for heavily integrated applications.

A more cost-effective solution is to perform multiplexing at the input of the transmitter before the signal is buffered up. Previous input-multiplexed architecture designs use static CMOS gates to perform multiplexing and buffering to drive the final output driver as shown in Fig. 4 [8], [9]. However, this design style is unable to achieve signaling rate higher than $4\tau_4$ because of the bandwidth limit of CMOS gates. Fig. 5 shows the maximum signaling rate versus the degree of multiplexing. The shaded area denotes the achievable bit time. The speed is initially limited by the achievable clock frequency at 2:1 multiplexing ratio. Above this point, high multiplexer fan-in becomes the bottleneck and the achievable speed gradually decreases.

This speed limitation is not an inherent property of the process technology but of the circuit topology. Since the output swing of the transmitter is much smaller than the full CMOS swing, signal attenuation is another degree of freedom in optimizing speed and power. In the output-multiplexed architecture, all of the signal attenuation occurs at the bottleneck point, the output. This signal attenuation trades gain for higher bandwidth. The input-multiplexed architecture, on the other hand, applies no signal attenuation at its bottleneck node, the multiplexer. A good balance between maximizing speed and minimizing power is achieved by an input-multiplexed architecture where the voltage swing and the capacitive fan-out at each stage (from the multiplexer to the final output driver) are carefully chosen to meet the required speed and final output swing. In order to do this, circuit topologies which allow direct tradeoff between signal swing and bandwidth are employed. The minimum bit time achievable with this configuration is about τ_4 .

A general rule of thumb can be derived from the above discussion to select a transmitter architecture given the system performance requirement. If the targeted bit time, t_{bit} is above $4\tau_4$

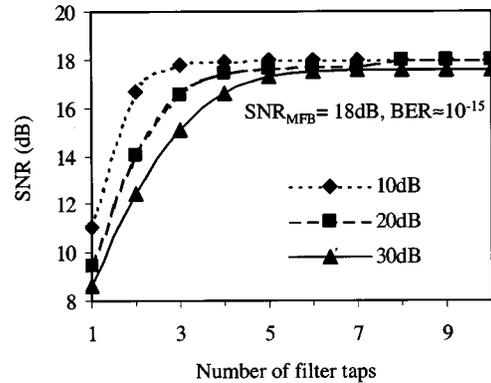


Fig. 6. SNR versus number of pre-emphasis equalizer taps for a channel with 10, 20, and 30 dB attenuation at 2 GHz.

(500 ps in 0.25- μm CMOS), an input-multiplexed architecture with static CMOS gates should be used due to its simplicity. For $\tau_4 < t_{\text{bit}} < 4\tau_4$, an input-multiplexed architecture with reduced voltage swing should be chosen to give higher speed than is possible with static CMOS while retaining the power advantage of input multiplexing. For $t_{\text{bit}} < \tau_4$, an output-multiplexed architecture should be employed.

C. Equalization

Our prototype circuit is designed to transmit across 1 m of 7-mil 0.5-oz PCB traces or 15 m of 24 AWG cable. The frequency dependent attenuation from dc to 2 GHz, which contains most of the signal energy for 4-Gb/s nonreturn-to-zero (NRZ) binary transmission, is about 10 dB for both cases. To cancel this loss and avoid noise amplification while operating at Gb/s signaling rate, the transmitter includes a finite-impulse-response (FIR) pre-emphasis filter. Fig. 6 shows the signal-to-noise ratio (SNR) versus the number of filter taps for various channel attenuations based on the minimum mean squared error (MMSE) criterion, where the following quantity is minimized [10]:

$$\sigma_{\text{MMSE-LE}}^2 = E(|e_k|^2) = E(|x_k - y_k|^2).$$

x_k is the original signal and y_k is the signal at the input of the receiver. SNR_{MFB} represents the maximum SNR without any channel attenuation and error-correcting codes and is chosen to be 18 dB for a typical bit-error rate (BER) of 10^{-15} . The channel is 7-mil 0.5-oz GETEK PCB trace [11], and is simulated using HSPICE's W -element. The plot indicates that increasing the number of filter taps beyond two improves SNR by at most 2 dB. To reduce the overall power and area, a simple two-tap FIR filter was therefore chosen. As channel attenuation becomes more severe, SNR gain beyond two taps becomes more significant.

III. CIRCUIT DETAILS

A. Transmitter

Fig. 7 shows the transmitter circuit diagram. It consists of a 4:1 multiplexer, a pre-amplifier, and an output driver. The transmitter employs dual pseudo-nMOS multiplexers at its input, one for the signal and one for its complement. Each multiplexer input is switched by two series nMOS that are gated by two

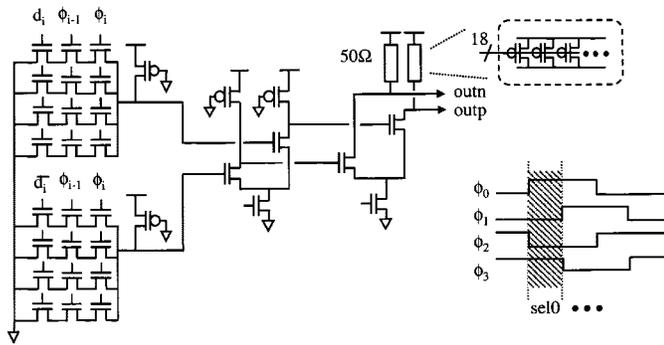


Fig. 7. Input-multiplexed transmitter architecture.

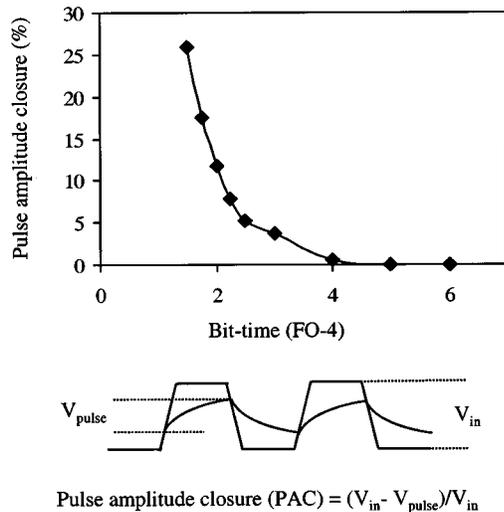


Fig. 8. Effect of bit-time on pulse amplitude closure for the 4:1 pseudo-nMOS multiplexer.

adjacent clock phases in the same manner that the driver pull-downs in Fig. 3 are gated by adjacent clock phases. Thus, input d_i is enabled onto the preamplifier input during phase ϕ_i .

Fig. 8 shows the pulse amplitude closure (PAC) versus the bit time for our pseudo-nMOS multiplexer implementation driving the preamplifier. The speed of this circuit is mainly determined by the resistance of pMOS and the total capacitance at the output node. If we allow a maximum of 10% PAC, this circuit can operate at $2\tau_4$, or 250 ps in a 0.25- μm technology. The power overhead for the increased speed compared to a static implementation is small since low energy signals are multiplexed before the preamplifier and the final driver.

The transmitter and receiver both include 50- Ω pMOS termination resistors with 18 bits of thermometer-coded control. The adjustment step is about 5%. In order for the pMOS transistor to work well as a resistor, the output swing should be kept well inside its linear regime. In our implementation, for example, to avoid more than 10% of resistance variation the swing needs to be less than 200 mV.

The two-tap FIR filter is implemented by summing two legs of transmitter drivers directly at the output pin (effectively a 2-bit digital-to-analog converter) [1], [2], [4]. The tap coefficients are adjusted by varying the bias current of the two output drivers. They can also be made programmable for different channels with simple current mirrors.

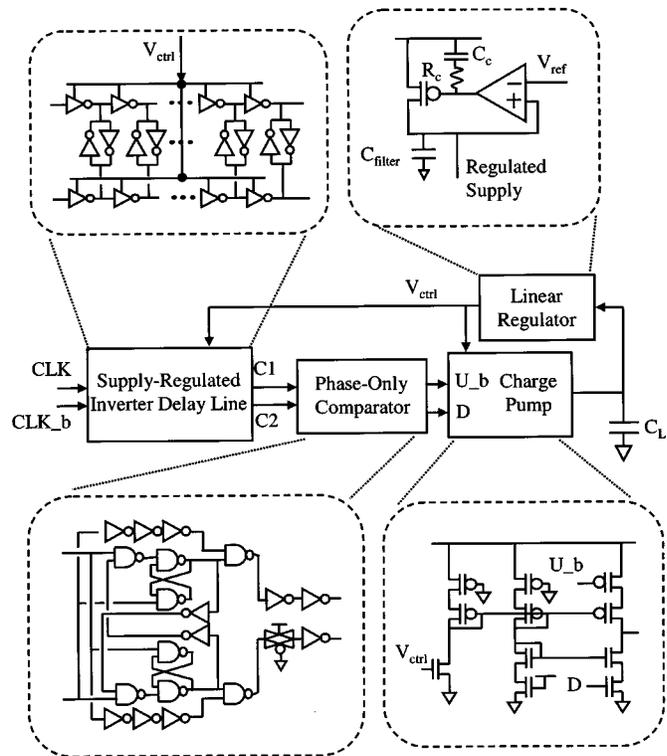


Fig. 9. Schematic diagram of DLL.

B. Delay-Locked Loop

The DLL generates evenly spaced clock phases at 1 GHz to sequence the multiplexer at the transmitter and the demultiplexer at the receiver. As shown in Fig. 9, our DLL uses a differential CMOS inverter delay line with a regulated power supply. Operating differentially generates fine phases and the complementary outputs simplify the level shifter. The true and complement outputs of each stage are cross-coupled with weak inverters to minimize skew. Delay is adjusted by varying the supply voltage with a linear voltage regulator.

A source-coupled differential pair with replica-bias delay adjustment is widely used as a delay element due to its low supply sensitivity of -0.2 (fraction delay change per fraction of supply change) [11], [12]. However, compared to a static CMOS inverter delay element, it requires more power and is more susceptible to substrate noise and transistor mismatches. The power consumed in an N-phase differential inverter delay line and differential source-coupled delay line are

$$P_{\text{INV}} = N \frac{C_T V_{C-\text{INV}} V_{dd}}{T_C}$$

$$= \frac{C_T V_{C-\text{INV}} V_{dd}}{T_D}, \text{ inverter element based}$$

$$P_{\text{SC}} = \frac{N}{2} \frac{C_T V_{C-\text{SC}} V_{dd}}{T_D}, \text{ source-coupled element based}$$

where

- T_D stage delay;
- T_C clock cycle time;
- $V_{C-\text{INV}}$ inverter delay line control voltage;

V_{C-SC} source-coupled delay line control voltage;
 C_T total capacitance charged at each stage during a cycle, roughly the same for both with the same accuracy requirement.

Notice that the inverter delay line requires twice as many delay elements compared to the source-coupled delay line since the availability of differential signals is assumed. If $V_{C-INV} = kV_{C-SC}$, this analysis indicates that inverter-based delay lines consume $2k/N$ of the power consumed by source-coupled delay lines, where k is usually between 1 and 1.5. Intuitively, the factor N comes from the fact that inverter delay line does not consume any static current. For our case, N is 4 and the power is reduced to $0.75 \sim 0.5$. As N increases (in applications such as clock recovery circuits or when the degree of multiplexing is increased), power saving is more significant.

Inverter delay elements are also more robust against substrate noise and transistor mismatches. A source coupled delay element is particularly vulnerable to any noise introduced to its tail current source. For the delay element described in [12], it was found that the sensitivity of its delay to the tail current around the correct bias point is about 0.5. Using this relationship, we can derive the variation in delay as

$$\begin{aligned} \left(\frac{\sigma_{td}}{td}\right)^2 &\approx \left(0.5 \frac{\sigma_{I_T}}{I_T}\right)^2 = \left(0.25 \frac{\sigma_{\beta}^2}{\beta^2} + \frac{\sigma_{V_T}^2}{(V_{gs} - V_T)^2}\right) \\ &\approx \frac{\sigma_{V_T}^2}{(V_{gs} - V_T)^2} \end{aligned}$$

where $\beta = \mu C_{ox}(W/L)$ [16]. The last approximation is valid in this case since the tail current source has a small $V_{gs} - V_T$. Static V_T mismatches become static phase error while dynamic V_T variation due to substrate or other noise sources converts to jitter. The inverter delay element is more robust against these noise sources since its $V_{gs} - V_T$ is considerably larger.

Since the two branches of the inverter delay line are not truly differential, cross-coupled inverters are inserted to minimize skew between the two lines. These cross-coupled inverters are weak compared to the delay inverters, but are very effective in eliminating skew and hence reducing phase spacing imbalances. In our design, the cross-coupled inverters are 1/4 the size of the delay inverters. Inserting input clock skews of up to 200 ps increases the phase spacing difference by less than 40 ps. Without the cross-coupled inverters, this number would increase to 400 ps.

Fig. 9 also shows the overall architecture of the DLL and the detailed schematics of the sequential phase-only comparator, the charge pump, and the linear voltage regulator. Since the phase of a delay line has a finite range, a phase-only comparator has to be employed in place of the commonly used three-state phase-frequency detector (PFD) to avoid pegging the DLL at the end of its adjustment range due to noise or incorrect starting state. The charge pump current I_p is made proportional to V_{ctrl}^2 ($I_p = K_1 V_{ctrl}^2$) with an nMOS transistor as shown in Fig. 9. The inverter delay line gain K_{DL} is roughly proportional to $1/V_{ctrl}^2$ ($K_{DL} = K_2/V_{ctrl}^2$). The loop bandwidth ω_1 of the DLL is thus

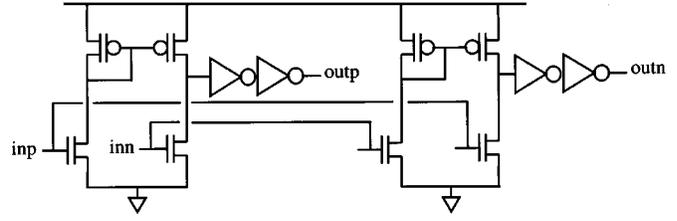


Fig. 10. Delay-line low-high output buffer.

fixed at a constant fraction of the input frequency as seen by

$$\begin{aligned} \omega_1 &= \frac{I_p K_{DL} \omega_{in}}{2\pi C_L} = \frac{(K_1 V_{ctrl}^2) \cdot (K_2 \cdot 1/V_{ctrl}^2) \cdot \omega_{in}}{2\pi C_L} \\ &= \frac{K_1 K_2}{2\pi C_L} \omega_{in} \end{aligned}$$

where ω_{in} is the input frequency and C_L is the loop capacitance filter [12]. The regulator, which has a -3 -dB bandwidth in excess of 300 MHz, does not affect the loop dynamics. Keeping the loop bandwidth at a constant fraction of the input frequency ensures the stability of the loop across a wide range of input frequencies as well as process, voltage, and temperature (PVT) conditions.

The goals of the linear voltage regulator are to provide enough driving capability for the delay line, to shield the delay line from the supply noise, and to have enough bandwidth to ensure the overall stability of the loop. The voltage regulator employs lead compensation at the output of the one-pole feedback amp. Inserting R_c creates one zero ($1/R_c C_c$) and one higher-frequency pole ($1/R_c C_T$, where C_T is the effective capacitance at the output of the feedback amp). Using the zero to cancel the pole at the output of the regulator thus effectively increases the frequency of the second pole. It also shields the stability of the regulator from the value of C_{filter} , which should be as large as possible to reject power supply noise. The output pull-up pMOS is sized as small as possible since the noise peak as a result of a supply transition is caused mostly by parasitic capacitance coupling. For our design, the supply sensitivity with a fast (100 ps) supply transition is 0.1 (peak noise) and the steady state error is about 0.01. As a consequence, although inverter delay element has a supply sensitivity of about -0.9 ($4.5 \times$ worse than the source-coupled delay element) [11], the voltage regulator is able to reduce this number by $10 \times$, resulting in the overall supply sensitivity of -0.09 .

Fig. 10 shows the level shifter at the output of the delay line that converts the V_{ctrl} level signal to full V_{DD} level. The level shifter employs circuit topologies that have opposite supply sensitivities connected in series to cancel noise from the unregulated power supply and to reduce the steady state phase error. The first stage current mirror amplifier has a positive supply sensitivity while the subsequent inverters have a negative supply sensitivity. The relative fanout of the two stages is tuned so that the combined supply sensitivity of the delay line and the low-high amplifier in steady state approaches zero.

Fig. 11 shows the DLL undergoing a 10% supply pulse in simulation under the typical corner. The DLL locks in about 30 cycles. The peak-to-peak jitter is 30 ps including the output clock buffers, and the steady state error is on the order of 1 ps,

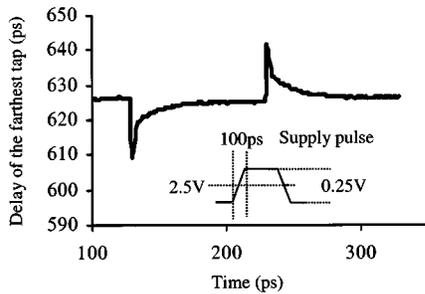


Fig. 11. DLL undergoes a 10% supply pulse with 100 ps rise/fall time.

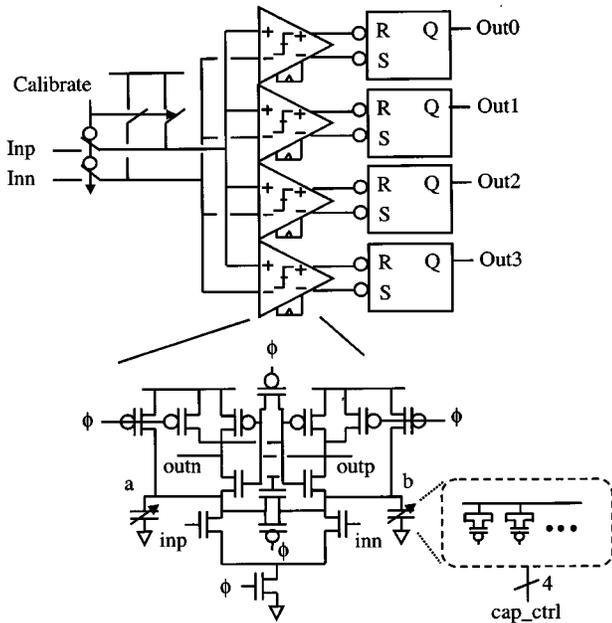


Fig. 12. Schematic diagram of the 4:1 demux receiver.

which shows the effectiveness of the noise sensitivity cancellation scheme described above.

C. Receiver

The receive amplifier, shown in Fig. 12, is a modified version of the StrongArm sense amplifier (SA) with capacitively trimmed offset voltage [13], [15]. We trim the SAs by placing 4-bit binary-weighted pMOS capacitors on the two integrating nodes directly above the input transistors (nodes a and b). Digitally adjusting the capacitance while shorting the inputs unbalances the amplifier to cancel the offset voltage. The trimming capacitors introduce up to ± 120 mV of offset in 8-mV steps. With digital bang-bang control, the worst case offset after cancellation is 8-mV with any untrimmed offset < 120 mV. The variation of offset control steps across all supply (2.25–2.75 V) and temperature (0–100 °C) corners is $< 10\%$, indicating its effectiveness as a static mechanism. The simulated 3σ offset of this sense amplifier is 60 mV (from manufacturer's process spec on A_{VT} and A_{β} [16]). Without offset cancellation, the receive amplifier would need to be enlarged by a factor given by

$$\left(\frac{60 \text{ mV}}{8 \text{ mV}}\right)^2 \approx 50$$

in order to have a 3σ offset of 8 mV.

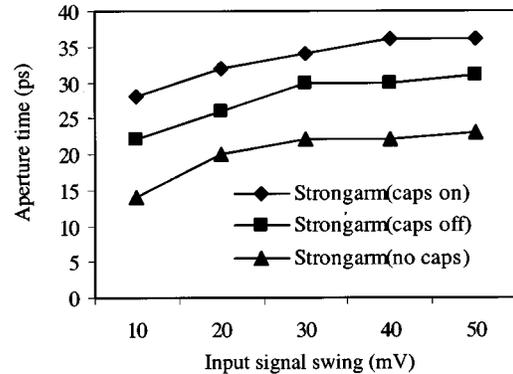


Fig. 13. Aperture window of receive amplifier versus the receiver input swing.

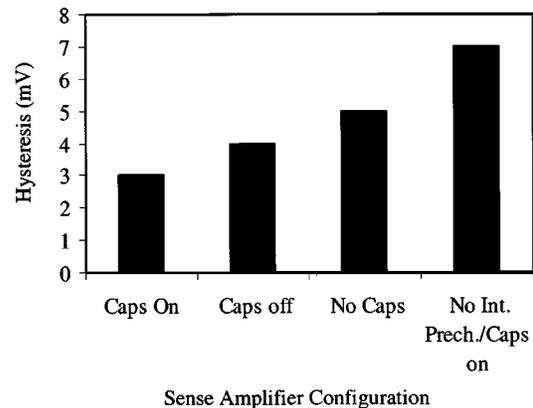


Fig. 14. Hysteresis of receive amplifier.

Both the outputs and the internal nodes a and b are precharged to reduce hysteresis, increase the input sensitivity, and increase the effectiveness of offset cancellation. Without precharging nodes a and b, the current difference on the two sides of SA would not have much time to integrate on these two trimmed capacitance nodes, and the effect of offset cancellation would degrade considerably.

Fig. 13 shows the simulated aperture time of three variations of our receive amplifier: capacitively trimmed SA with all capacitors switched on, the same SA with all capacitors off, and an SA without any trimming capacitors attached. The simulation assumes a clock rise/fall time of 100 ps. The worst case aperture time with all trimming capacitors switched on is ~ 35 ps, ~ 15 ps (6% of the 250-ps bit time) worse than the bare SA.

Fig. 14 shows the hysteresis for several variations of the SA followed by an RS latch. Hysteresis is simulated by sampling an input swing of 50 mV, and then switching the differential input into the smallest negative input swing that would toggle the SA. If the internal nodes directly above the input transistors are not precharged, the hysteresis increases from 3 to 7 mV due to internal residual memory from previous bits. Adding capacitive load at the internal nodes with capacitive trimming slightly improves the hysteresis since it increases the current difference on the two sides by keeping the drain of the input transistors at a higher voltage during regeneration. The majority of the hysteresis comes from the data dependent capacitive load of the RS latch. Inserting a scaled down version of the StrongArm latch between the input sense amplifier and the RS latch would reduce the hysteresis to an undetectable level. The sensitivity of

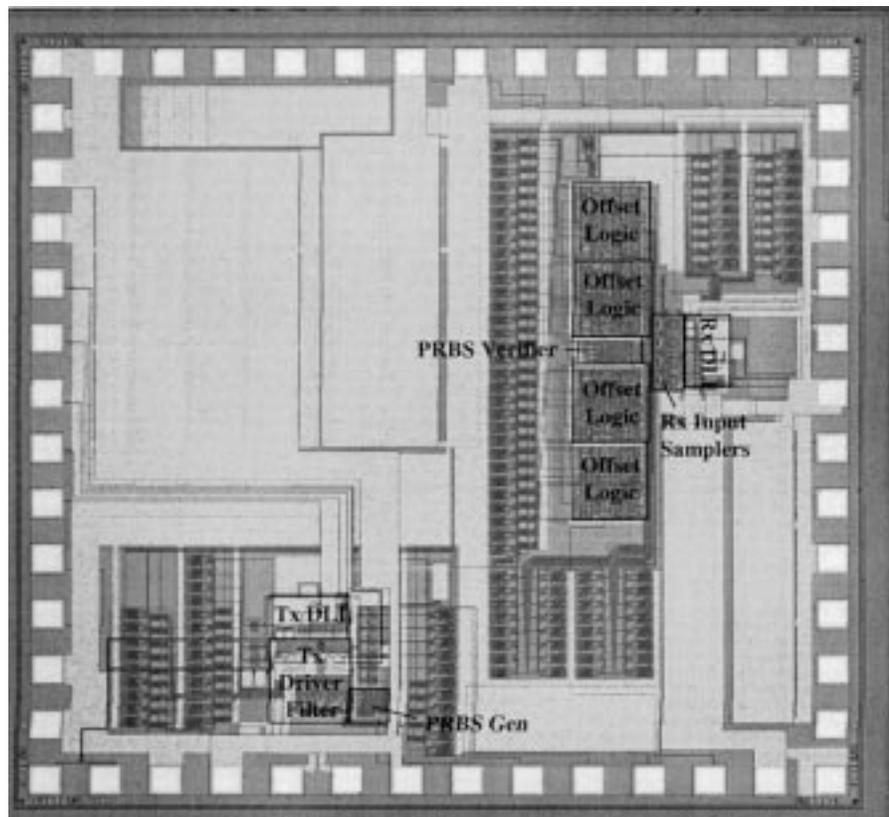


Fig. 15. Chip photomicrograph.

such sense amplifier is generally on the order of μV and is negligible compared to its hysteresis.

IV. EXPERIMENTAL RESULTS

A prototype chip was fabricated in National Semiconductor's $0.25\text{-}\mu\text{m}$ CMOS technology with a 2.5-V nominal supply. Fig. 15 shows the chip photomicrograph. The die area is $2\text{ mm} \times 2\text{ mm}$ while the core transceiver circuit including DLLs occupies only 0.1 mm^2 . The chip is packaged in a 52-pin leaded chip carrier (LDCC) package with internal power planes for controlled impedance. Receiver timing recovery circuits were not implemented in this test chip but can be easily integrated by incorporating a peripheral DLL loop as described in [17].

Fig. 16(a) shows the eye diagram at the output of the transmitter with the equalizer disabled. The swing shown is 100 mV . The peak current drive can be as high as 20 mA . Fig. 16(b) shows the eye diagram after 1 m of 7-mil 0.5-oz GETEK PCB trace. The diagram shows that this medium causes enough intersymbol interference (ISI) to completely close the eye, making reliable detection impossible. Fig. 16(c) shows the eye diagram at the near end and Fig. 16(d) at the far end after equalization is turned on. The figures show that there is sufficient eye opening at the far end for reliable detection.

It was observed that the widths of the four bits in a 1 GHz cycle are uneven. Post tapeout simulations on extracted layout showed the same uneven eye patterns, and the cause was determined to be grossly asymmetrical wire layout on one of the clock phases, resulting in its phase being shifted by $20\text{--}30\text{ ps}$,

enlarging one of the bits while shrinking its neighboring one. The peak-peak jitter at the transmitter output is 16.4 ps , which is negligible compared to the 250-ps targeted bit time.

Fig. 17 shows the receiver timing margin at 4 Gb/s . The graph shows whether the link operates properly (PASS) as a function of single-ended signal level (the vertical axis) and clock position (the horizontal axis). All "PASS" points have a BER of at least 10^{-12} (5 min of operation without any error). The plot shows that receiver offset cancellation increases the timing margin by about 40 to 220 ps (out of 250-ps bit time, or 0.88 UI) and reduces the minimum resolvable swing from 20 to 8 mV . Under varying temperature conditions and 8 mV of transmitter swing, the link achieves a BER of better than 10^{-13} . Because of offset cancellation, the I/O circuits operate quite reliably with very small voltage swings. The receiver has a BER well below 10^{-14} with a swing of only 20 mV (no error has ever been seen with signal swings above this value). Fig. 16 also shows that the particular chip tested has an untrimmed offset of at least 20 mV , corresponding to 1σ offset.

Fig. 18 shows the power consumption of the I/O versus the signal swing at the input of the receiver. The solid line is for a channel without significant attenuation and the dotted line for 1 m of 7-mil 0.5-oz PCB trace. Because of the channel attenuation, the power consumption for the latter case is significantly higher since more current needs to be driven at the transmitter to get the same signal swing at the receiver. At 20-mV receiver swing, the total power consumption of the link, including I/O circuits and supporting test logic, is 90 mW . Approximately 7 mW is due to the supporting test logic. Fig. 19

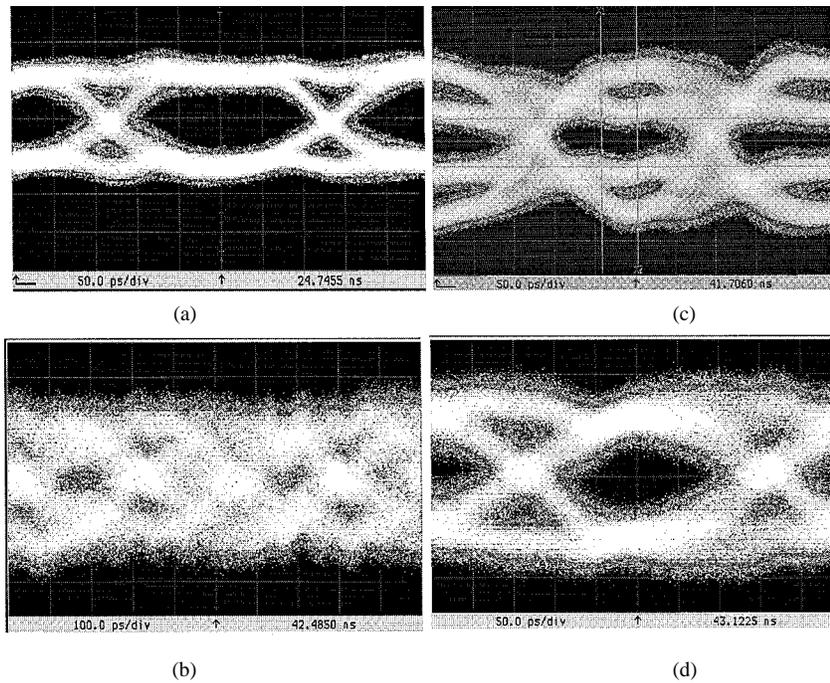


Fig. 16. Transmitter eye diagram. (a) At transmitter output. (b) At the far end of 1-m 7-mil 0.5-oz PCB trace without equalization. (c) At the near end of 1-m 7-mil 0.5-oz PCB trace with equalization. (d) At the far end of 1-m 7-mil 0.5-oz PCB trace with equalization.

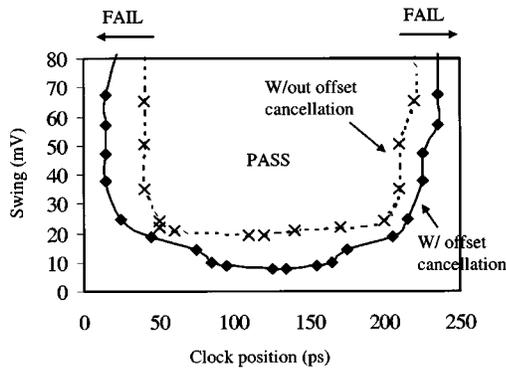


Fig. 17. Timing margin of the receiver.

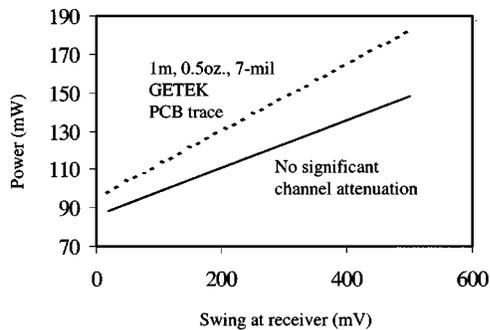


Fig. 18. Power versus swing at receiver input.

shows the power consumption versus the maximum speed for supply varying from 2.5 to 2.85 V. At 2.5 V, the maximum speed of the DLL and the transmitter is 1.15 GHz and 4.6 Gb/s. At 2.85 V, the maximum speed is 1.325 GHz and 5.3 Gb/s. The receiver, which is not shown, is limited to 4 Gb/s due to a speed path in the PRBS verifier. Table I summarizes the test link performance.

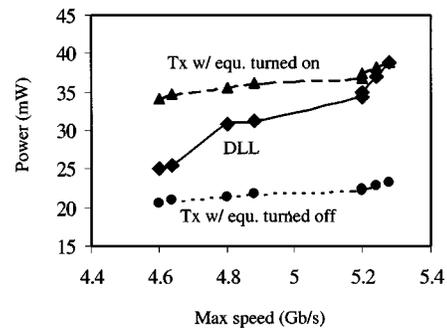


Fig. 19. Power versus maximum speed at 20 mV receiver swing for supply varying from 2.5 to 2.85 V.

TABLE I
TEST CHIP PERFORMANCE SUMMARY

Process	National 0.25 μ m CMOS
Nominal Supply	2.5V
Max Speed	Tx: 5.3Gb/s, DLL: 5.3Gb/s, Rx: 4Gb/s
Power @ 2.5V, 4Gb/s, 20mV Swing	Tx Driver & Test Logic (no eq.): 20mW Tx Driver & Test Logic: 30mW 2 DLL: 50mW Rx Input Samplers & Test Logic: 18mW
BER @ 4Gb/s, 20mV Swing	$\ll 10^{-14}$
Active Area	Tx Driver & Test Logic: 160 x 200 μ m ² DLL: 120 x 200 μ m ² Receive amplifiers & Test Logic: 250 x 100 μ m ² OC Synthesized Logic: 820 x 160 μ m ²
Min Swing @ 4Gb/s	8 mV (for BER $< 10^{-15}$)
Jitter (quiet supply) @ 4Gb/s	16.5 psec (p-p)

V. SUMMARY AND CONCLUSION

We have employed three circuit techniques to reduce the power and area of I/O circuits. An input-multiplexed trans-

mitter architecture with reduced voltage swing allows a small transmitter to be used while still providing most of the speed advantage of an output-multiplexed architecture. Because low energy signals are multiplexed before the preamplifier and the output driver, clock load, clock power and clock jitter are significantly reduced. A two-tap transmitter pre-emphasis FIR filter is determined to be sufficient based on MMSE analysis. It is employed over receiver equalization to avoid noise amplification, reduce complexity, and achieve a higher speed of operation. An inverter-based DLL with regulated supply reduces the power consumption of the delay line while achieving better supply noise rejection compared to a source-coupled differential-pair delay line. It is also less sensitive to substrate noise and transistor mismatches due to a higher gate overdrive. Capacitive offset trimming at the receiver eliminates a major noise source in I/O links without affecting the performance of the receive amplifier. It allows multiple parallel receive amplifiers to be employed at the input pad with negligible power, area and input capacitance overhead. Signal transmission energy can be significantly reduced since a smaller signal swing is required.

The above techniques were employed in a 4-Gb/s test link that fits in 0.1 mm² of die area, dissipates 90 mW of power, and operates over 1 m of 7-mil 0.5-oz PCB trace. With 8 mV of minimum resolvable swing, it also shows that the offset trimming technique is quite effective. The technique we describe here enable a high level of I/O integration to relieve the pin bandwidth bottleneck of modern VLSI chips.

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