Announcements

• Exam 2 is April 30
  • Will emphasize (but not limited to)
    • Equalization properties & circuits
    • Link Budgeting (noise & timing)
    • PLLs
    • CDRs (high-level properties)

• Project Feedback meetings on Friday

• Final Project Report Due May 4
Agenda

• CDR circuits
  • PI
  • DLL

• CDR Jitter Properties

• Injection-Locked Oscillator De-Skew
Embedded Clock I/O Circuits

- TX PLL
- TX Clock Distribution
- CDR
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs
  - Global PLL requires RX clock distribution to individual channels
Phase Interpolator (PI) Based CDR

- Frequency synthesis loop produces multiple clock phases used by the phase interpolators.
- Phase interpolator mixes between input phases to produce a fine sampling phase.
  - Ex: Quadrature 90° PI inputs with 5 bit resolution provides sampling phases spaced by $90°/(2^5-1)=2.9°$
- Digital phase tracking loop offers advantages in robustness, area, and flexibility to easily reprogram loop parameters.

[Hsieh]
Phase Interpolator (PI) Based CDR

- Frequency synthesis loop can be a global PLL

- Can be difficult to distribute multiple phases long distance
  - Need to preserve phase spacing
  - Clock distribution power increases with phase number
  - If CDR needs more than 4 phases consider local phase generation
DLL Local Phase Generation

- Only differential clock is distributed from global PLL.
- Delay-Locked Loop (DLL) locally generates the multiple clock phases for the phase interpolators.
  - DLL can be per-channel or shared by a small number (4).
- Same architecture can be used in a forwarded-clock system.
  - Replace frequency synthesis PLL with forwarded-clock signals.

Diagram:

- ¼ Rate Dual-Loop CDR
- Frequency Synthesis PLL
- Local DLL
- 4:1 MUX
- RX
- Phase-Recovery Loop
- 10Gb/s
- FSM
Phase Rotator PLL

- Phase interpolators can be expensive in terms of power and area
- Phase rotator PLL places one interpolator in PLL feedback to adjust all VCO output phases simultaneously
- Now frequency synthesis and phase recovery loops are coupled
  - Need PLL bandwidth greater than phase loop
    - Useful in filtering VCO noise
Phase Interpolators

- Phase interpolators realize digital-to-phase conversion (DPC)
- Produce an output clock that is a weighted sum of two input clock phases
- Common circuit structures
  - Tail current summation interpolation
  - Voltage-mode interpolation
- Interpolator code mapping techniques
  - Sinusoidal
  - Linear

[Weinlader]
Sinusoidal Phase Interpolation

- Arbitrary phase shift can be generated with linear summation of I/Q clock signal

\[ X_I = A \sin(\omega t) \]
\[ X_Q = A \sin(\omega t - \pi / 2) = -A \cos(\omega t) \]
\[ Y = A \sin(\omega t - \phi) \]
\[ = A \cos(\phi) \sin(\omega t) - A \sin(\phi) \cos(\omega t) \quad \left(0 \leq \phi \leq \frac{\pi}{2}\right) \]
\[ = \cos(\phi)X_I + \sin(\phi)X_Q = a_1X_I + a_2X_Q \]

where \( a_1 = \cos(\phi) \) and \( a_2 = \sin(\phi) \)

\[ a_1^2 + a_2^2 = 1 \]
Sinusoidal vs Linear Phase Interpolation

- It can be difficult to generate a circuit that implements sinusoidal weighting:
  \[ a_1^2 + a_2^2 = 1 \]
- In practice, a linear weighting is often used:
  \[ a_1 + a_2 = 1 \]
Phase Interpolator Model

- Interpolation linearity is a function of the phase spacing, $\Delta t$, to output time constant, $RC$, ratio.
Phase Interpolator Model

\[
V_o(t) = V_{cc} + R \cdot I \cdot \left[ (1 - \alpha) \cdot u(t) \cdot \left( e^{\frac{-t}{RC}} - 1 \right) + \alpha \cdot u(t - \Delta t) \cdot \left( e^{\frac{-t-\Delta t}{RC}} - 1 \right) \right]
\]

w/ ideal step inputs:

w/ finite input transition time:

\[
V_o(t) = V_{cc} + (1 - \alpha) \cdot \frac{I_{max} \cdot t}{\Delta t} \cdot R \cdot \alpha \cdot [u(t) - u(t - \Delta t)] \cdot \left( e^{\frac{t}{RC}} - 1 \right) + \\
\alpha \cdot \frac{I_{max} \cdot t}{\tau_r} \cdot R \cdot [u(t - \Delta t) - u(t - 3\Delta t)] \cdot \left( e^{\frac{-t-\Delta t}{RC}} - 1 \right).
\]

For more details see D. Weinlader’s Stanford PhD thesis
Tail-Current Summation PI

[Bulzacchelli JSSC 2006]

• For linearity over a wide frequency range, important to control either input or output time constant (slew rate)
For linearity over a wide frequency range, important to control either input or output time constant (slew rate)
Delay-Locked Loop (DLL)

- DLLs lock delay of a voltage-controlled delay line (VCDL)
- Typically lock the delay to 1 or $\frac{1}{2}$ input clock cycles
  - If locking to $\frac{1}{2}$ clock cycle the DLL is sensitive to clock duty cycle
- DLL does not self-generate the output clock, only delays the input clock

[Sidiropoulos JSSC 1997]
Voltage-Controlled Delay Line

[Sidiropoulos]
Delay-Locked Loop (DLL)

- First-order loop as delay line doesn’t introduce a pole
- VCDL doesn’t accumulate jitter like a VCO
- DLL doesn’t filter input jitter

\[
D_O(s) = (D_I(s) - D_O(s)) \cdot F_{REF} \cdot \frac{I_{CH}}{sC_1} \cdot K_{DL}
\]

\[
\frac{D_O(s)}{D_I(s)} = \frac{1}{1 + s/\omega_N}
\]

\[
\omega_N = I_{CH} \cdot K_{DL} \cdot F_{REF} \cdot \frac{1}{C_1}
\]

[Maneatis JSSC 1996]
CDR Jitter Properties

• Jitter Transfer

• Jitter Generation

• Jitter Tolerance
CDR Jitter Model

\[ \frac{\phi_{out}}{\phi_{in}} = \frac{s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}{s^2 + s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}} \]

\[ K_P = I_C \cdot R \quad K_i = \frac{I_C}{C} \quad \omega_n = \sqrt{K_i \cdot K_{PD} \cdot K_{VCO}} \quad \zeta = \frac{K_P}{K_i} \cdot \frac{\omega_n}{2} \]

[Lee]
Jitter transfer is how much input jitter “transfers” to the output.

If the PLL has any peaking in the phase transfer function, this jitter can actually be amplified.

\[
\frac{\phi_{out}}{\phi_{in}} = \frac{s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}{s^2 + s \cdot K_P \cdot K_{PD} \cdot K_{VCO} + K_i \cdot K_{PD} \cdot K_{VCO}}
\]

[Lee]
Jitter Transfer Measurement

\[ JTF(f) = 20\log\left(\frac{OutputJitter(f)}{InputJitter(f)}\right) \]

[TrV89] [RaO91] [Walker]
Jitter Transfer Specification

This specification is intended to control jitter peaking in long repeater chains.
Jitter Generation

• Jitter generation is how much jitter the CDR “generates”
  • Assumed to be dominated by VCO
  • Assumes jitter-free serial data input

VCO Phase Noise:

\[ H_{nyco}(s) = \frac{\phi_{out}}{\phi_{nyco}} = \frac{s^2}{s^2 + \left( \frac{K_{Loop}}{N} \right) RC s + \frac{K_{Loop}}{N}} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]

For CDR, N should be 1
Jitter Generation

High-Pass Transfer Function

\[ 20 \log_{10} \left| \frac{\theta_{\text{out}}(s)}{\theta_{\text{vcon}}(s)} \right| \]

\[ \text{Gain [dB]} \]

\[ \text{Frequency [GHz]} \]

Jitter accumulates up to time \( \propto \frac{1}{\text{PLL bandwidth}} \)

SONET specification:
- rms output jitter \( \leq 0.01 \) UI

[McNeill]
Jitter Tolerance

- How much sinusoidal jitter can the CDR “tolerate” and still achieve a given BER?

\[ \phi_e = (1 - \frac{\phi_{out}}{\phi_{in}}) \cdot \phi_{n.in} = \frac{TM}{2} \]

\[ JTOL(s) = 2 \cdot \phi_{n.in} = \frac{TM}{(1 - \frac{\phi_{out}}{\phi_{in}})} \]

[Sheikholeslami] [Lee]
Jitter Tolerance Measurement

Signal Generator

Noisy Clock

Delay Ctrl

Random Noise (RJ)

Sine (SJ)

Tyco Backplane (DJ)

Differential PRBS Data

Test Chip

16 Bit PRBS Error Count

[Lee]
Jitter Tolerance Measurement

[Diagram showing a graph with frequency on the x-axis and peak-to-peak jitter $U_{pp}$ on the y-axis. The graph indicates tracking and pass/fail regions with arrows and labels:]

- Tracking
- Pass
- Fail
- Margin Testing

[Reference: Lee]
Injection Locking Oscillation

Jie Zou

The Analog & Mixed Signal Center
Texas A&M University
Injection Locking in LC Tanks

a) a free-running oscillator consisting of an ideal positive feedback amplifier and an LC tank;

b) we insert a phase shift in the loop. We know this will cause the oscillation frequency to shift since the loop gain has to have exactly $2\pi$ phase shift (or multiples).
Phase Shift for Injected Signal

- Assume the oscillator “locks” onto the injected current and oscillates at the same frequency.

- Since the locking signal is not in general at the resonant center frequency, the tank introduces a phase shift.

- In order for the oscillator loop gain to be equal to unity with zero phase shift, the sum of the current of the transistor and the injected currents must have the proper phase shift to compensate for the tank phase shift.
Injection Locked Oscillator Phasors

Note that the frequency of the injection signal determines the extra phase shift $\Phi_0$ of the tank. This is fixed by the frequency offset.

- The current from the transistor is fed by the tank voltage, which by definition the tank current times the tank impedance, which introduces $\Phi_0$ between the tank current/voltage.
- The angle between the injected current and the oscillator current $\theta$ must be such that their sum aligns with the tank current.
The geometry of the problem implies the following constraints on the injected current amplitude relative to the oscillation amplitude: 

\[
\sin \phi_0 = \frac{B}{I_{tank}} \\
\cos(\pi/2 - \theta) = \sin(\theta) = \frac{B}{I_{inj}} \\
\sin \phi_0 = \frac{I_{inj}}{I_{tank}} \sin(\theta) \\
\sin \phi_0 = \frac{I_{inj} \sin(\theta)}{|I_{osc}e^{j\theta} + I_{inj}|} = \frac{I_{inj} \sin(\theta)}{\sqrt{I_{osc}^2 + I_{inj}^2 + 2 \cos \theta I_{osc} I_{inj}}} \\
\]
Locking Range

\[
\sin \phi_0 = \frac{I_{inj}}{I_T} \sin \theta = \frac{I_{inj} \sin \theta}{\sqrt{I_{osc}^2 + I_{inj}^2 + 2I_{osc}I_{inj} \cos \theta}}
\]

\[
\Rightarrow \sin \phi_{0,max} = \frac{I_{inj}}{I_{osc}}, \text{if } \cos \theta = -\frac{I_{inj}}{I_{osc}}
\]

A second-order parallel tank consisting of L, C, Rp exhibits a phase shift of:

\[
\phi_0 = \frac{\pi}{2} - \tan^{-1} \left( \frac{L \cdot \omega}{R_p} \cdot \frac{\omega_0^2}{\omega_0^2 - \omega^2} \right)
\]

\[
\therefore \omega_0^2 - \omega^2 \approx 2\omega_0(\omega_0 - \omega), \quad \frac{L \cdot \omega}{R_p} = \frac{1}{Q} \cdot \frac{\pi}{2} - \tan^{-1}(x) = \tan^{-1}(x^{-1})
\]

\[
\therefore \tan \phi_0 \approx \frac{2Q}{\omega_0}(\omega_0 - \omega)
\]

\[
\therefore \tan \phi_0 = \frac{I_{inj}}{I_T}, I_T = \sqrt{I_{osc}^2 - I_{inj}^2}
\]

At the edge of the lock range, the injected current is orthogonal to the tank current.

The phase angle between the injected current and the oscillator is \(90^\circ + \Phi_{0,max}\)

Source: Razavi
Locking Range

\[ \Rightarrow \frac{I_{\text{inj}}}{I_T} \approx \frac{2Q}{\omega_0} (\omega_0 - \omega) \]

\[ \frac{I_{\text{inj}} \cdot I_{\text{osc}}}{I_{\text{osc}} \cdot I_T} = \frac{I_{\text{inj}}}{I_{\text{osc}}} \cdot \frac{1}{\sqrt{1 - \frac{I_{\text{inj}}^2}{I_{\text{osc}}^2}}} \]

\[ \Rightarrow \frac{I_{\text{inj}}}{I_{\text{osc}}} \cdot \frac{1}{\sqrt{1 - \frac{I_{\text{inj}}^2}{I_{\text{osc}}^2}}} \approx \frac{2Q}{\omega_0} (\omega_0 - \omega) \]

\[ \Rightarrow \omega_0 - \omega_{\text{inj}} \approx \frac{\omega_0}{2Q} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \cdot \frac{1}{\sqrt{1 - \frac{I_{\text{inj}}^2}{I_{\text{osc}}^2}}} \]

\[ I_{\text{inj}} \ll I_{\text{osc}} \]

\[ \omega_{\Delta,L} = \omega_0 - \omega_{\text{inj}} \approx \frac{\omega_0}{2Q} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \]

When: \( \omega_0 = 10\text{GHz}, Q = 5, K = \frac{I_{\text{inj}}}{I_{\text{osc}}} = 0.1 \)

\[ \Rightarrow \omega_{\Delta,L} \approx 100\text{MHz} \]
The digitally controlled switch-capacitor bank tunes the free-running frequency of DCO to adjust the phase of the forwarded clock and also compensate for PVT.

Next Time

- Optical I/O