Announcements

• Project Preliminary Report #1 due now
• Exam 2 is still April 30
• Reading
  • Posted clocking papers
  • Website additional links has PLL and jitter tutorials
• Majority of today’s material from Fischette tutorial and M. Mansuri’s PhD thesis (UCLA)
Agenda

• PLL noise transfer functions

• PLL circuits
Forward Clock I/O Circuits

- TX PLL
- TX Clock Distribution
- Replica TX Clock Driver
- Channel
- Forward Clock Amplifier
- RX Clock Distribution
- De-Skew Circuit
  - DLL/PI
  - Injection-Locked Oscillator
Embedded Clock I/O Circuits

- **TX PLL**
- **TX Clock Distribution**
- **CDR**
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs
  - Global PLL requires RX clock distribution to individual channels
Input Noise Transfer Function

Input Phase Noise:
\[ H_{\text{in}}(s) = \frac{\phi_{\text{out}}}{\phi_{\text{in}}} = \frac{K_{\text{Loop}} (RCs + 1)}{s^2 + \left( \frac{K_{\text{Loop}}}{N} \right) RCs + \frac{K_{\text{Loop}}}{N}} = \frac{N(2\zeta\omega_n s + \omega_n^2)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]

Voltage Noise on Input Clock Source:
\[ T_{\text{in}}(s) = \frac{\phi_{\text{out}}}{v_{\text{in}}} = \left( \frac{\phi_{\text{out}}}{\phi_{\text{in}}} \right) \left( \frac{K_o}{s} \right) = \frac{K_o K_{\text{Loop}} (RCs + 1)}{s \left( s^2 + \left( \frac{K_{\text{Loop}}}{N} \right) RCs + \frac{K_{\text{Loop}}}{N} \right)} \]
VCO Noise Transfer Function

VCO Phase Noise:

\[ H_{v_{VCO}}(s) = \frac{\phi_{out}}{\phi_{v_{VCO}}} = \frac{s^2}{s^2 + \left(\frac{K_{Loop}}{N}\right)RCs + \frac{K_{Loop}}{N}} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]

Voltage Noise on VCO Inputs:

\[ T_{v_{VCO}}(s) = \frac{\phi_{out}}{v_{v_{VCO}}} = \left(\frac{\phi_{out}}{\phi_{v_{VCO}}}\right)\left(\frac{K_{VCO}}{s}\right) = \frac{K_{VCO}s}{s^2 + \left(\frac{K_{Loop}}{N}\right)RCs + \frac{K_{Loop}}{N}} \]

\[ K_{VCO} \text{ is different if the input is at the } V_{cntrl} \text{ input (} K_{VCO} \text{) or supply (} K_{Vdd} \text{)} \]
Clock Buffer Noise Transfer Function

Output Phase Noise: \[ H_{nbuf}(s) = \frac{\phi_{out}}{\phi_{nbuf}} = \frac{s^2}{s^2 + \left(\frac{K_{Loop}}{N}\right)RCs + \frac{K_{Loop}}{N}} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]

Voltage Noise on Buffer Inputs:

\[ T_{nbuf}(s) = \frac{\phi_{out}}{v_{nbuf}} = \left(\frac{\phi_{out}}{\phi_{nbuf}}\right) \left(\frac{K_{delay}\omega_{VCO}}{s + \frac{K_{delay}\omega_{VCO}}{\omega_{buf}} + 1} + 1\right) \approx \frac{K_{delay}\omega_{VCO}s^2}{s^2 + \left(\frac{K_{Loop}}{N}\right)RCs + \frac{K_{Loop}}{N}} \]
Noise Transfer Functions

- Input phase noise (N=1) (low-pass)
- Input clock noise
- VCO input voltage noise (band-pass)
- VCO noise (b)
- Clock buffer noise (c)
- Buffer phase or voltage noise (high-pass)
Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider
Phase Detector

- Detects phase difference between feedback clock and reference clock
- The loop filter will filter the phase detector output, thus to characterize phase detector gain, extract average output voltage (or current for charge-pump PLLs)
- Can be analog or digital

\[ \text{avg}\{V_e(t)\} = K_{PD} \Delta \phi \]
Analog Multiplier Phase Detector

If $\omega_1 = \omega_2$ and filtering out high-frequency term

$$y(t) = \frac{\alpha A_1 A_2}{2} \cos([\omega_1 + \omega_2]t + \Delta \phi) + \frac{\alpha A_1 A_2}{2} \cos([\omega_1 - \omega_2]t - \Delta \phi)$$

$\alpha$ is mixer gain

- **If $\omega_1 = \omega_2$** and filtering out high-frequency term

$$\overline{y(t)} = \frac{\alpha A_1 A_2}{2} \cos \Delta \phi$$

- **Near $\Delta \phi$ lock region of $\pi/2$**:

$$\overline{y(t)} \approx \frac{\alpha A_1 A_2}{2} \left( \frac{\pi}{2} - \Delta \phi \right)$$

$K_{PD} = -\frac{\alpha A_1 A_2}{2}$

[Razavi]
XOR Phase Detector

- Sensitive to clock duty cycle
XOR Phase Detector

For \(-\pi < \Phi_{\text{ref}} - \Phi_{\text{div}} < 0\):

\[
W = -\left(\frac{\Phi_{\text{ref}} - \Phi_{\text{div}}}{\pi}\right)\frac{T}{2}
\]

For \(0 < \Phi_{\text{ref}} - \Phi_{\text{div}} < \pi\):

\[
W = \left(\frac{\Phi_{\text{ref}} - \Phi_{\text{div}}}{\pi}\right)\frac{T}{2}
\]

The average value of \(e(t)\) is:

\[
\text{avg}\{e(t)\}
\]

Gain = \(-\frac{2}{\pi}\) for \(-\pi < \Phi_{\text{ref}} - \Phi_{\text{div}} < 0\)

Gain = \(\frac{2}{\pi}\) for \(0 < \Phi_{\text{ref}} - \Phi_{\text{div}} < \pi\)

Phase detector range = \(\pi\)

[Perrott]
Cycle Slipping

- If there is a frequency difference between the input reference and PLL feedback signals the phase detector can jump between regions of different gain
  - PLL is no longer acting as a linear system

[Perrott]
Cycle Slipping

- If frequency difference is too large the PLL may not lock
Phase Frequency Detector (PFD)

- Phase Frequency Detector allows for wide frequency locking range, potentially entire VCO tuning range
- 3-stage operation with UP and DOWN outputs
- Edge-triggered results in duty cycle insensitivity
PFD Transfer Characteristic

UP=1 & DN=-1

- Constant slope and polarity asymmetry about zero phase allows for wide frequency range operation

Gain = $1/(2\pi)$

Phase detector range = $4\pi$
PFD Deadzone

- If phase error is small, then short output pulses are produced by PFD
- Cannot effectively propagate these pulses to switch charge pump
- Results in phase detector “dead zone” which causes low loop gain and increased jitter
- Solution is to add delay in PFD reset path to force a minimum UP and DOWN pulse length

[Fischette]
PFD Operation

Ref

FbClk

GoFaster

GoSlower

Vctl

Min. Pulse Width

Cycle Slip
Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider
Charge Pump

- Converts PFD output signals to charge
- Charge is proportional to PFD pulse widths

**PFD-CP Gain:** \( \left( \frac{1}{2\pi} \right) I_{CP} \)
Simple Charge Pump

- Issues
  - Switch resistance can vary Vctrl due to body effect
  - Charge injection from switches onto Vctrl
  - Charge sharing between current source drain nodes and Vctrl

[Razavi]
Charge Pump Mismatch

- PLL will lock with static phase error
- Extra "ripple" on Vctrl
  - Results in frequency domain spurs at the reference clock frequency offset from the carrier

[Razavi]
Charge Pump w/ Improved Matching

- Amplifier keeps current source Vds voltages constant, resulting in reduced transient current mismatch

[Young J SSC 1992]
Charge Pump w/ Reversed Switches

- Swapping switches reduces charge injection
  - MOS caps (Md1-4) provide extra charge injection cancellation

- Helper transistors Mx and My quickly turn-off current source

- Dummy brand helps to match PFD loading

[Ingino JSSC 2001]
Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider
• Lowpass filter extracts average of phase detector error pulses
Loop Filter Transfer Function

- Neglecting secondary capacitor, $C_2$

\[
F(s) = \frac{V_c(s)}{I_e(s)} = \frac{R \left( s + \frac{1}{RC_1} \right)}{s}
\]

VCO Control Voltage

[Diagram of the circuit with $C_1$, $R$, and $C_2$]
Loop Filter Transfer Function

- With secondary capacitor, $C_2$

\[ Z(s) = \frac{1}{C_2} \left( s + \frac{1}{RC_1} \right) \frac{s}{s(C_1 + C_2)} + \frac{1}{RC_1 C_2} \]

![Diagram of the loop filter with secondary capacitor $C_2$](image)

- Pole at 0Hz
- Zero at $f = \frac{1}{2\pi RC_1} = 80.5\text{kHz}$
- Second Pole at $f = \frac{C_1 + C_2}{2\pi RC_1 C_2} = 915\text{kHz}$
Why have C2?

- Secondary capacitor smoothes control voltage ripple
- Can’t make too big or loop will go unstable
  - $C_2 < C_1/10$ for stability
  - $C_2 > C_1/50$ for low jitter

![PLL Synthesizing a 380MHz Signal](image)

**Control Voltage Ripple**
Filter Capacitors

• To minimize area, we would like to use highest density caps

• Thin oxide MOS cap gate leakage can be an issue
  • Similar to adding a non-linear parallel resistor to the capacitor
  • Leakage is voltage and temperature dependent
  • Will result in excess phase noise and spurs

• Metal caps or thick oxide caps are a better choice
  • Trade-off is area

• Metal cap density can be < 1/10 thin oxide caps

• Filter cap frequency response can be relatively low, as PLL loop bandwidths are typically 1-50MHz
Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider
Voltage-Controlled Oscillator

\[\omega_{\text{out}}(t) = \omega_0 + \Delta \omega_{\text{out}}(t) = \omega_0 + K_{\text{VCO}}v_c(t)\]

- Time-domain phase relationship

\[\theta_{\text{out}}(t) = \int \Delta \omega_{\text{out}}(t) \, dt = K_{\text{VCO}} \int v_c(t) \, dt\]
Voltage-Controlled Oscillators (VCO)

- **Ring Oscillator**
  - Easy to integrate
  - Wide tuning range (5x)
  - Higher phase noise

- **LC Oscillator**
  - Large area
  - Narrow tuning range (20-30%)
  - Lower phase noise
Barkhausen’s Oscillation Criteria

Closed-loop transfer function:

\[
\frac{H(j\omega)}{1-H(j\omega)}
\]

- Sustained oscillation occurs if \( H(j\omega) = 1 \)

- 2 conditions:
  - Gain = 1 at oscillation frequency \( \omega_0 \)
  - Total phase shift around loop is \( n360^\circ \) at oscillation frequency \( \omega_0 \)

[Sanchez]
Ring Oscillator Example

Three-stage ring oscillator

\[ H(s) = -\frac{A_0^3}{\left(1 + \frac{s}{\omega_0}\right)^3} \]

\[ \omega_{osc} = \sqrt{3}\omega_0 \]

\[ \tan^{-1} \frac{\omega_{osc}}{\omega_o} = 60^\circ \]

\[ \frac{V_{out}(s)}{V_{in}(s)} = \frac{-A_0^3}{\left(1 + \frac{s}{\omega_0}\right)^3} = \frac{-A_0^3}{\left(1 + \frac{s}{\omega_0}\right)^3 + A_0^3} \]

\[ \left[ \frac{A_0^3}{\sqrt{1 + \left(\frac{\omega_{osc}}{\omega_0}\right)^2}} \right]^3 = 1 \]

\[ A_0 = 2 \]
Ring Oscillator Example

- 4-stage oscillator
  - $A_0 = \sqrt{2}$
  - Phase shift = 45

- Easier to make a larger-stage oscillator oscillate, as it requires less gain and phase shift per stage

\[ H(s) = -\frac{A_0^3}{\left(1 + \frac{s}{\omega_0}\right)^3} \]
\[ \omega_{osc} = \sqrt{3}\omega_0 \]
\[ \tan^{-1}\left(\frac{\omega_{osc}}{\omega_0}\right) = 60^\circ \]

\[ \frac{V_{out}(s)}{V_{in}(s)} = \frac{-A_0^3}{\left(1 + \frac{s}{\omega_0}\right)^3} = \frac{-A_0^3}{\left(\frac{\omega_{osc}}{\omega_0}\right)^3 + A_0^2} \]

\[ \frac{A_0^3}{\sqrt{1 + \left(\frac{\omega_{osc}}{\omega_0}\right)^2}} = 1 \]

$A_0 = 2$

[Sanchez]
Next Time

- PLL wrap-up
- CDRs