Announcements

• Project Preliminary Report #1 due April 16 (in class)

• Exam 2 is April 30

• Reading
  • Posted clocking papers
  • Website additional links has PLL and jitter tutorials

• Majority of today’s material from Fischette tutorial and M. Mansuri’s PhD thesis (UCLA)
Agenda

• PLL modeling
Introduction

• A phase-locked loop (PLL) is a negative feedback system where an oscillator-generated signal is phase AND frequency locked to a reference signal

• PLLs applications
  • Frequency synthesis
    • Multiplying a 100MHz reference clock to 10GHz
  • Skew cancellation
    • Phase aligning an internal clock to an I/O clock
  • Clock recovery
    • Extract from incoming data stream the clock frequency and optimum phase of high-speed sampling clocks
  • Modulation/De-modulation
    • Wireless systems
    • Spread-spectrum clocking
PLL Block Diagram

\[ \phi_{\text{ref}}, \; CK_{\text{ref}} \]

Phase Detector

error

Low-Pass Filter

Oscillator

\[ \phi_{\text{out}}, \; CK_{\text{out}} \]

\[ \phi_{\text{feedback}}, \; CK_{\text{feedback}} \]

Frequency Divider: \( N \)

[Mansuri]
Linear PLL Model

\[ \theta_{\text{ref}} + \sum \theta_{e} \rightarrow K_{\text{PD}} \rightarrow F(s) \rightarrow \frac{K_{\text{VCO}}}{s} \rightarrow \theta_{\text{out}} \]

- **Phase Detector**
- **Loop Filter**
- **VCO**
- **Loop Divider**
Understanding PLL Frequency Response

- Linear “small-signal” analysis is useful for understand PLL dynamics if
  - PLL is locked (or near lock)
  - Input phase deviation amplitude is small enough to maintain operation in lock range
- Frequency domain analysis can tell us how well the PLL tracks the input phase as it changes at a certain frequency
- PLL transfer function is different depending on which point in the loop the output is responding to
Phase Detector

- Detects phase difference between feedback clock and reference clock
- The loop filter will filter the phase detector output, thus to characterize phase detector gain, extract average output voltage (or current for charge-pump PLLs)

\[
\text{avg}\{V_e(t)\} = K_{PD} \Delta \phi
\]
Loop Filter

- Lowpass filter extracts average of phase detector error pulses

![Diagram of loop filter with components labeled VDD, VSS, C1, C2, R, and F(s).]
Voltage-Controlled Oscillator

\[ \omega_{out}(t) = \omega_0 + \Delta \omega_{out}(t) = \omega_0 + K_{VCO} v_c(t) \]

- Time-domain phase relationship

\[ \theta_{out}(t) = \int \Delta \omega_{out}(t) dt = K_{VCO} \int v_c(t) dt \]

Laplace Domain Model
Loop Divider

- Time-domain model

\[ \omega_{fb}(t) = \frac{1}{N} \omega_{out}(t) \]

\[ \theta_{fb}(t) = \int \frac{1}{N} \omega_{out}(t) \, dt = \frac{1}{N} \theta_{out}(t) \]
Linear PLL Model

\[ \theta_{ref} \rightarrow + \rightarrow \sum \rightarrow K_{PD} \rightarrow F(s) \rightarrow K_{VCO} \frac{1}{s} \rightarrow \theta_{out} \]

- **Phase Detector**
- **Loop Filter**
- **VCO**

\[ \theta_{e} \]

\[ \theta_{fb} \]

\[ \frac{1}{N} \]

**Loop Divider**
Charge-Pump PLL Linear Model

- Charge-pump supplies current to loop filter capacitor which integrates it to produce the VCO control voltage.
- For stability, a zero is added with the resistor which gives a proportional gain term.

[Mansuri]
Open-Loop PLL Transfer Function

\[ H_{\text{open}}(s) = K_{PFD} \cdot \frac{I_{CP}}{2\pi} \cdot F(s) \cdot K_{VCO}/s \]

ignoring \( C_1 \):

\[ H_{\text{open}}(s) = K_{PFD} \cdot \frac{I_{CP}}{2\pi \cdot C_{CP}} \cdot (1 + RC_{CP}s) \cdot \frac{K_{VCO}}{s^2} \]

with \( C_1 \):

\[ H_{\text{open}}(s) = K_{PFD} \cdot \frac{I_{CP}}{2\pi \cdot (C_{CP} + C_1)} \cdot (1 + RC_{CP}s) \cdot \frac{K_{VCO}}{s^2 \cdot [1 + R(C_{CP}\parallel C_1)s]} \]
Open-Loop PLL Transfer Function

with $C_1$ (2$^{nd}$ order)

$|H_{\text{open}}(s)| \cdot \frac{1}{N}$

$40\text{dB/dec}$

$0\text{dB}$

$\omega_Z$ $\omega_C$

$\angle H_{\text{open}}(s)$

$-90^\circ$

$-180^\circ$

with $C_1$ (3$^{rd}$ order)

$|H_{\text{open}}(s)| \cdot \frac{1}{N}$

$40\text{dB/dec}$

$0\text{dB}$

$\omega_Z$ $\omega_C$ $\omega_{p3}$

$\angle H_{\text{open}}(s)$

$-90^\circ$

$-180^\circ$

[Mansuri]
Closed-Loop PLL Transfer Function

\[
\frac{\phi_{out}(s)}{\phi_{in}} = H_{closed}(s) = \frac{H_{open}(s)}{1 + H_{open}(s) \cdot 1/N}
\]

ignoring \(C_1\):

\[
\frac{\phi_{out}(s)}{\phi_{in}} = \frac{K_{Loop} \cdot (1 + RC_{CP}s)}{s^2 + (K_{Loop}/N)RC_{CP}s + K_{Loop}/N}
\]

\[
K_{Loop} = K_{PFD} \cdot K_{VCO} \cdot I_{CP}/(2\pi C_{CP})
\]
PLL Natural Frequency and Damping Factor

\[
\frac{\phi_{out}(s)}{\phi_{in}} = \frac{K_{Loop} \cdot (1 + RC_{CPS}s)}{s^2 + (K_{Loop}/N)RC_{CPS}s + K_{Loop}/N}
\]

Standard 2\textsuperscript{nd}-order denominator: \( s^2 + 2\zeta\omega_n s + \omega_n^2 \)

Natural Frequency: \( \omega_n = \sqrt{\frac{K_{Loop}}{N}} \)

Damping Factor: \( \zeta = \frac{\omega_n}{2 \cdot \omega_z} \)

Loop Bandwidth: \( \omega_{3dB} = \omega_n \left(a + \sqrt{a^2 + 1}\right)^{1/2} \)

\[
a = 2\zeta^2 + 1 - \frac{\omega_n N}{K_{PD}K_{VCO}} \left(4\zeta - \frac{\omega_n N}{K_{PD}K_{VCO}} \right)
\]
Damping Factor Impact

- If damping factor is too low, frequency peaking occurs
  - Damping factor ~1 is usually preferred
- Excessively high damping also causes peaking
  - Need 3rd order model to observe this

[Fischette]
Damping Factor Impact

• Peaking in frequency domain leads to ringing in the time domain
PLL Noise Transfer Function

[Mansuri]
Noise Transfer Functions

![Graph showing noise transfer functions with labels: Input clock noise (a), VCO noise (b), Clock buffer noise (c). The x-axis represents frequency in Hz on a logarithmic scale, and the y-axis represents noise transfer function in dB.](Mansuri)
Next Time

- PLL modeling
- PLL circuits