Lecture 14: Clock Distribution Techniques

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Agenda

• Clock distribution in serial I/O systems
• Wire scaling
• Clock distribution techniques
  • Inverter Chain
  • CML Chain
  • Transmission Line
  • Inductive Load
  • Capacitively Driven Wires
• CML2CMOS converters
• On-die global clock distribution is necessary in multi-channel embedded and forwarded clock serial link systems
VLSI Interconnect (Wires)

Loose pitch + thick metal on upper layers
- High speed global wires
- Low resistance power grid

Tight pitch on lower layers
- Maximum density for local interconnects

[Bohr ISSCC 2009]
Wire Scaling

- Ideally, we scale everything by 0.7x when we move to a more advanced technology node for 2x density.
- Results in 2x wire resistance, which dramatically increases wire RC delay.
  - To compensate, resistance wires get taller.
- Cap grows at a smaller pace with scaling.
  - Taller wires increase sidewall cap.
  - Improved (low-k) dielectrics help reduce cap.
Wire Scaling - Delay

- Global on-chip wire RC delay becomes many (100+) gate delays (if driven with one lumped driver)

[Ho Proc. IEEE 2001]
Limited Wire Bandwidth

• Global on-chip wire bandwidth is much worse than chip-to-chip channels

• RC-dominated on-chip wires vs (R)LC-dominated off-chip wires
Clock Distribution Techniques

- Clock distribution techniques are typically compared in regards to jitter, delay, and power

- Techniques
  - Inverter Chain
  - CML Chain
  - Transmission Line
  - Inductive Load
  - Capacitively Driven Wires
Inverter Chain Distribution

- Instead of driving the long low-bandwidth wire with one huge inverter, break wire up into N segments driven by N inverters
Elmore Delay of Inverter Chain Distribution

\[ t_p = N \left[ 0.69 R_{eq} c_o + \left( 0.69 R_{eq} + 0.38 \frac{R_w L}{N} \right) \frac{C_w L}{N} + 0.69 \left( \frac{R_{eq}}{N} + \frac{R_w L}{N} \right) c_i \right] \]

\[ = N \left[ 0.69 \frac{R_{equ}}{m} mc_{ou} + \left( 0.69 \frac{R_{equ}}{m} + 0.38 \frac{R_w L}{N} \right) \frac{C_w L}{N} + 0.69 \left( \frac{R_{equ}}{m} + \frac{R_w L}{N} \right) mc_{iu} \right] \]

\[ = 0.69 NR_{equ} \left( c_{ou} + c_{iu} \right) + 0.38 \frac{R_w C_w L^2}{N} + 0.69 \frac{R_{equ} C_w L}{m} + 0.69 m R_w L c_{iu} \]

\( N \) = segment number
\( C_i, C_o, R_{eq} \) = inverter input cap, output cap, equivalent resistance
\( R_w, C_w \) = wire unit resistance and capacitance
\( L \) = wire length
\( C_{in}, C_{ou}, R_{equ} \) = unit inverter input cap, output cap, equivalent resistance
\( m \) = multiple factor of unit inverter

N FO1 inverter \( \tau_s \)
Inherent wire delay divided by \( N \) segments
RC of one inverter driving total wire cap
RC of wire driving one inverter
Elmore Delay of Inverter Chain Distribution

\[ N = \text{segment number} \]
\[ C_i, C_o, R_{eq} = \text{inverter input cap, output cap, equivalent resistance} \]
\[ R_w, C_w = \text{wire unit resistance and capacitance} \]
\[ L = \text{wire length} \]
\[ C_{iu}, C_{ou}, R_{eq} = \text{unit inverter input cap, output cap, equivalent resistance} \]
\[ m = \text{multiple factor of unit inverter} \]

\[ t_p = 0.69NR_{equ}(c_{ou} + c_{iu}) + 0.38 \frac{R_w C_w L^2}{N} + 0.69 \frac{R_{equ} C_w L}{m} + 0.69mR_w Lc_{iu} \]

For Minimum Propagation Delay

\[ N = 0.742L \sqrt{\frac{R_w C_w}{R_{equ}(c_{ou} + c_{iu})}} \quad \text{and} \quad m = \sqrt{\frac{R_{equ} C_w}{R_w c_{iu}}} \]
Delay and jitter are correlated, but don’t necessarily share the same minimum.

For 5mm wire in 90nm CMOS:
- Minimum jitter (36ps): N=3 and m=256
- Minimum delay (321ps): N=3 and m=128
- Minimum power: N=4 and m=64
CML Chain Distribution

- Relative to inverter-based buffers, low-swing CML buffers offer increased bandwidth and PSRR
- Same model used to analyze CML distribution

[Hu ISCAS 2009]
CML Chain Distribution
Delay, Jitter, and Power Trade-offs

- Analysis with $400 \text{mV}_{\text{ppd}}$ swing ($R=200\Omega$, $I_{\text{tail}}=1\text{mA}$)
- For 5mm wire in 90nm CMOS
  - Minimum jitter (0.5ps): $N=2$ and $m=8$
  - Minimum delay (182ps): $N=4$ and $m=8$
  - Minimum power: $N=2$ and $m=1$
- Much better jitter performance than inverter-based distribution
  - However, jitter amplification is not considered in this work
  - CML buffers may be more sensitive to input jitter than inverter-based
Transmission Line Distribution

- On-die transmission lines can be realized with wider than minimum-width wires
- DC resistance is small relative to characteristic impedance, i.e. distributed wire inductance has strong impact on wire delay
- Allows for “speed-of-light” propagation velocity
- Passive transmission line doesn’t introduce any jitter

[Hu I SCAS 2009]
On-Die Transmission Lines

• If signaling is strictly on-chip, have more freedom to choose differential impedance

• Larger impedance will allow for lower power, but there are limitations
  • Parasitic capacitance
  • DC resistance

• Because of this, many times the on-die transmission lines will display differential impedance close to the typical off-chip 100Ω value
Clock Swing Along Transmission Line

5mm Transmission Line
W=6\,\mu m, \, d=2.5\,\mu m, \, W_{gnd}=4\,\mu m, \, s=4\,\mu m
Zo=120\,\Omega \, \text{and} \, \text{RDC} = 42\,\Omega

- DC-loss of transmission lines causes reduction in the clock swing as it travels down the line
- For 5mm line, \, delay=43\,ps \, \text{and} \, \text{jitter}=0.18\,ps

[Hu I SCAS 2009]
Inductive Load Distribution

- Inductively-loaded wire can boost wire impedance by resonating with the wire capacitance at the clock frequency
  - Reduces power
  - Provides jitter filtering
- Cost is high inductor area, particularly at lower clock frequencies

[Hu ISCAS 2009]
Inductive Load Distribution

- For similar clock swing, inductive termination can offer significant power savings

<table>
<thead>
<tr>
<th>5GHz</th>
<th>Inductor Load</th>
<th>R Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vswing</td>
<td>500mV</td>
<td>538mV</td>
</tr>
<tr>
<td>Power</td>
<td>1.2mW</td>
<td>7.2mW</td>
</tr>
</tbody>
</table>
Capacitively Driven Wires Distribution

• Adding a capacitor in series to the pseudo-differential inverter-based drivers significantly reduces driver loading

[Hu ISCAS 2009]
Capacitively Driven Wires Model

\[ t_p = 0.69R_{eq}(c_o + c_{p1} + c_c) + 0.19R_wC_wL^2 \]

[Ho J SSC 2008]

[Distributed wire model]

[Single-pi model]

[Hu I SCAS 2009]
Capacitively Driven Wires Distribution

\[ t_p = 0.69 R_{eq} \left( c_o + c_{p1} + c_c \right) + 0.19 R_w C_w L^2 \]  

[Hu I SCAS 2009]

- Minimum series cap reduces delay and power, but swing also
- If cap is too small, increased jitter is observed
Clock Distribution Performance Comparison

<table>
<thead>
<tr>
<th>Technology</th>
<th>1.2V 90nm CMOS</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Methods (with optimal tradeoff)</td>
<td></td>
<td>jitter(ps)</td>
</tr>
<tr>
<td>Inverter chain (N=3, m=128)</td>
<td>36</td>
<td>321</td>
</tr>
<tr>
<td>CML chain (N=2, m=1)</td>
<td>1</td>
<td>221</td>
</tr>
<tr>
<td>Transmission line</td>
<td>0.18</td>
<td>43</td>
</tr>
<tr>
<td>Inductive load (L=6nH, Q=2)</td>
<td>0.42</td>
<td>55</td>
</tr>
<tr>
<td>CDW (Cc=50f)</td>
<td>1.98</td>
<td>116</td>
</tr>
</tbody>
</table>

• Transmission-line distribution offers best jitter and delay performance
• CDW offers minimum jitter-power and delay-power product
• Note, everything but inverter-chain distribution is low-swing
• If CML2CMOS converter is not designed well, that can kill your nice distribution network performance
CML2CMOS Converter (1)

- Differential input stage followed by high-swing output stage
- Can be sensitive to power-supply noise and reduce jitter benefits of low-swing distribution techniques
- Often require some type of duty-cycle control
AC-coupled self-biased inverter input stages and cross-coupled buffer stages can help improve duty cycle performance.