ECEN720: High-Speed Links Circuits and Systems Spring 2019

Lecture 14: Clock Distribution Techniques

Sam Palermo

Analog & Mixed-Signal Center

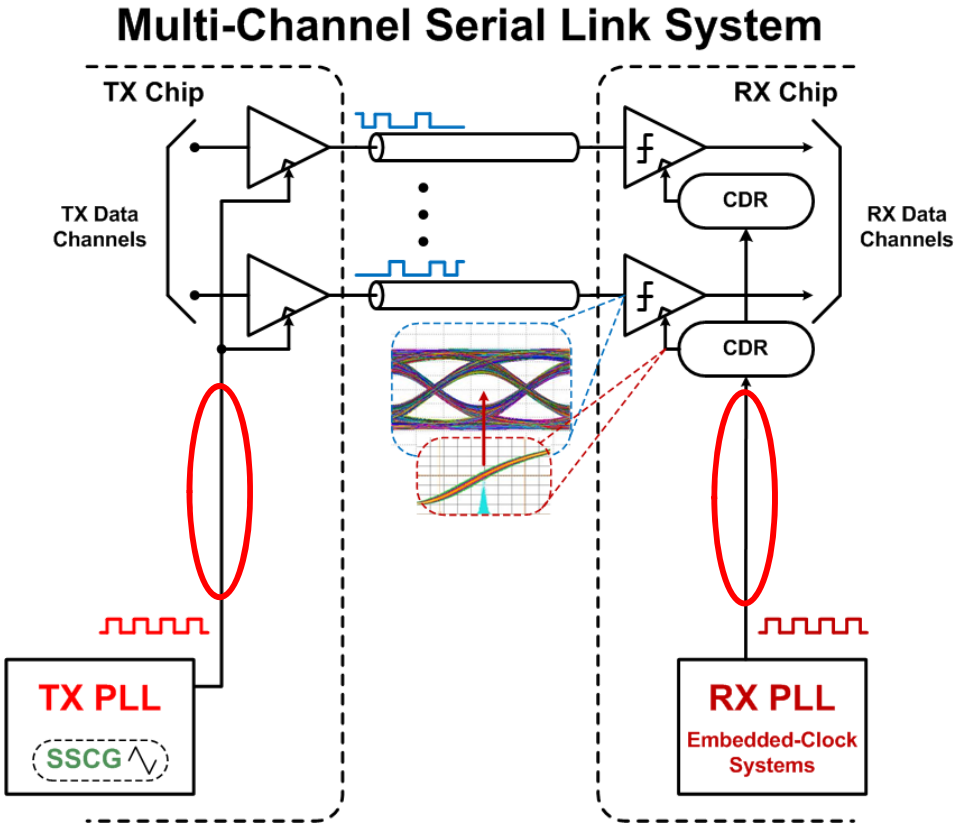
Texas A&M University

Agenda

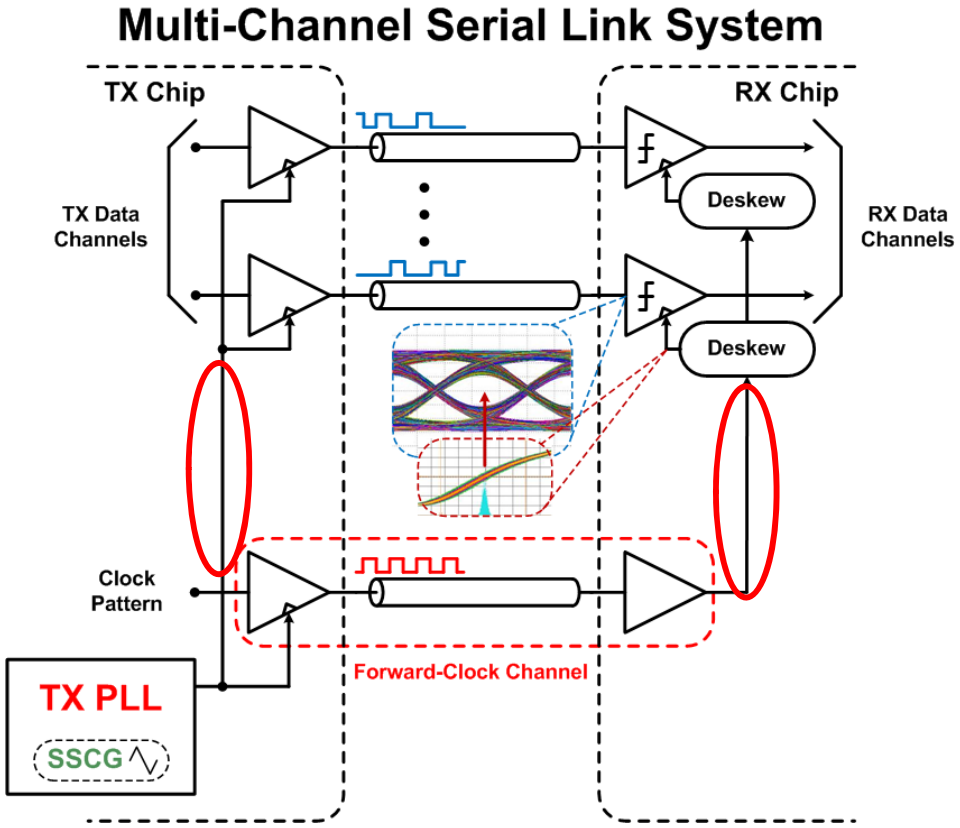
- Clock distribution in serial I/O systems
- Wire scaling
- Clock distribution techniques
  - Inverter Chain
  - CML Chain
  - Transmission Line
  - Inductive Load
  - Capacitively Driven Wires
- CML2CMOS converters

Clock Distribution in Serial I/O Systems

Embedded Clock System



Forwarded Clock System



- On-die global clock distribution is necessary in multi-channel embedded and fowarded clock serial link systems

VLSI Interconnect (Wires)

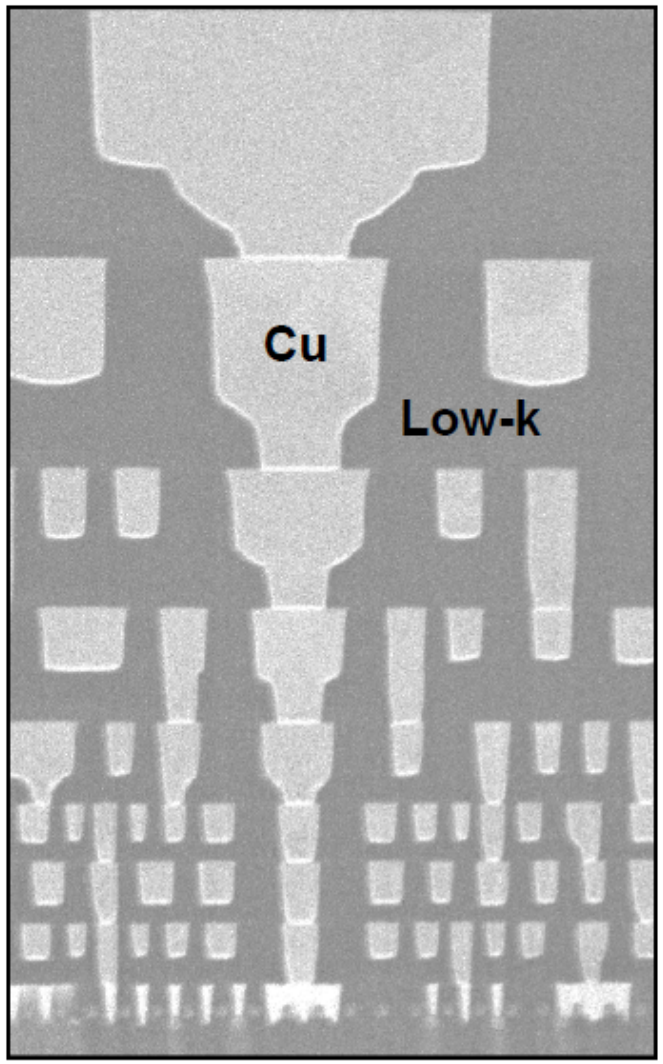
Loose pitch + thick metal on upper layers

- High speed global wires
- Low resistance power grid

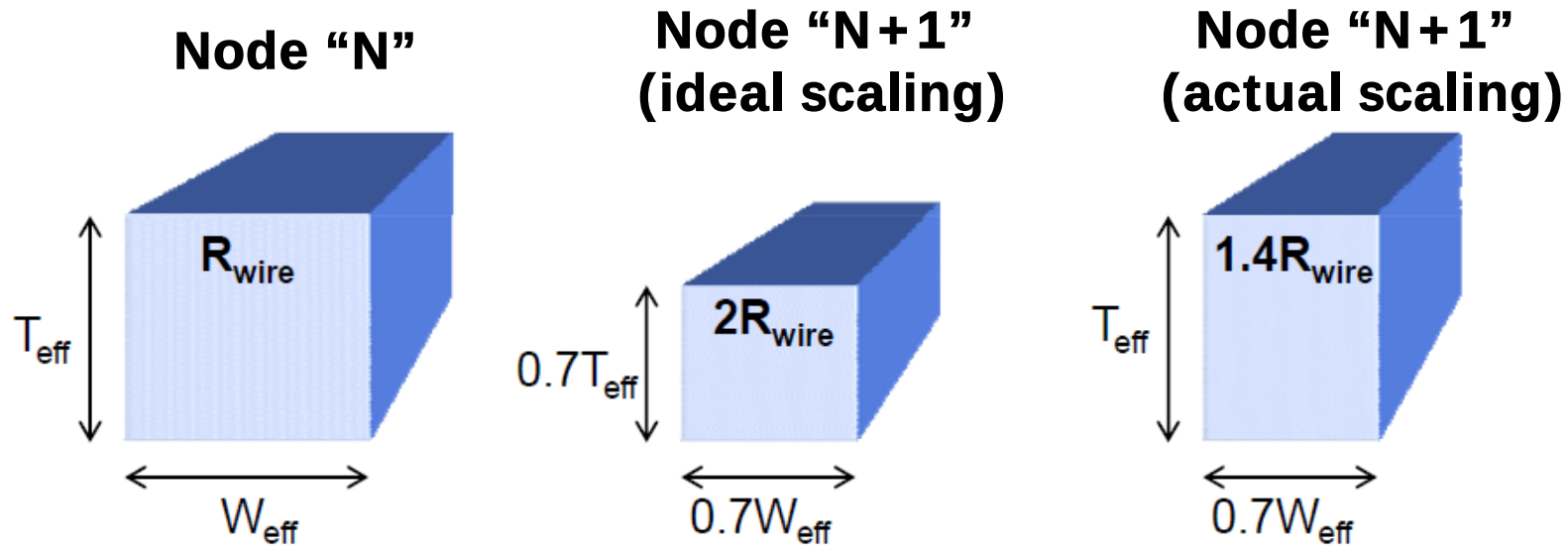
Tight pitch on lower layers

- Maximum density for local interconnects

[Bohr ISSCC 2009]



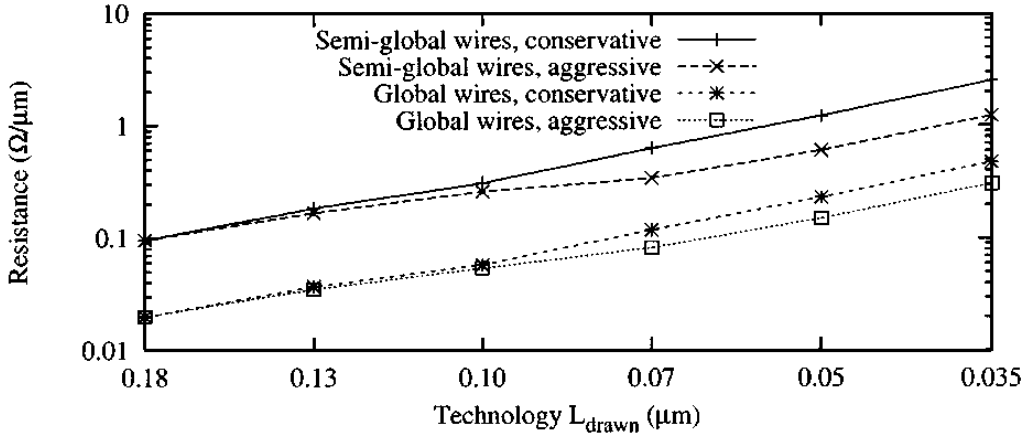
Wire Scaling

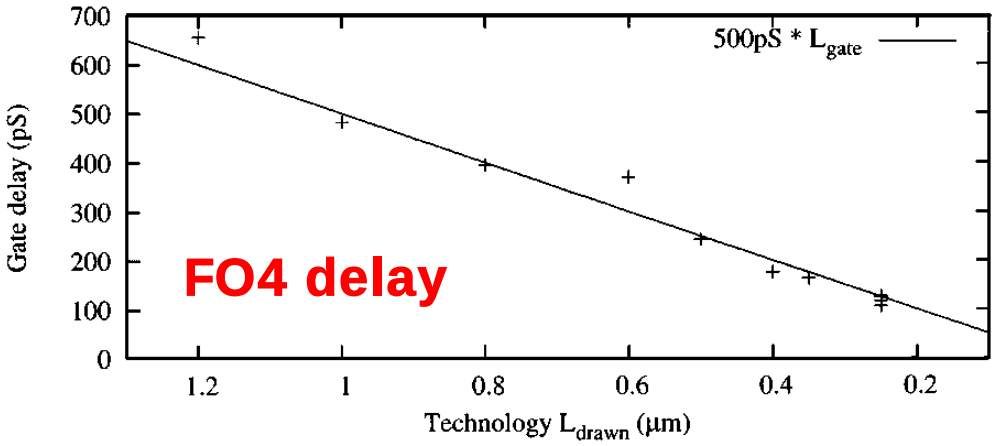


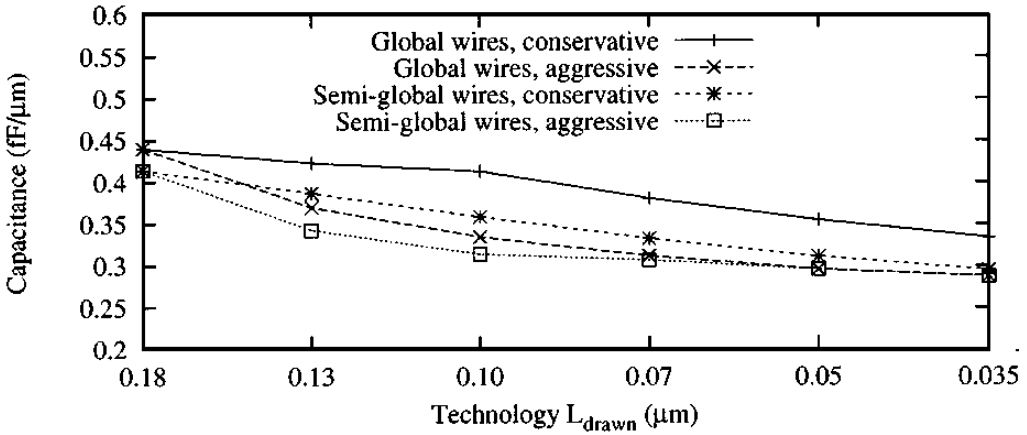
[Ho]

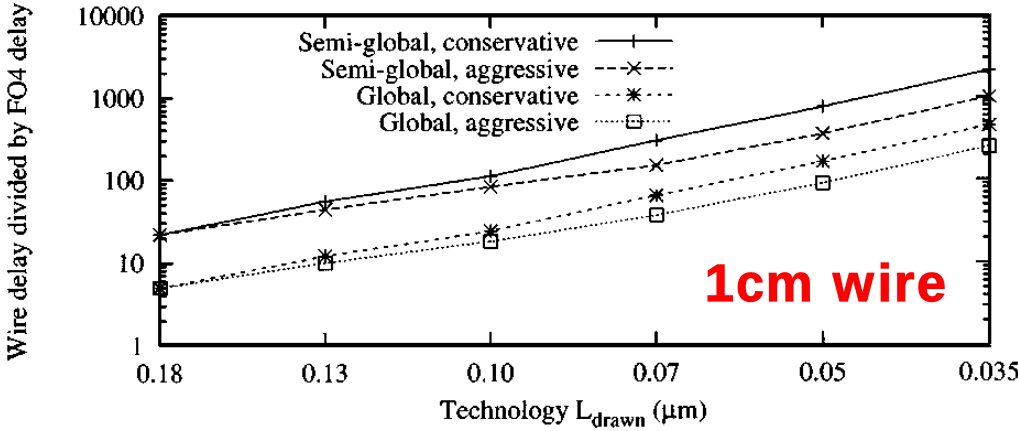
- Ideally, we scale everything by 0.7x when we move to a more advanced technology node for 2x density
- Results in 2x wire resistance, which dramatically increases wire RC delay
  - To compensate resistance wires get taller
- Cap grows at a smaller pace with scaling
  - Taller wires increase sidewall cap
  - Improved (low-k) dielectrics help reduce cap

Wire Scaling - Delay





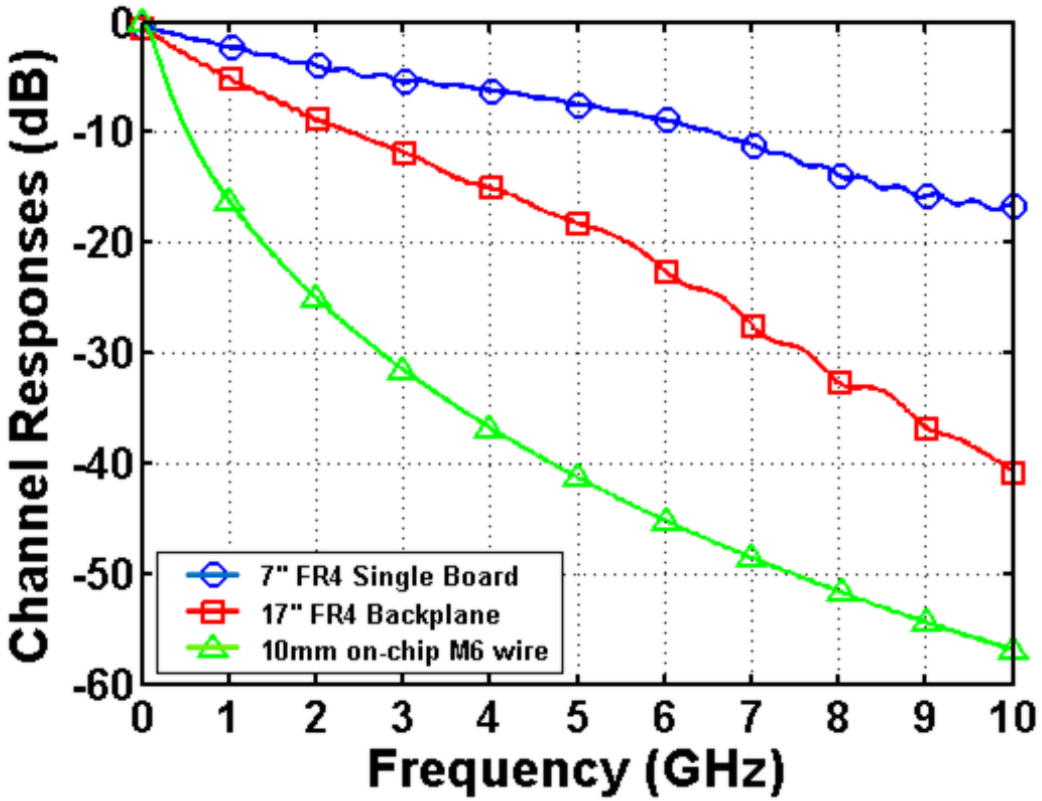




[Ho Proc. IEEE 2001]

- Global on-chip wire RC delay becomes many (100+) gate delays (if driven w/ one lumped driver)

Limited Wire Bandwidth



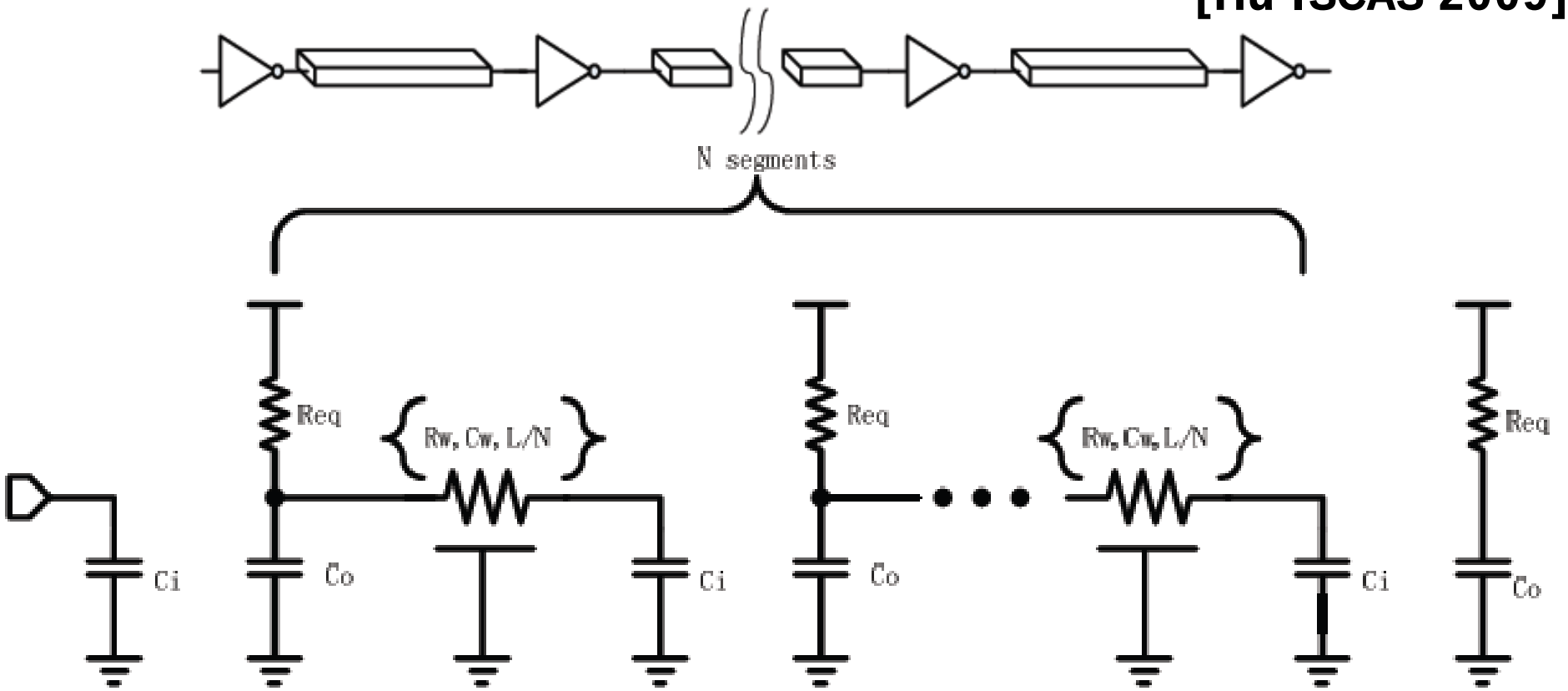
- Global on-chip wire bandwidth is much worse than chip-to-chip channels
- RC-dominated on-chip wires vs (R)LC-dominated off-chip wires

Clock Distribution Techniques

- Clock distribution techniques are typically compared in regards to jitter, delay, and power
- Techniques
  - Inverter Chain
  - CML Chain
  - Transmission Line
  - Inductive Load
  - Capacitively Driven Wires

Inverter Chain Distribution

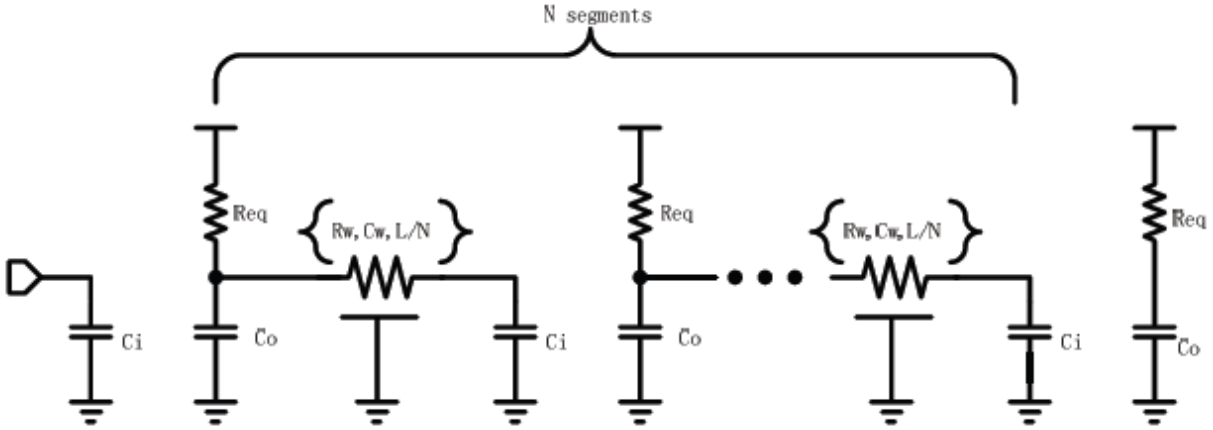
[Hu ISCAS 2009]



- Instead of driving the long low-bandwidth wire with one huge inverter, break wire up into N segments driven by N inverters

Elmore Delay of Inverter Chain Distribution

[Hu ISCAS 2009]



N = segment number

C_i, C_o, R_{eq} = inverter input cap, output cap, equivalent resistance

R_w, C_W = wire unit resistance and capacitance

L = wire length

C_{iu}, C_{ou}, R_{equ} = unit inverter input cap, output cap, equivalent resistance

m = multiple factor of unit inverter

$$t_P = N\left[0.69R_{eq}c_o + \left(0.69R_{eq} + 0.38\frac{R_wL}{N}\right)\frac{C_wL}{N} + 0.69\left(R_{eq} + \frac{R_wL}{N}\right)c_i\right]$$

$$= N\left[0.69\frac{R_{equ}}{m}mc_{ou} + \left(0.69\frac{R_{equ}}{m} + 0.38\frac{R_wL}{N}\right)\frac{C_wL}{N} + 0.69\left(\frac{R_{equ}}{m} + \frac{R_wL}{N}\right)mc_{iu}\right]$$

$$= 0.69NR_{equ}\left(c_{ou} + c_{iu}\right) + 0.38\frac{R_wC_wL^2}{N} + 0.69\frac{R_{equ}C_wL}{m} + 0.69mR_wLc_{iu}$$

N FO1 inverter τs

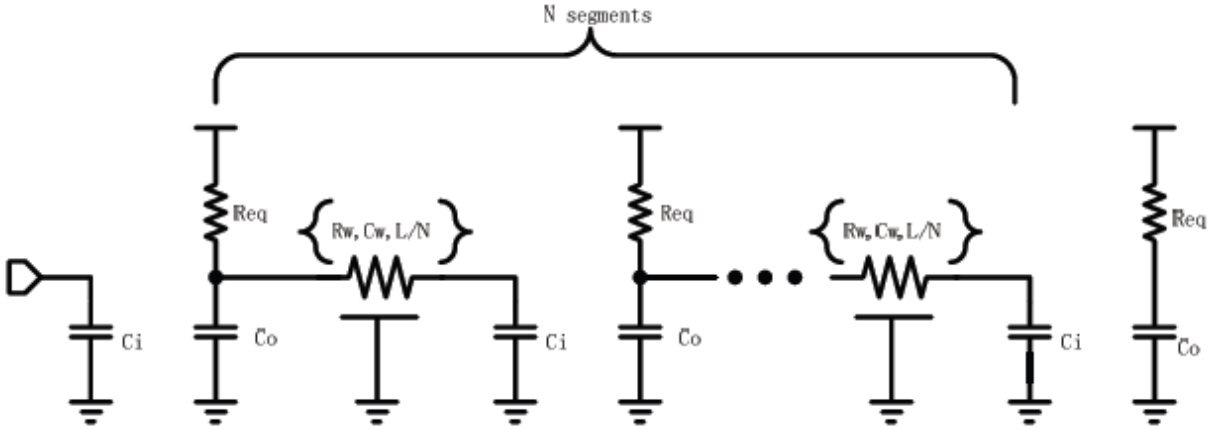
Inherent wire delay divided by N segments

RC of one inverter driving total wire cap

RC of wire driving one inverter

Elmore Delay of Inverter Chain Distribution

[Hu ISCAS 2009]



N = segment number

C_i, C_o, R_{eq} = inverter input cap, output cap, equivalent resistance

R_w, C_W = wire unit resistance and capacitance

L = wire length

C_{iu}, C_{ou}, R_{equ} = unit inverter input cap, output cap, equivalent resistance

m = multiple factor of unit inverter

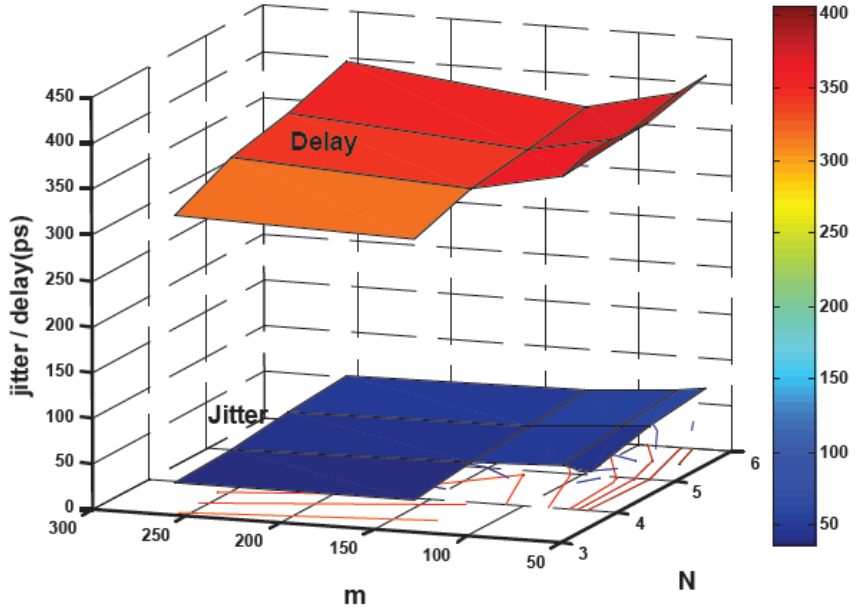
$$t_P = 0.69NR_{equ}\left(c_{ou} + c_{iu}\right) + 0.38\frac{R_w C_w L^2}{N} + 0.69\frac{R_{equ} C_w L}{m} + 0.69mR_w L c_{iu}$$

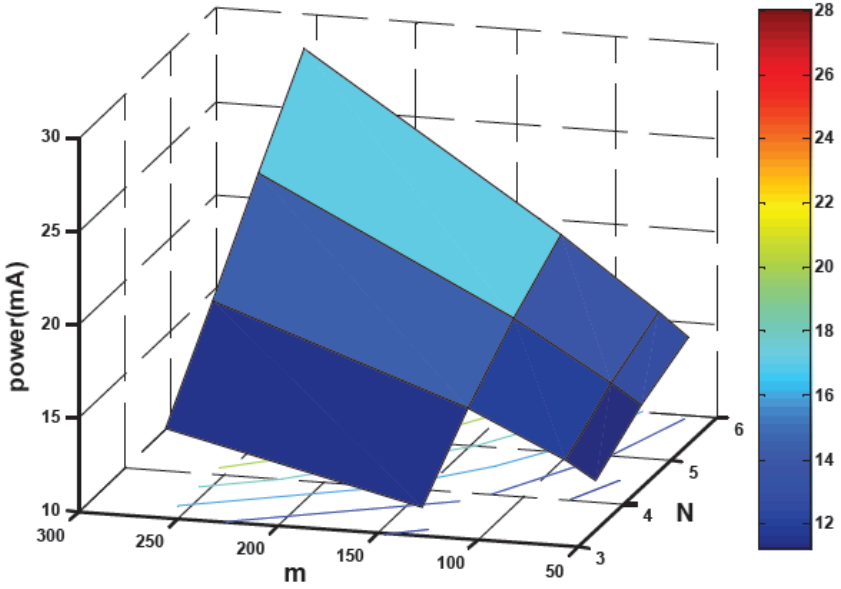
For Minimum Propagation Delay

$$N = 0.742L\sqrt{\frac{R_W C_w}{R_{equ}\left(c_{ou} + c_{iu}\right)}} \quad \text{and} \quad m = \sqrt{\frac{R_{equ} C_w}{R_W c_{iu}}}$$

Inverter Chain Distribution
Delay, Jitter, and Power Trade-offs

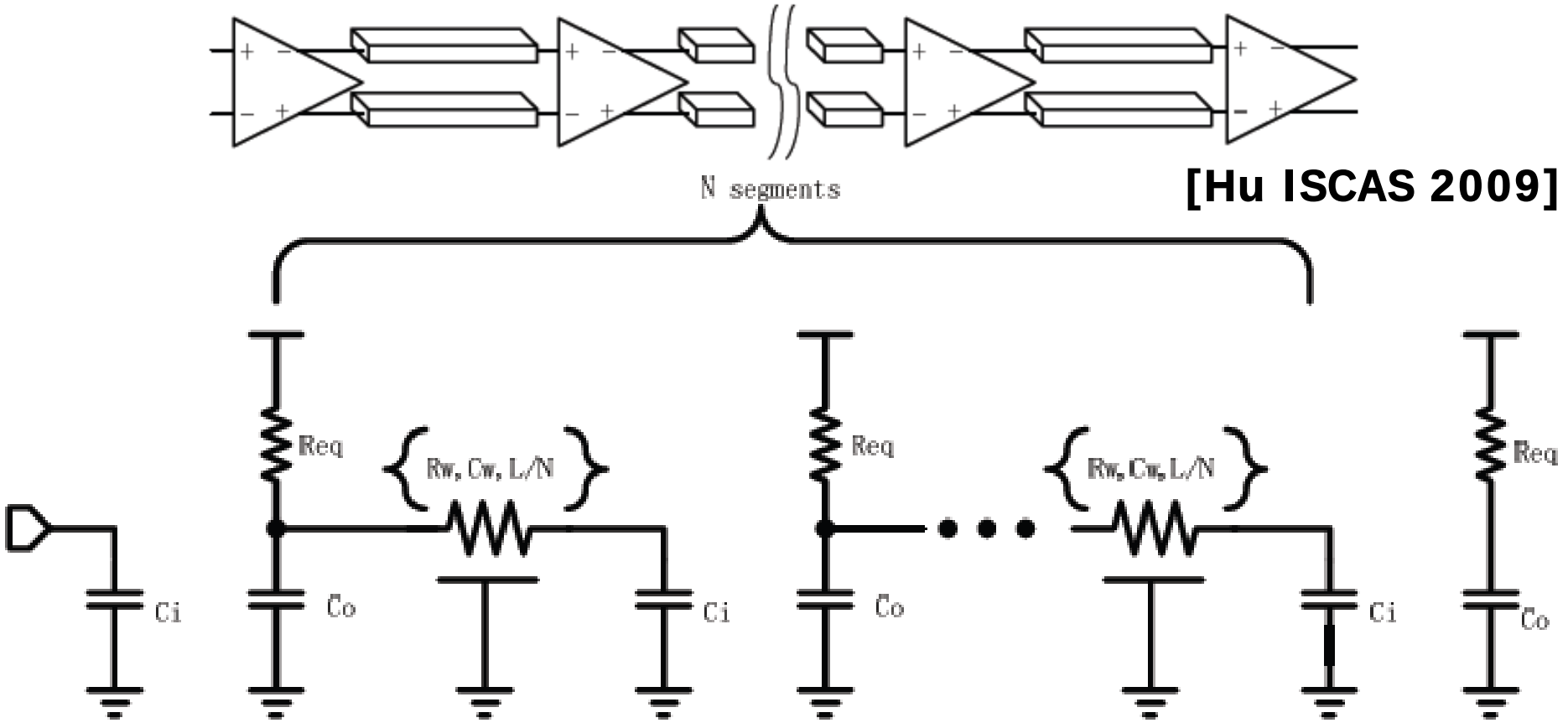
[Hu ISCAS 2009]





- Delay and jitter are correlated, but don't necessarily share same minimum
- For 5mm wire in 90nm CMOS
  - Minimum jitter (36ps): N=3 and m=256
  - Minimum delay (321ps): N=3 and m=128
  - Minimum power: N=4 and m=64

CML Chain Distribution

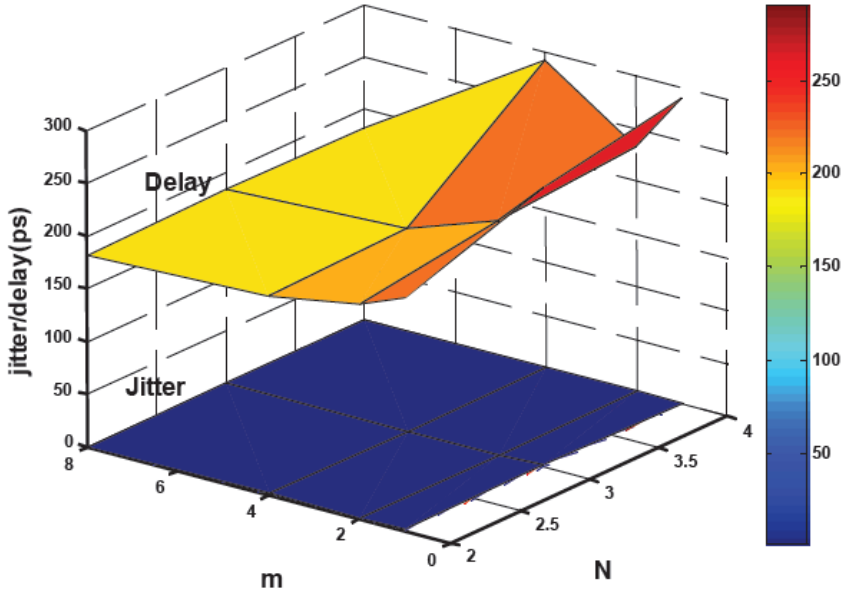


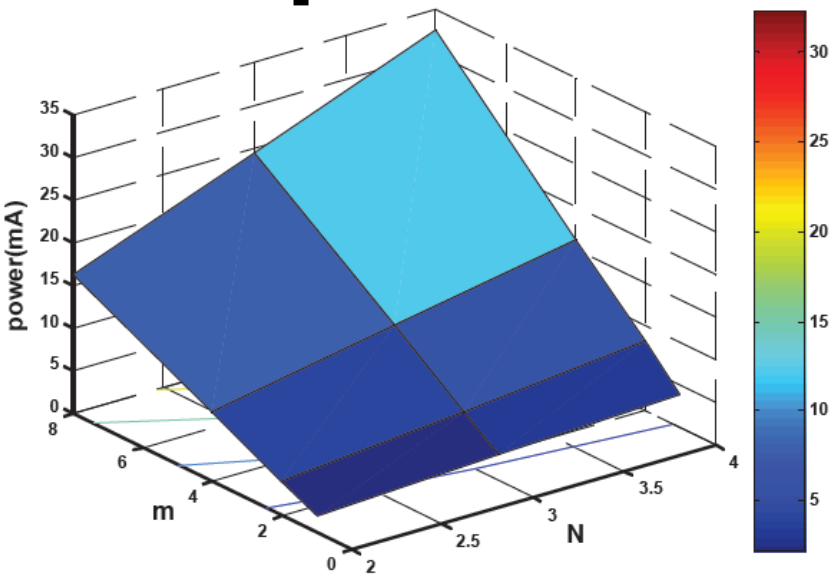
[Hu ISCAS 2009]

- Relative to inverter-based buffers, low-swing CML buffers offer increased bandwidth and PSRR
- Same model used to analyze CML distribution

CML Chain Distribution
Delay, Jitter, and Power Trade-offs

[Hu ISCAS 2009]

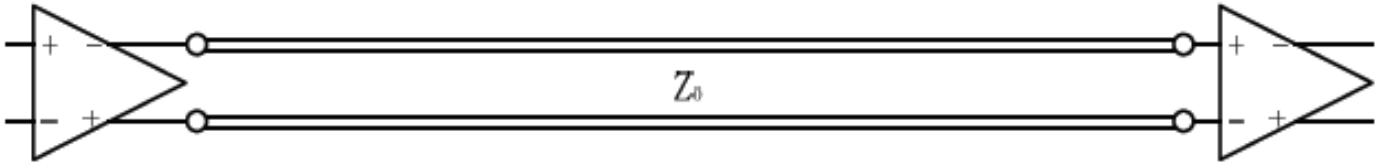




- Analysis with 400mV$_{ppd}$ swing (R=200Ω, I$_{tail}$=1mA)
- For 5mm wire in 90nm CMOS
  - Minimum jitter (0.5ps): N=2 and m=8
  - Minimum delay (182ps): N=4 and m=8
  - Minimum power: N=2 and m=1
- Much better jitter performance than inverter-based distribution
  - However, jitter amplification is not considered in this work
  - CML buffers may be more sensitive to input jitter than inverter-based

Transmission Line Distribution

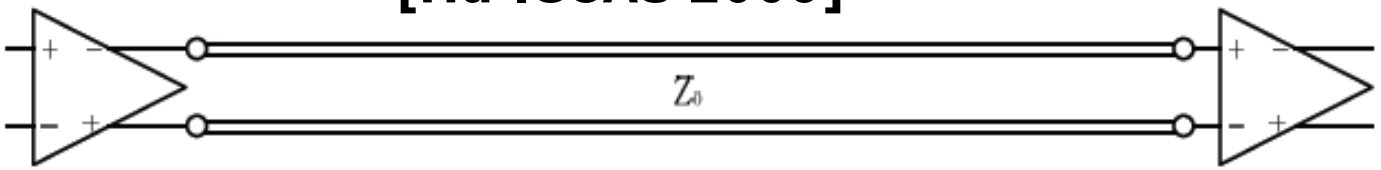
[Hu ISCAS 2009]

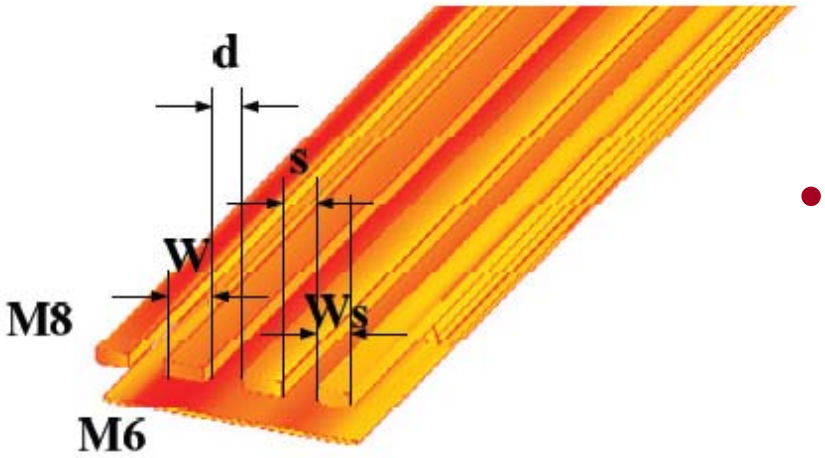


- On-die transmission lines can be realized with wider than minimum-width wires
- DC resistance is small relative to characteristic impedance, i.e. distributed wire inductance has strong impact on wire delay
- Allows for “speed-of-light” propagation velocity
- Passive transmission line doesn’t introduce any jitter

On-Die Transmission Lines

[Hu ISCAS 2009]





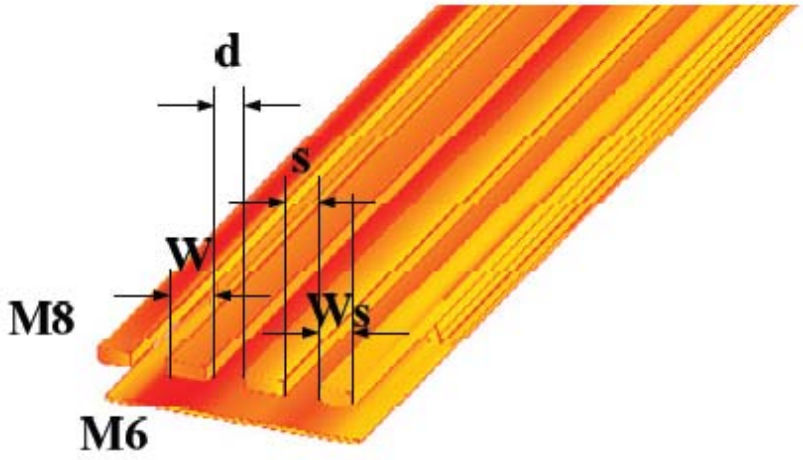
- If signaling is strictly on-chip, have more freedom to choose differential impedance
- Larger impedance will allow for lower power, but there are limitations
  - Parasitic capacitance
  - DC resistance

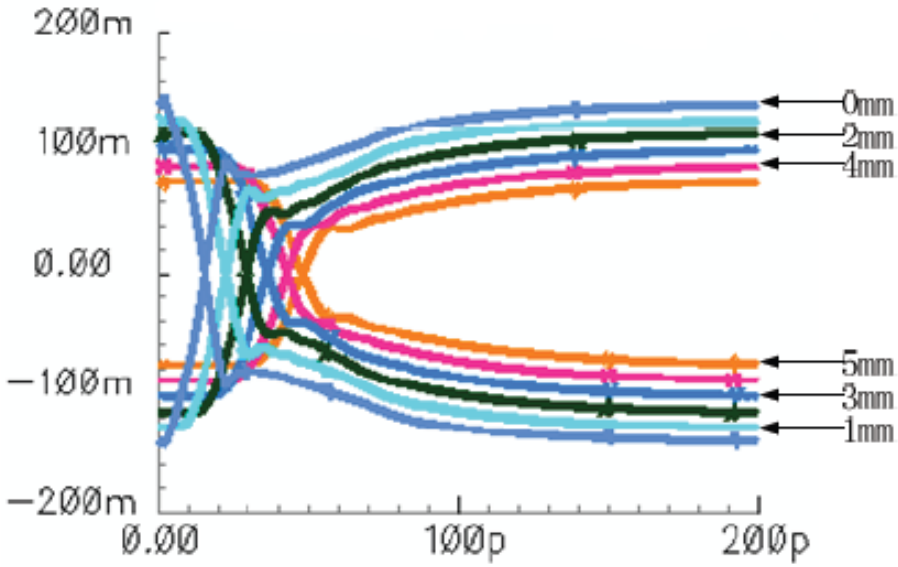
- Because of this, many times the on-die transmission lines will display differential impedance close to the typical off-chip 100Ω value

Clock Swing Along Transmission Line

5mm Transmission Line
W=6μm, d=2.5μm, Wgnd=4μm, s=4μm
Zo=120Ω and RDC = 42Ω

[Hu ISCAS 2009]





- DC-loss of transmission lines causes reduction in the clock swing as it travels down the line
- For 5mm line, delay=43ps and jitter=0.18ps

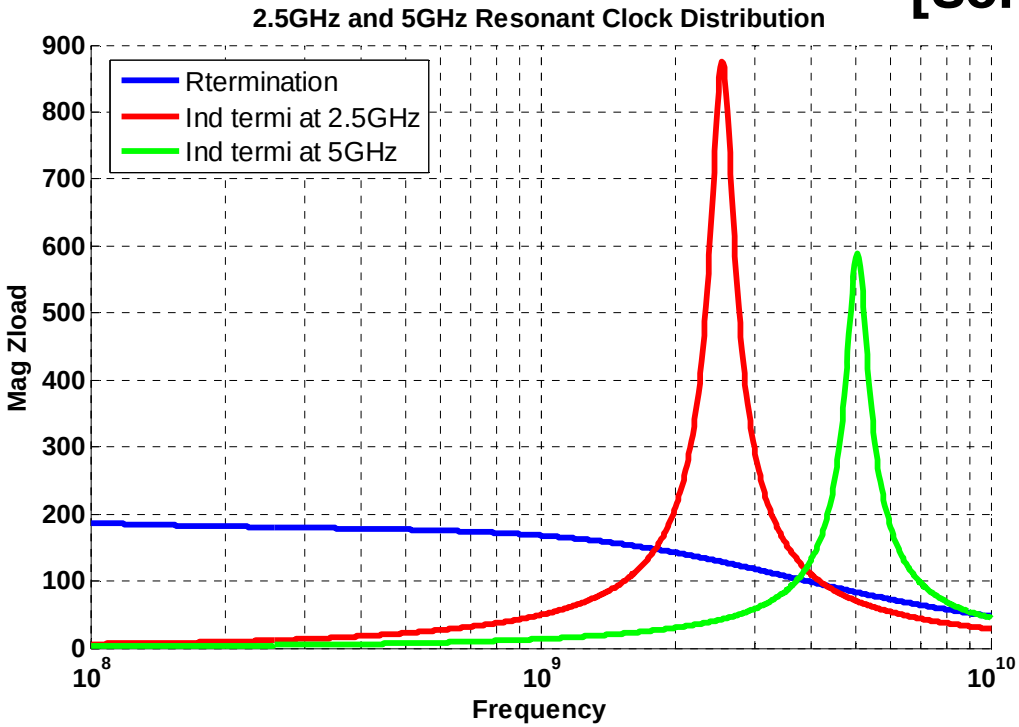
Inductive Load Distribution

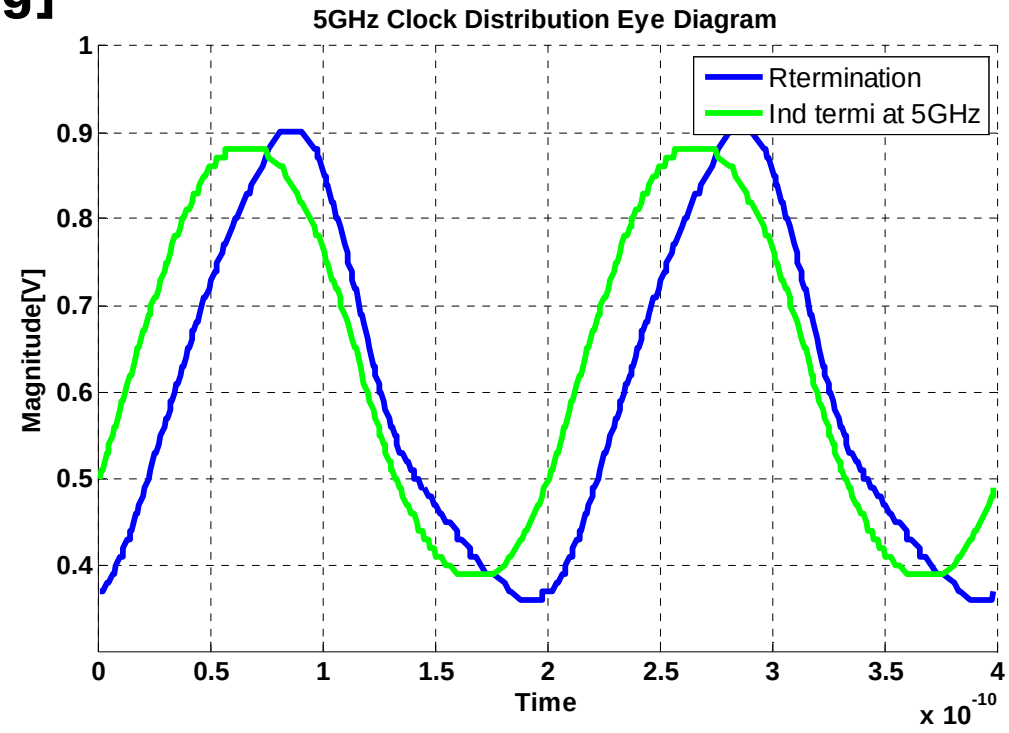
[Hu ISCAS 2009]

- Inductively-loaded wire can boost wire impedance by resonating with the wire capacitance at the clock frequency
  - Reduces power
  - Provides jitter filtering
- Cost is high inductor area, particularly at lower clock frequencies

Inductive Load Distribution

[Song]



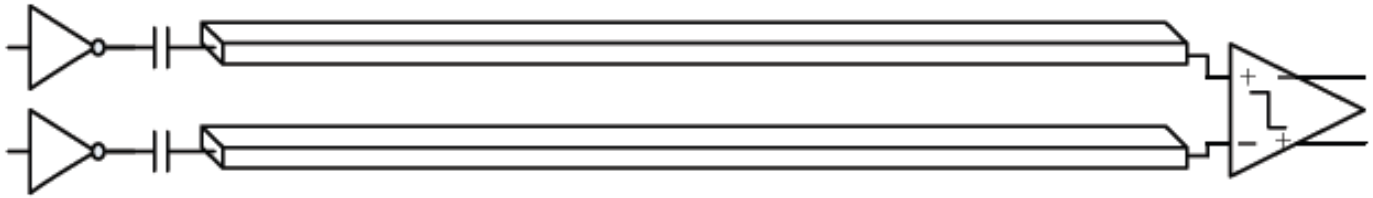


5GHz	Inductor Load	R Load
Vswing	500mV	538mV
Power	1.2mW	7.2mW

- For similar clock swing, inductive termination can offer significant power savings

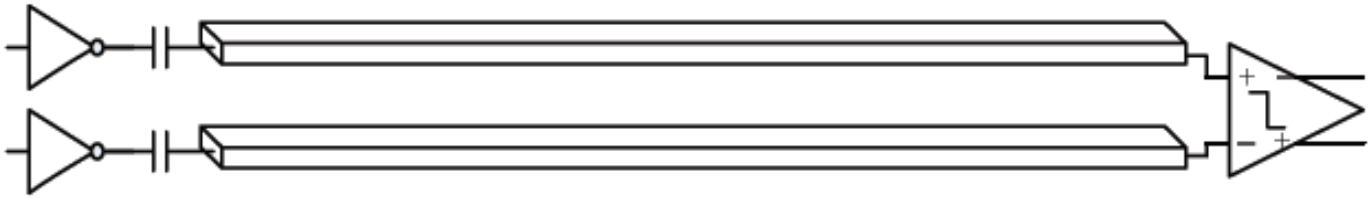
Capacitively Driven Wires Distribution

[Hu ISCAS 2009]



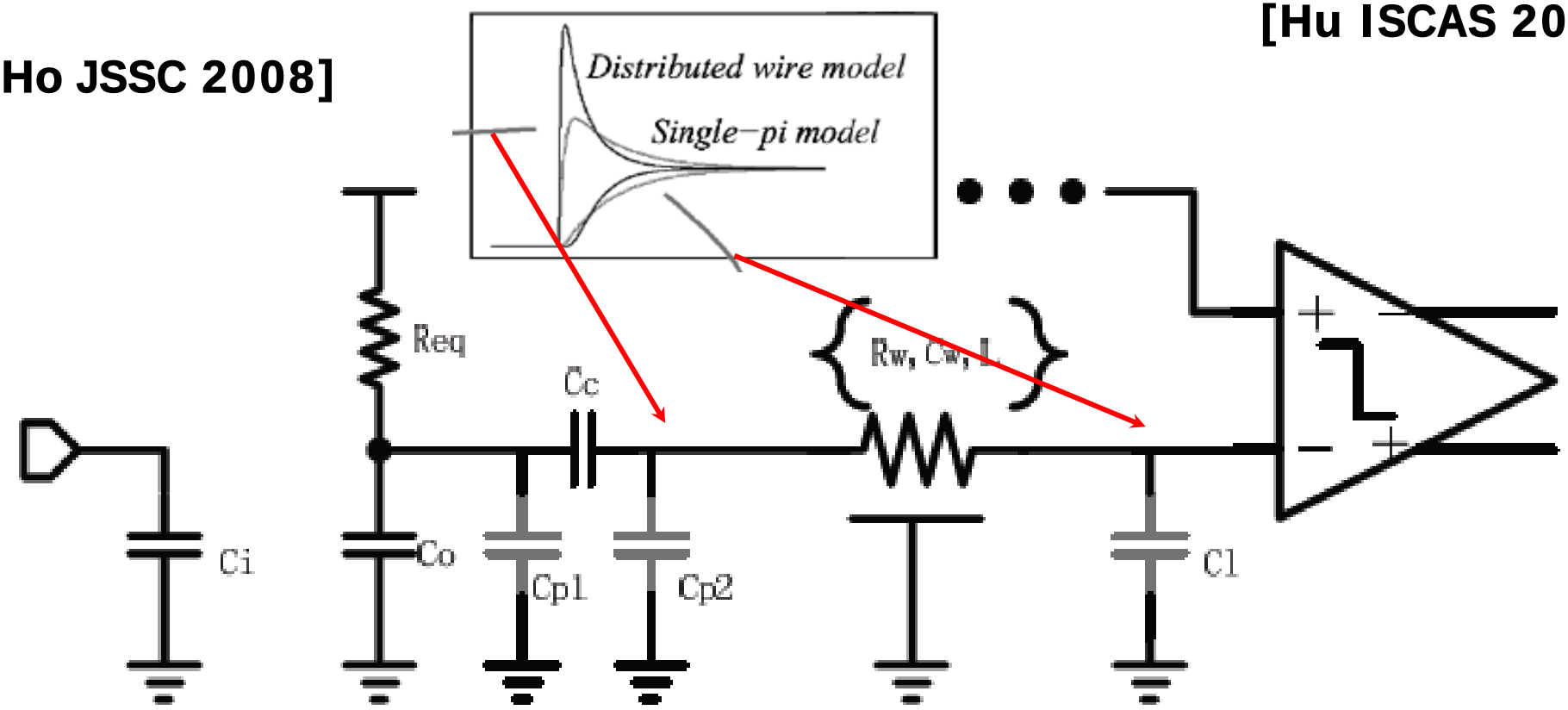
- Adding a capacitor in series to the psuedo-differential inverter-based drivers significantly reduces driver loading

Capacitively Driven Wires Model



[Hu ISCAS 2009]

[Ho JSSC 2008]

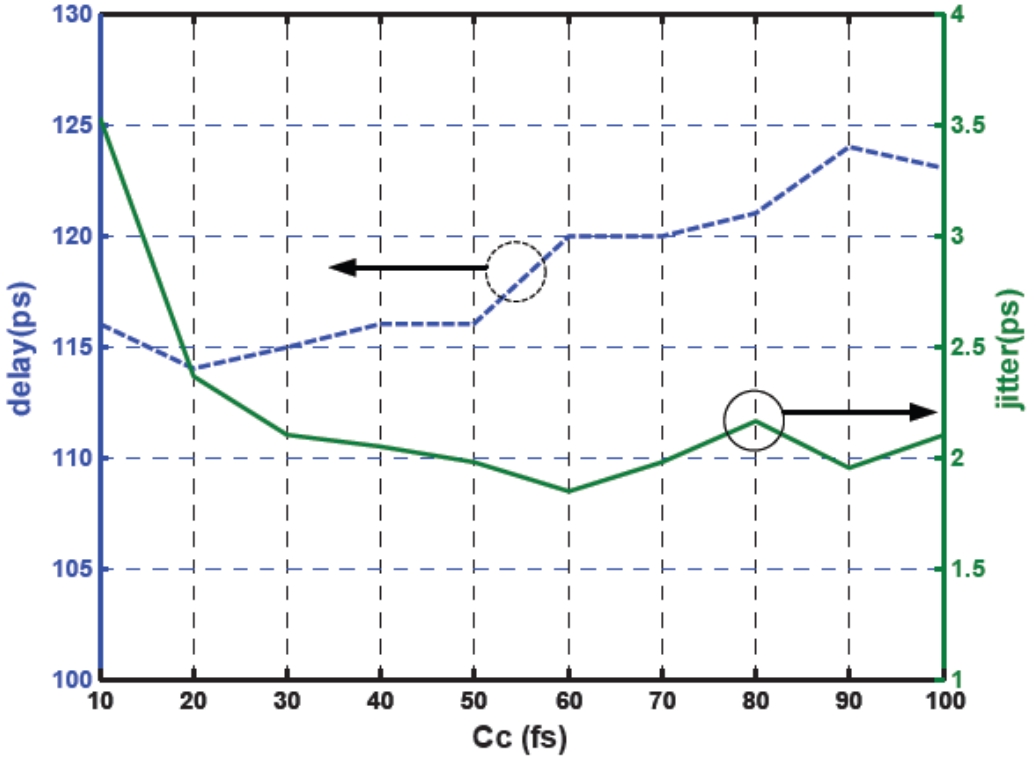


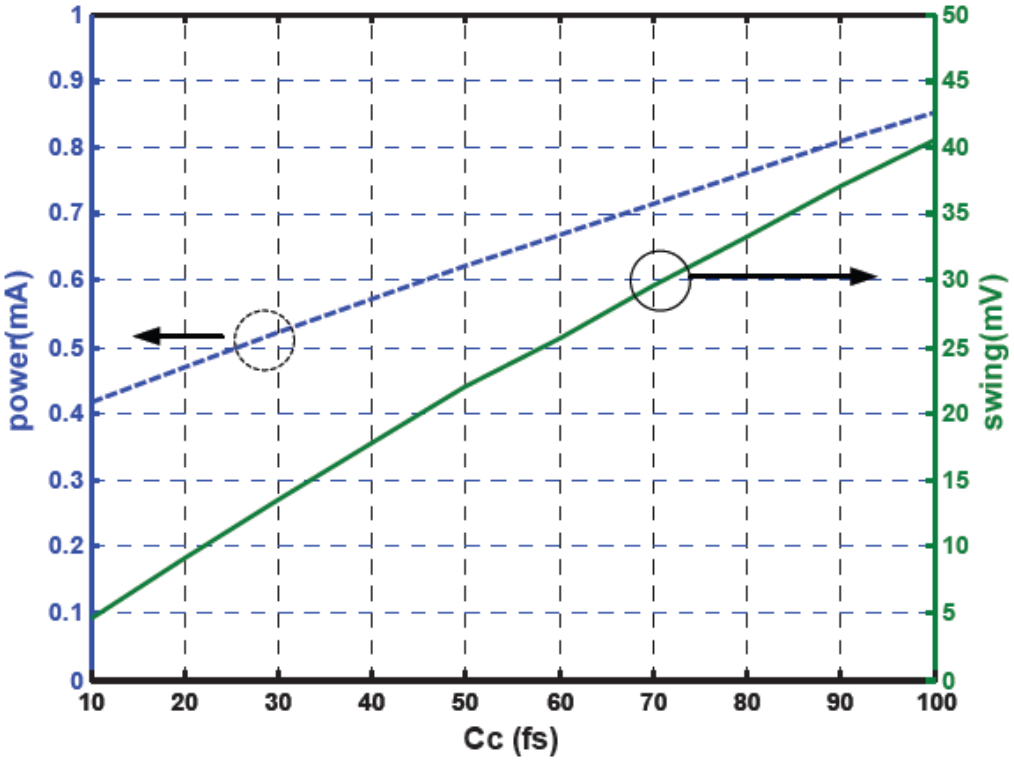
$$t_P = 0.69R_{eq}\left(c_o + c_{p1} + c_c\right) + 0.19R_wC_wL^2$$

Capacitively Driven Wires Distribution

$$t_P = 0.69R_{eq}\left(c_o + c_{p1} + c_c\right) + 0.19R_wC_wL^2$$

[Hu ISCAS 2009]





- Minimum series cap reduces delay and power, but swing also
- If cap is too small, increased jitter is observed

Clock Distribution Performance Comparison

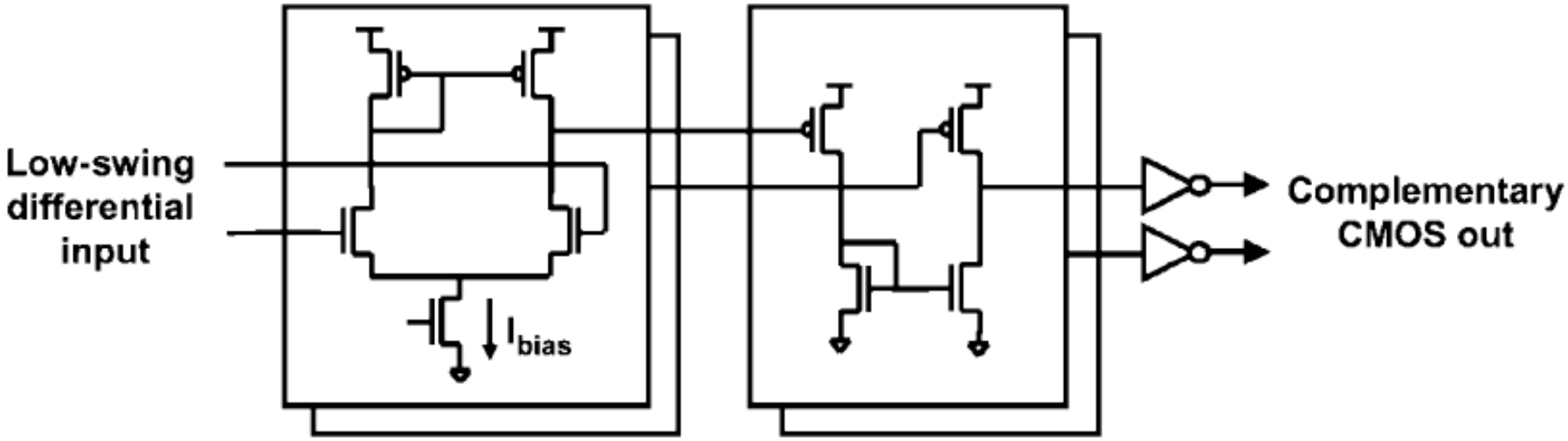
Technology	1.2V 90nm CMOS		
Methods (with optimal tradeoff)	**Performance**		
	jitter(ps)	***delay(ps)***	***power(mW)***
Inverter chain (N=3, m=128)	36	321	11.5
CML chain (N=2, m=1)	1	221	2
Transmission line	0.18	43	4
Inductive load (L=6nH, Q=2)	0.42	55	4
CDW (Cc=50f)	1.98	116	0.62

[Hu ISCAS 2009]

- Transmission-line distribution offers best jitter and delay performance
- CDW offers minimum jitter-power and delay-power product
- Note, everything but inverter-chain distribution is low-swing
- If CML2CMOS converter is not designed well, that can kill your nice distribution network performance

CML2CMOS Converter (1)

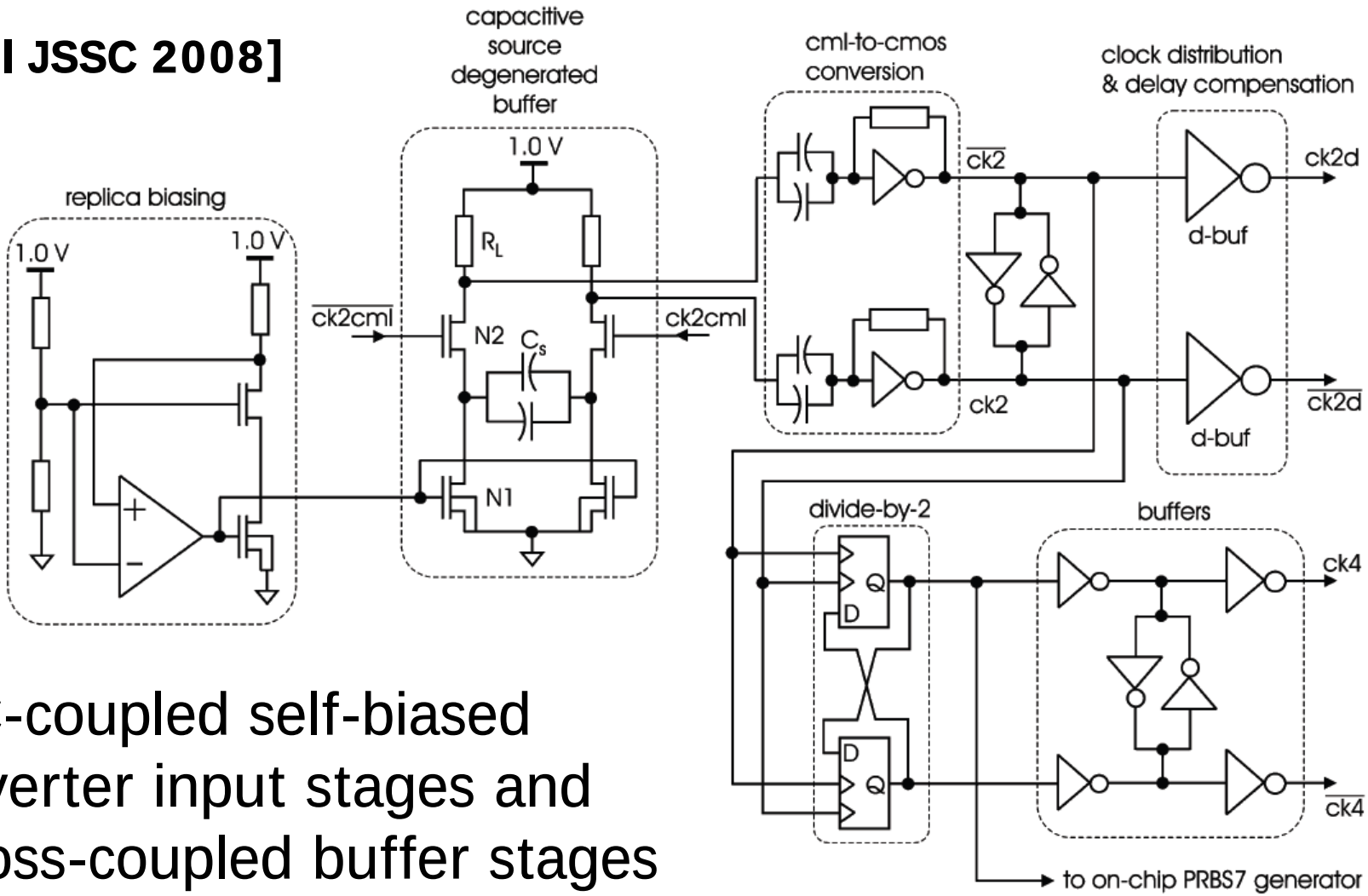
[Balamurugan JSSC 2008]



- Differential input stage followed by high-swing output stage
- Can be sensitive to power-supply noise and reduce jitter benefits of low-swing distribution techniques
- Often require some type of duty-cycle control

CML2CMOS Converter (2)

[Kossel JSSC 2008]



- AC-coupled self-biased inverter input stages and cross-coupled buffer stages can help improve duty cycle performance