ECEN689: Special Topics in High-Speed Links Circuits and Systems Spring 2010

Lecture 10: Termination & Transmitter Circuits

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Announcements

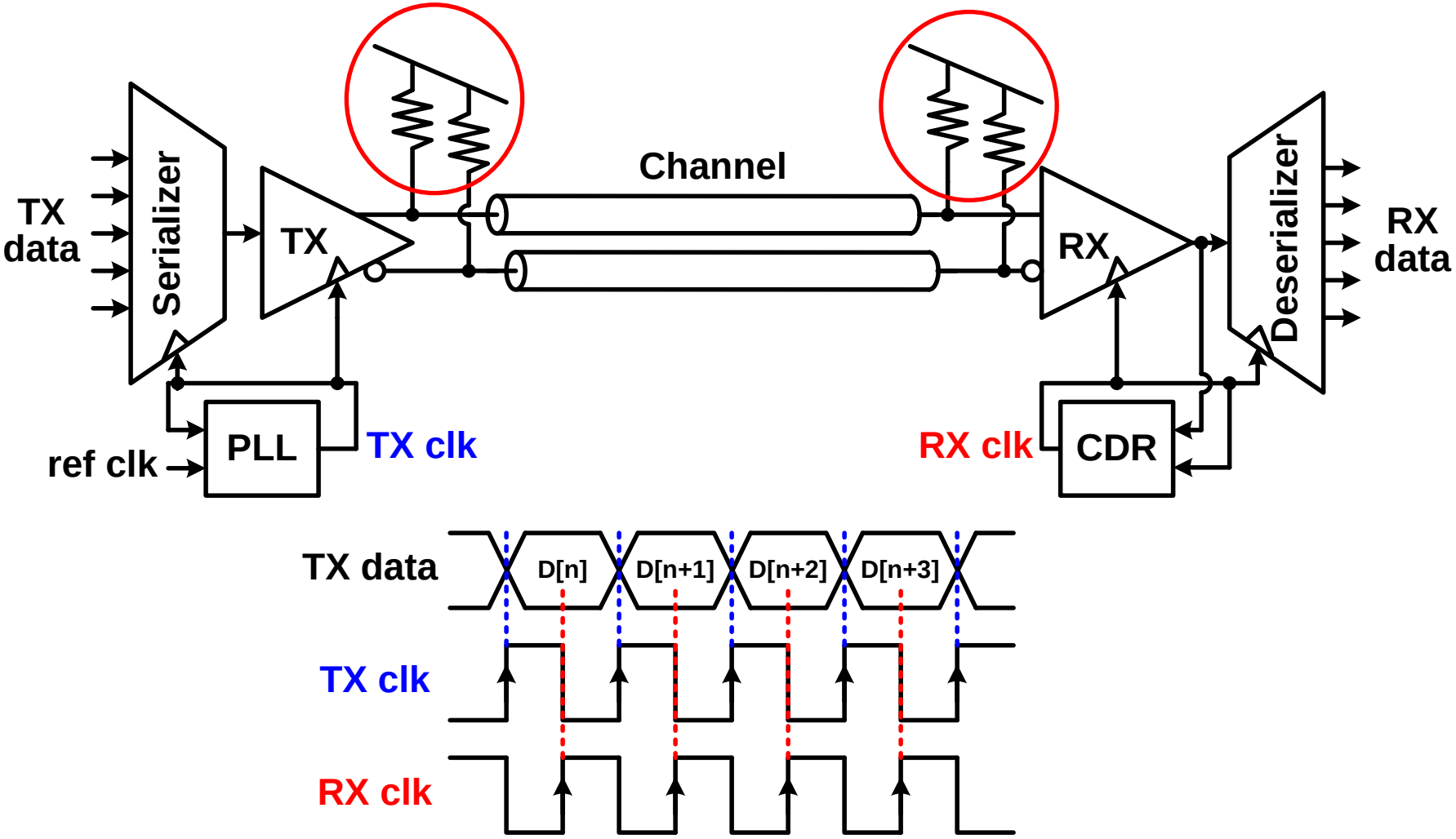
- Exam 1 will be second week of March (3/8-12)

- Reading
  - Dally 11.1-11.3

Agenda

- Termination Circuits
- Transmitter Circuits

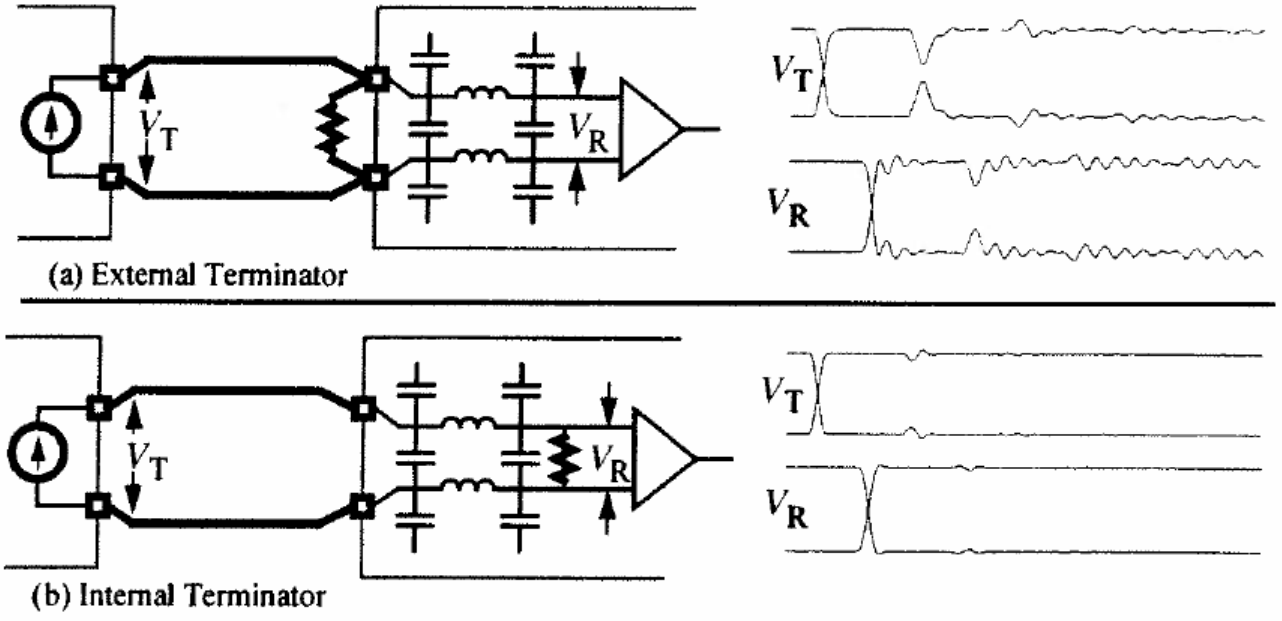
High-Speed Electrical Link System



Termination

- Off-chip vs on-chip
- Series vs parallel
- DC vs AC Coupling
- Termination circuits

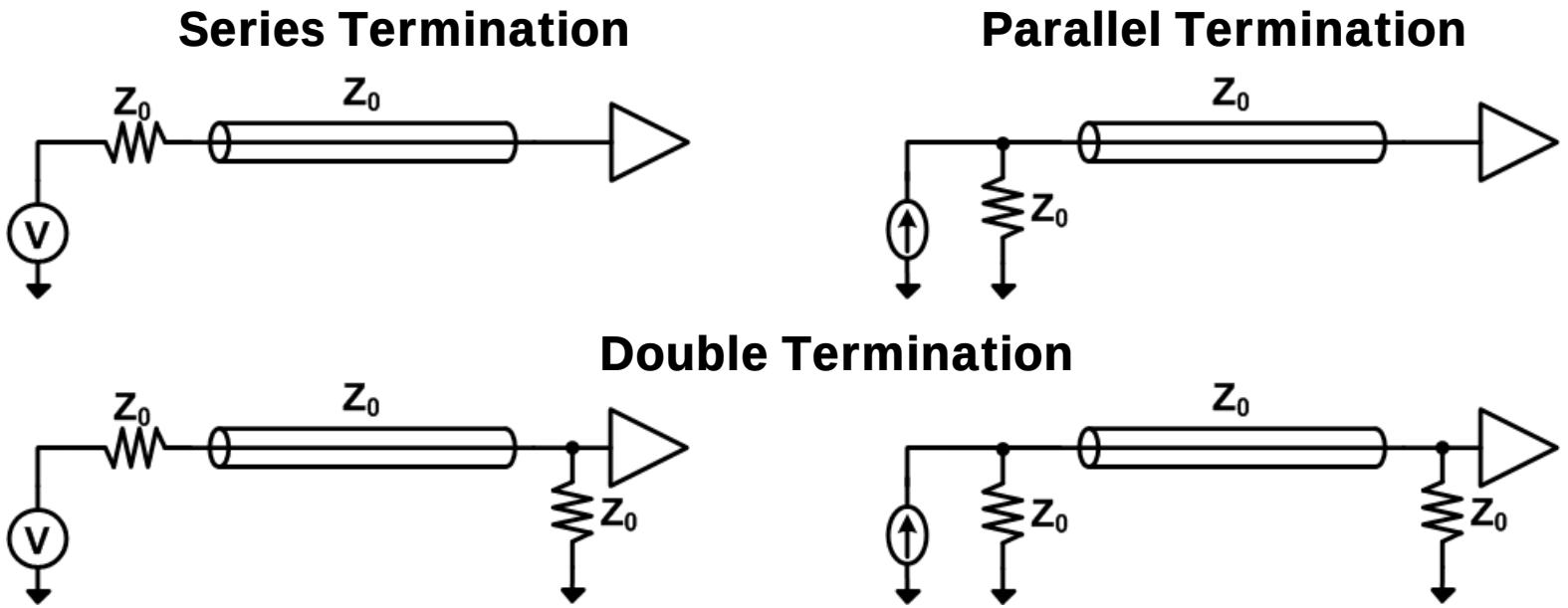
Off-Chip vs On-Chip Termination



[**Dally**]

- Package parasitics act as an unterminated stub which sends reflections back onto the line
- On-chip termination makes package inductance part of transmission line

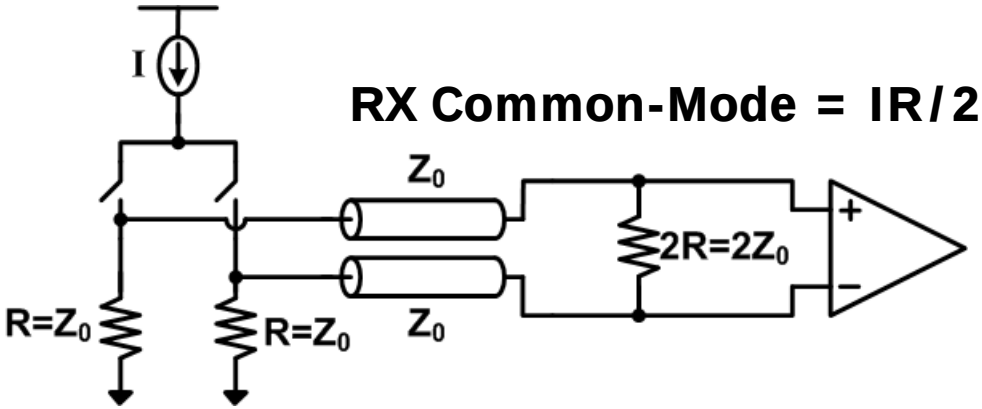
Series vs Parallel Termination



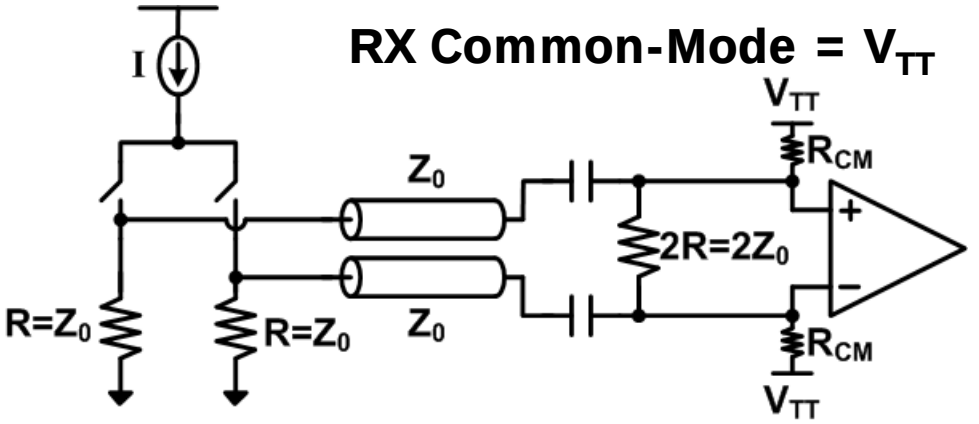
- Low impedance voltage-mode driver typically employs series termination
- High impedance current-mode driver typically employs parallel termination
- Double termination yields best signal quality
  - Done in majority of high performance serial links

AC vs DC Coupled Termination

- DC coupling allows for uncoded data
- RX common-mode set by transmitter signal level



- AC coupling allows for independent RX common-mode level
- Now channel has low frequency cut-off
  - Data must be coded



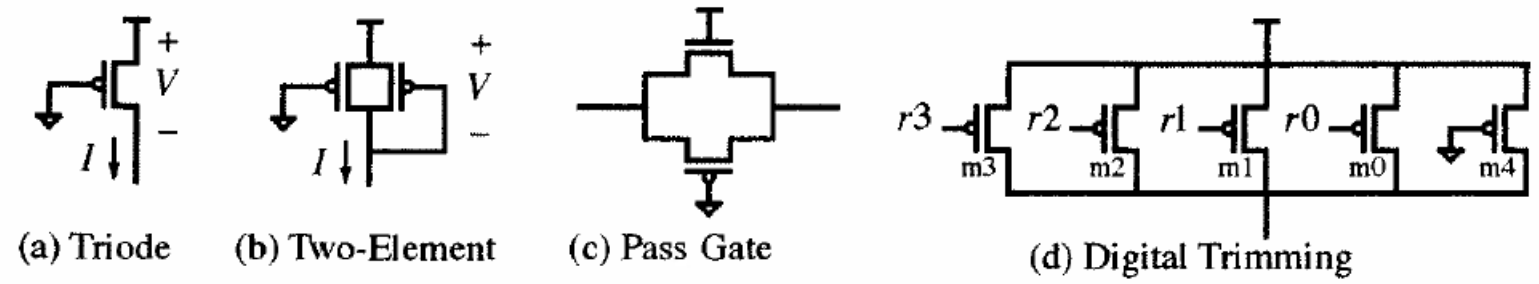
Passive Termination

- Choice of integrated resistors involves trade-offs in manufacturing steps, sheet resistance, parasitic capacitance, linearity, and ESD tolerance
- Integrated passive termination resistors are typically realized with unsalicided poly, diffusion, or n-well resistors
- Poly resistors are typically used due to linearity and tighter tolerances, but they typically vary +/-30% over process and temperature

Resistor Options (90nm CMOS)

Resistor	Poly	N-diffusion	N-well
Sheet R (Ω/sq)	90±10	300±50	450±200
VC1(V^{-1})	0	10^{-3}	$8x10^{-3}$
Parasitic Cap	2-3fF/um^2 (min L poly)	0.9fF/um^2 (area), 0.04fF/um (perimeter)	0.2fF/um^2 (area), 0.7fF/um (perimeter)

Active Termination



- Transistors must be used for termination in CMOS processes which don't provide resistors
- Triode-biased FET works well for low-swing (<500mV)
  - Adding a diode connected FET increases linear range
- Pass-gate structure allows for differential termination

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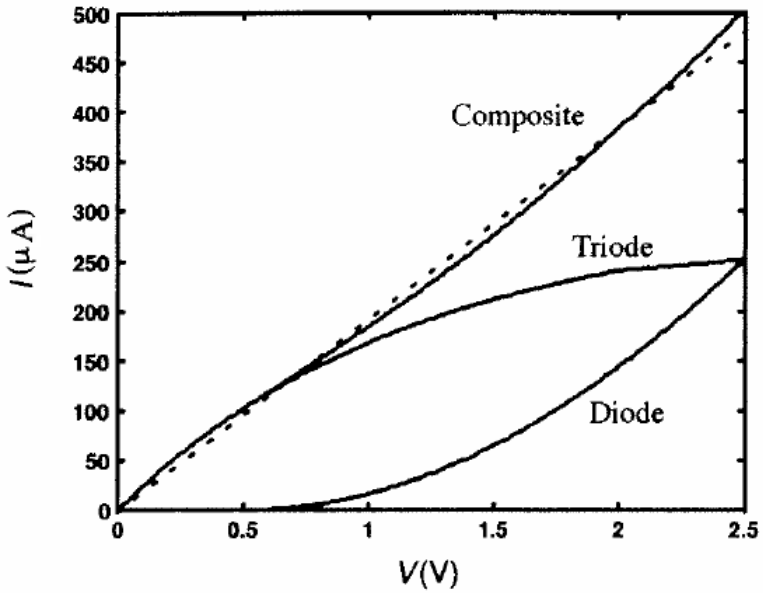
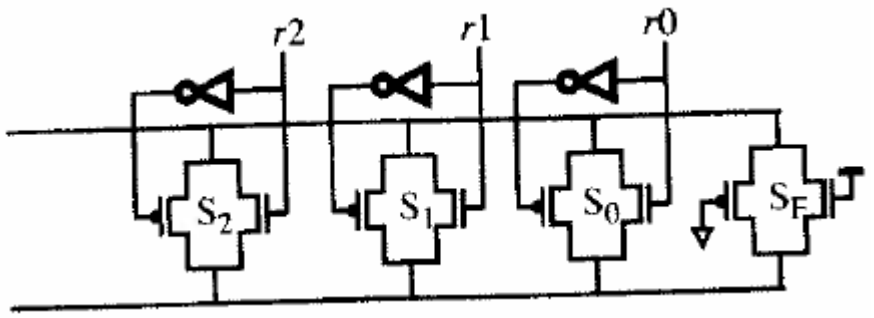


Adjustable Termination

- FET resistance is a function of gate overdrive

$$R_{FET} = \frac{1}{\mu C_{ox}(W/L)(V_{GS} - V_t)}$$



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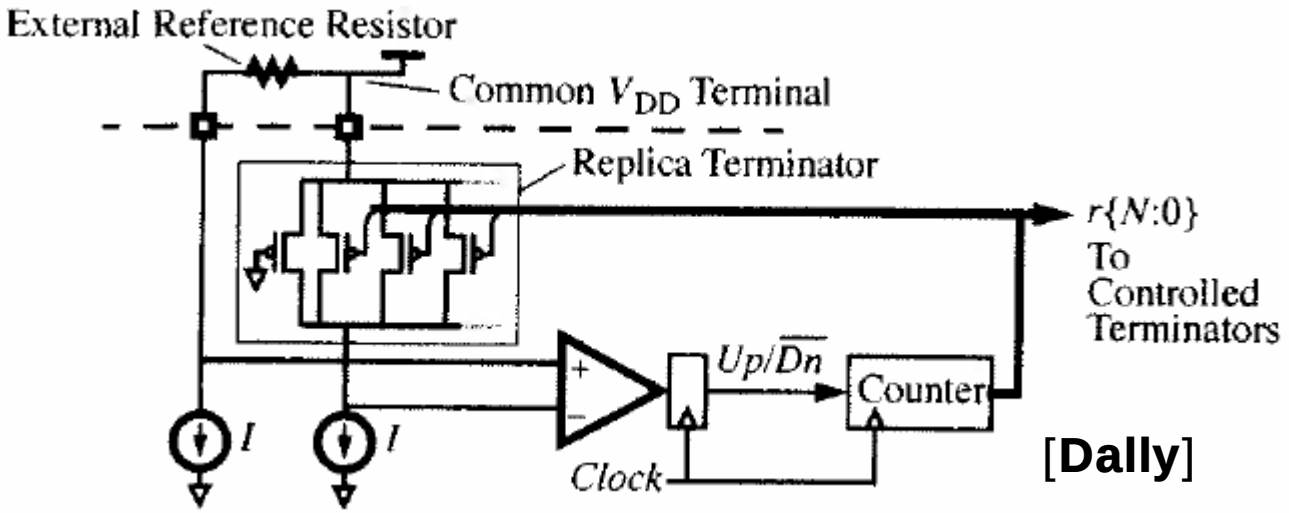
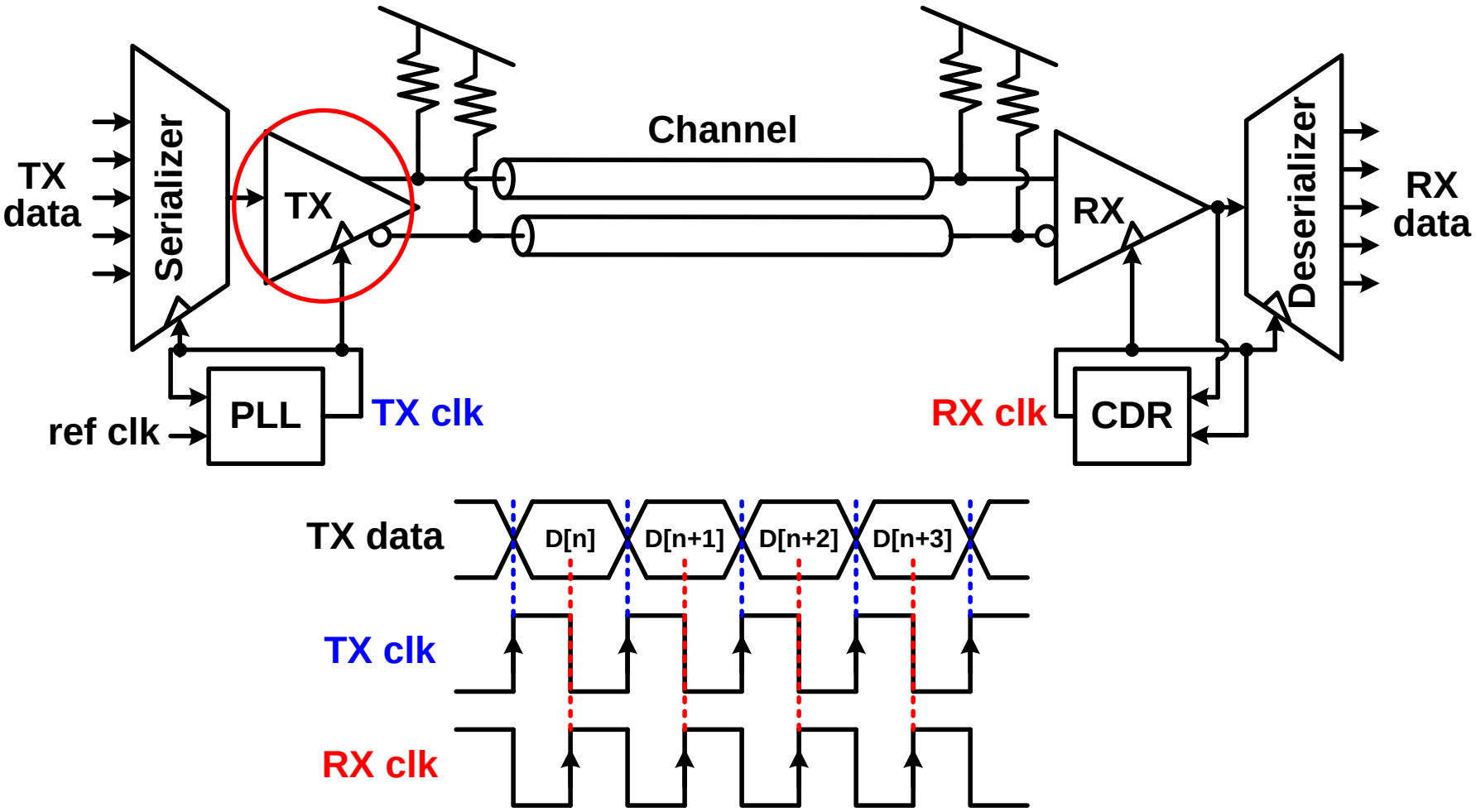
- Large variance in FET threshold voltage requires adjustable termination structures
- Calibration can be done with an analog control voltage or through digital "trimming"
  - Analog control reduces V_{GS} and linear range
  - Digital control is generally preferred

Termination Digital Control Loop



- Off-chip precision resistor is used as reference
- On-chip termination is varied until voltages are within an LSB
  - Dither filter typically used to avoid voltage noise
- Control loop may be shared among several links, but with increased nanometer CMOS variation per-channel calibration may be necessary

High-Speed Electrical Link System

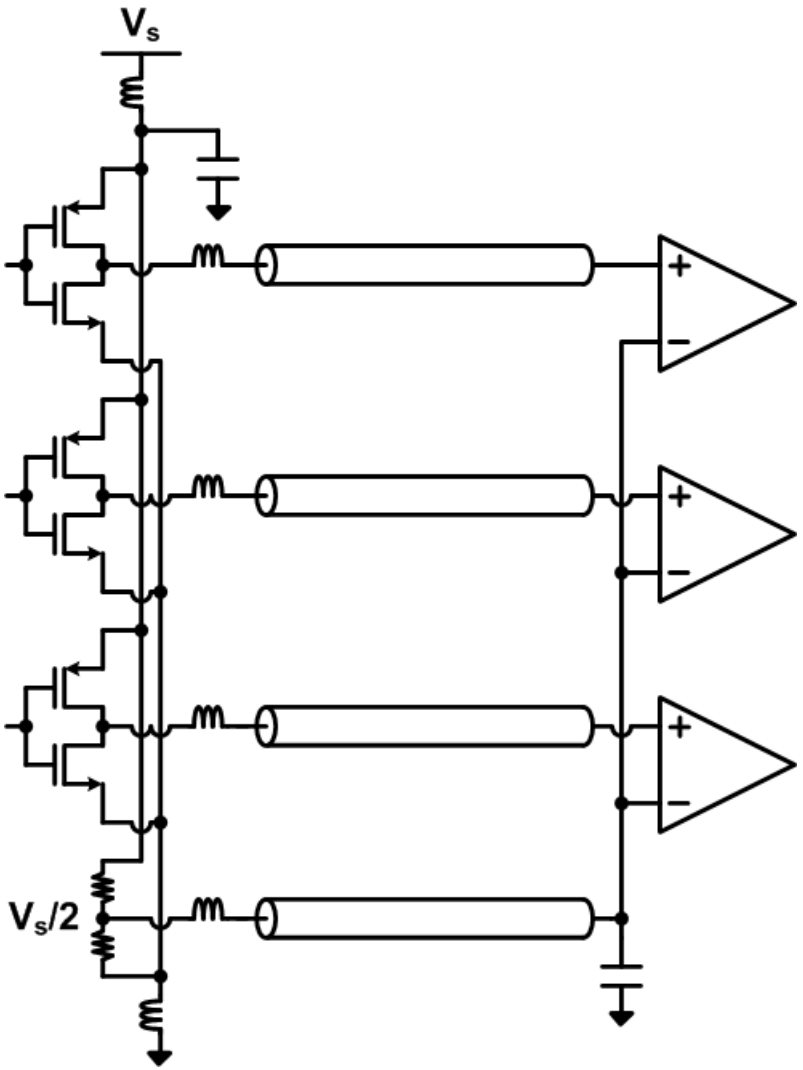


Transmitter Circuits

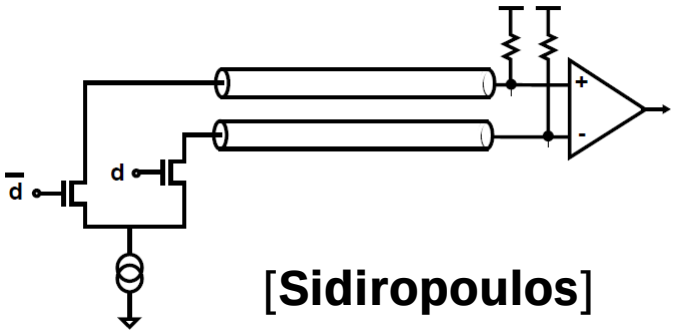
- Single-ended vs differential signaling
- Current-mode drivers
- Voltage-mode drivers
- Slew-rate control

Single-Ended Signaling

- Finite supply impedance causes significant Simultaneous Switching Output (SSO) noise (xtalk)
- Necessitates large amounts of decoupling capacitance for supplies and reference voltage
  - Decap limits I/O area more that circuitry



Differential Signaling



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- A difference between voltage or current is sent between two lines
- Requires 2x signal lines relative to single-ended signaling, but less return pins
- Advantages
  - Signal is self-referenced
  - Can achieve twice the signal swing
  - Rejects common-mode noise
  - Return current is ideally only DC

Next Time

- Transmitter Circuits
  - Current-mode drivers
  - Voltage-mode drivers
  - Slew-rate control
- Multiplexing Circuits
- Receiver Circuits