1. **High-Speed Comparator Design.** This problem involves the design of 4 different high-speed comparators to meet the following specifications:
   a. clk → D_{out} delay ≤ 200ps with a 10mV static differential input voltage (D_{in}^+-D_{in}^-) at a common mode voltage of 80%*VDD. Measure delay from when the clock is at 50% VDD to D_{out}^+ is at 50% VDD for an output rising transition.
   b. Clock frequency = 2.5GHz. Use at least one inverter-based buffer to clock your circuit for realistic clock waveforms.
   c. Load cap on D_{out}^+ and D_{out}^- is 10fF.
   d. Input referred offset σ ≤ 10mV. Here you can optimistically assume that the input referred offset is just due to the input differential pair Vt mismatch and use the mismatch equation given in the notes (check your tox in your model), i.e. no need to run Monte Carlo simulations.
   e. Optimize the design for power consumption, i.e. don’t overdesign for a supper small delay. Try to minimize total capacitance while still meeting the 200ps delay and offset specifications.

Design the comparators based on the following 4 architectures:
   1. **Conventional Strong-Arm Latch.** For an example schematic, refer to Figure 4 in J. Kim *et al*., “Simulation and Analysis of Random Decision Errors in Clocked Comparators,” IEEE Transactions on Circuits and Systems - I, vol. 56, no. 8, Aug. 2009, pp. 1844-1857. Feel free to change the pre-charge transistors configuration if you desire.
   2. **CML Latch.** For an example schematic, refer to Figure 11a in T. Toifl *et al*., “A 22-Gb/s PAM-4 Receiver in 90-nm CMOS SOI Technology,” IEEE Journal of Solid-State Circuits, vol. 41, no. 4, Apr. 2006, pp. 954-965.
   3. **Schinkel Low-Voltage Latch.** For an example schematic, refer to Figure 2 in D. Schinkel *et al*., “A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time,” IEEE International Solid-State Circuits Conference, Feb. 2007.
   4. **Goll Low-Voltage Latch.** For an example schematic, refer to Figure 2 in B. Goll and H. Zimmermann, “A Comparator with Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65V,” IEEE Transactions on Circuits and Systems - II, vol. 56, no. 11, Nov. 2009, pp. 810-814.

The comparators should realize a flip-flop function.
   a. As shown in Figure 1, for the Strong-Arm type latches (1,3, and 4) follow with the optimized SR-latch shown in Figure 2. For more details on the optimized SR-latch, refer to B. Nikolic *et al*., “Improved Sense-Amplifier-Based Flip-Flop: Design and Measurements,” IEEE Journal of Solid-State Circuits, vol. 35, no. 6, June 2000, pp. 876-884. **Note: for architecture (3) you will need to modify this optimized SR-latch – as the sense-amp pre-charges to GND (vs VDD in 1 & 4).**
   b. To realize a CML flip-flop with architecture (2), simply cascade 2 CML latches to realize a master-slave flip-flop.
2. **High-Speed Comparator Characterization.** For the 4 comparator architectures designed in problem 1, produce the following:
   a. **Plot comparator delay vs VDD** for VDD varying from 50% of nominal VDD to 100% VDD. For this keep the input common mode equal to 80% of the supply, i.e. sweep the input common-mode along with the supply. Also scale the clock input signal level with VDD.
   b. **Plot comparator power vs VDD** in a similar manner.
   c. **Generate the comparator Impulse Sensitivity Function (ISF) at the nominal VDD, 80%VDD and 60%VDD (3 curves).** Again, track the input common-mode with VDD. To do this use the equivalent test circuit in Slide 9 of Lecture 14, for more details refer to M. Jeeradit et al., “Characterizing Sampling Aperture of Clocked Comparators,” *IEEE VLSI Symposium*, June 2008. For the characterization try an input differential step input of 50mV, i.e. $V_{CM} \pm 25mV$ for the differential input signals. **Report the comparator aperture time**, with the assumption that it is the width of the ISF that contains 80% of the sensitivity.

3. **Choose a comparator design.** Given the results from problems 1 & 2, choose the comparator design which you feel is best suited for a low-power ¼ rate RX architecture working at 10Gb/s with the 4 parallel comparators clocked at 2.5GHz. Assume you have the flexibility to scale down VDD for increased power savings. Note: No additional design is required for this problem, just justify your choice.