Texas A&M University
Department of Electrical and Computer Engineering

ECEN 720 – High-Speed Links

Spring 2021

Exam #1

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are **6** pages in your exam
- Good Luck!

Problem	Score	Max Score
1		30
2		20
3		25
4		25
Total		**100**

Name: SAM PALERMO

UIN: _____

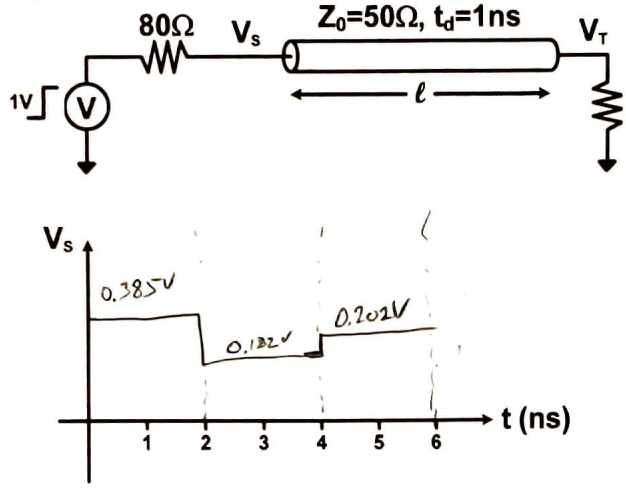
Problem 1 (30 points)

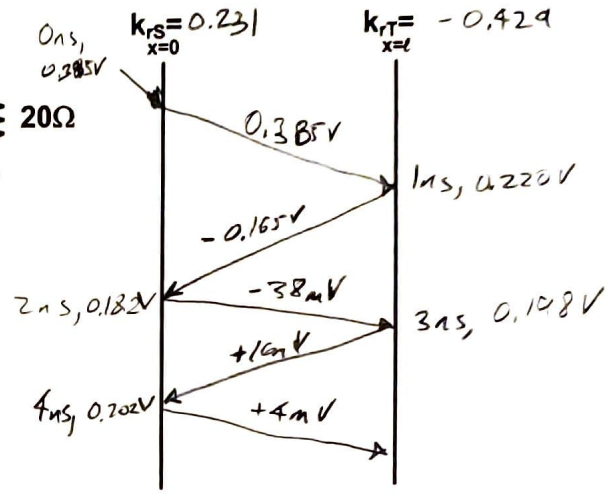
a) A 1V step is launched onto the channel below at t=0ns. (20 points)

i. Calculate the reflection coefficient at the source, k_{rS}, and the end termination, k_{rT}

ii. Fill in the lattice diagram below until the source voltage, Vs, has reached to within 10mV of its final value.

iii. Also plot the source voltage, Vs, and make sure to label the voltage values in the transient plot.

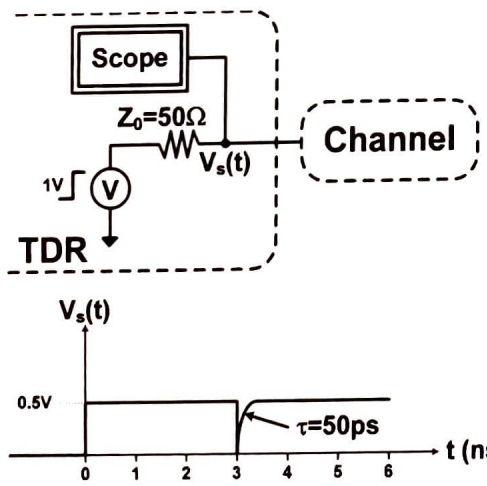


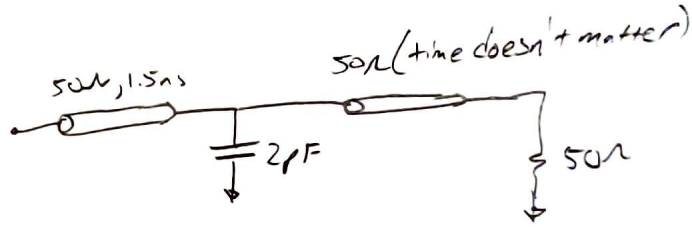


Initial Voltage $= \frac{50}{80+50}(1V) = 0.385V$, Final Voltage $= \frac{20}{80+20}(1V) = 0.2V$

$K_{rS} = \frac{80-50}{80+50} = 0.231$ $\quad K_{rT} = \frac{20-50}{20+50} = -0.429$

b) An ideal TDR ($t_r \sim 0$) measurement of an unknown channel displays the following waveform below. Sketch the channel model and give values for any lumped elements and transmission line characteristic impedance and length (in time). Assume all transmission lines are loss-less. (10 points)





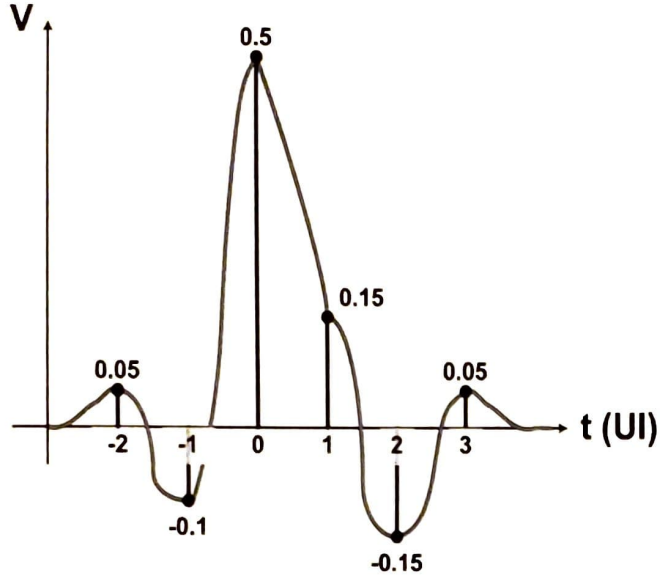
Downward spike means shunt capacitive discontinuity

$\tau = \frac{Z_0 C}{2} \Rightarrow C = \frac{2\tau}{Z_0}$

$C = \frac{2(50ps)}{50\Omega} = 2pF$

Problem 2 (20 points)
A channel has the pulse response, $y^{(1)}$, below for a "1" bit.
a. Find the channel's worst-case eye height at this bit rate.
b. Give the channel's worst-case bit pattern at this bit rate.

$$y^{(1)} = [0.05\ \ -0.1\ \ 0.5\ \ 0.15\ \ -0.15\ \ 0.05]$$



$y_0^{(1)} = 0.5$

$\sum_{k\neq 0} y^{(1)}\Big|_{y<0} = -0.1 - 0.15$

$= -0.25$

$\sum_{k\neq 0} y^{(1)}\Big|_{y>0} = 0.05 + 0.15 + 0.05$

$= 0.25$

W.C. Eye Height = $2(0.5 - 0.25 - 0.25) = 0$

To find W.C. Bit Pattern:

Flip about cursor and invert all but cursor

$[0.05\ \ -0.1\ \ 0.5\ \ 0.15\ \ -0.15\ \ 0.05] \Rightarrow [-0.05\ \ 0.15\ \ -0.15\ \ 0.5\ \ 0.1\ \ -0.05]$

Then take sign

$[-0.05\ \ 0.15\ \ -0.15\ \ 0.5\ \ 0.1\ \ -0.05] \Rightarrow [-1\ \ 1\ \ -1\ \ 1\ \ 1\ \ -1]$

Worst-Case Eye Height = 0

Worst-Case Bit Pattern = $[-1\ \ 1\ \ -1\ \ \underset{\uparrow}{1}\ \ 1\ \ -1]$ (W.C. "1")

$[1\ \ -1\ \ 1\ \ \underset{\uparrow}{-1}\ \ -1\ \ 1]$ (W.C. "-1")

Cursors

Problem 3 (25 points)

For the circuit below, use the following NMOS parameters

$KP_N=\mu_nC_{ox}=600\mu A/V^2$, $V_{TN}=0.35V$, $\lambda_N=0V^{-1}$

and the following PMOS parameters

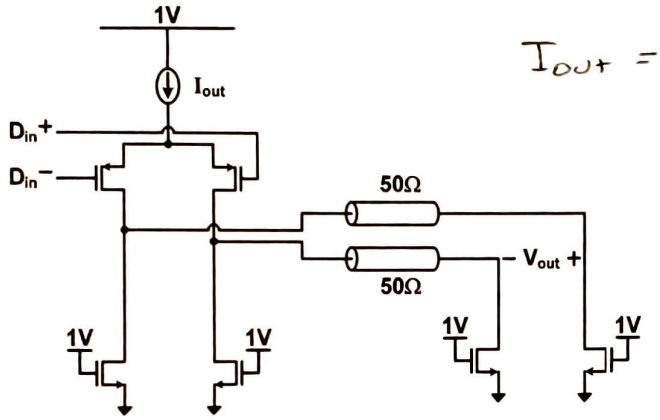
$KP_P=\mu_pC_{ox}=150\mu A/V^2$, $V_{TP}=-0.35V$, $\lambda_P=0V^{-1}$

For the current-mode driver below

i. Calculate the tail current I_{out} to generate a peak-to-peak differential voltage output swing of $400mV_{ppd}$. Here assume that the NMOS termination transistors are perfectly linear.

ii. Give the common-mode value of the output voltage with the $400mV_{ppd}$ output swing. Again, assume that the NMOS termination transistors are perfectly linear.

iii. Give the NMOS termination transistors aspect ratios for proper termination. Include V_{DS} effects and optimize the termination at the ideal output common-mode level of part (ii). Assume that the PMOS switch transistors remain in saturation.



$$I_{out} = \frac{V_{ppd}}{R} = \frac{400mV}{50\Omega} = 8mA$$

"1" bit

$V_{out}^+ = 4mA(50\Omega) = 0.2V$

$V_{out}^- = 0V$

"-1" bit

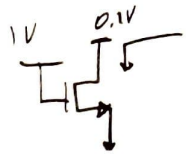
$V_{out}^+ = 0V$

$V_{out}^- = 4mA(50\Omega) = 0.2V$

$$V_{out,cm} = \frac{0.2V-0V}{2} = 0.1V$$

* Sizing NMOS termination at common-mode level

Looking into drain of NMOS in deep triode



$$R_N = \frac{1}{g_D} = \frac{1}{KP_N\frac{W}{L}(V_{GS}-V_T-V_{DS})}$$

$$\frac{W}{L} = \frac{1}{R_N K_{PN}(V_{GS}-V_T-V_{DS})} = \frac{1}{(50\Omega)(600\mu A/V^2)(1V-0.35V-0.1V)}$$

$I_{out} = 8mA$

$V_{out,CM} = 0.1V$

$(W/L)_N = 60.6$

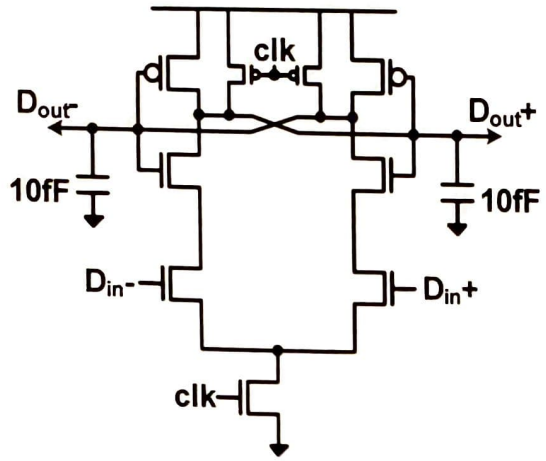
* PMOS transistors remain in saturation, so shouldn't impact output termination

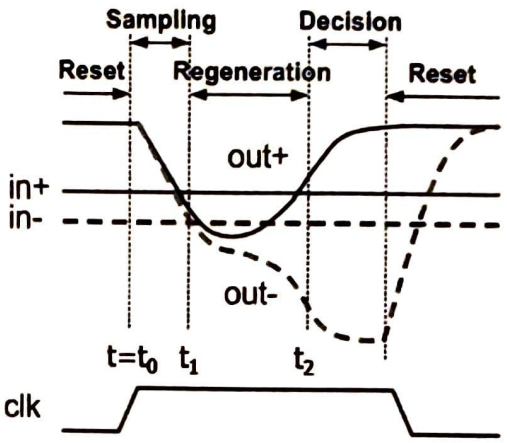
Problem 4 (25 points)

This problem involves designing the below comparator to **make a decision in 160ps from the time the clock goes high.** Assume that the **Sample Time=20ps** and the **Sample Gain=1.** Assume that all the capacitors are represented by the explicitly drawn capacitors.

i. What regeneration time constant, τ_R, is required to amplify a 10mV differential input voltage to the 500mV required to make a decision?

ii. Given the **total** output capacitance of the comparator is 10fF, what is the effective total regeneration transconductance, g_{mr}, required for this time constant, τ_R?





Decision Time = Sample + Regeneration Time $\leq$ 160ps

$\Rightarrow$ Regen Time $\leq$ 140ps

Necessary Regeneration Gain, $G_R = \frac{500mV}{10mV} = 50$

$$G_R = e^{\frac{\text{Regen Time}}{\tau_R}} = 50$$

$$\tau_R = \frac{140ps}{\ln(50)} = 35.8ps$$

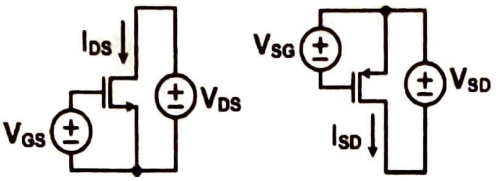
$$\tau_R = \frac{C_{out}}{g_{mr}} = 35.8ps$$

$$g_m = \frac{10fF}{35.8ps} = 279\mu A/V$$

$\tau_R = 35.8ps$

$g_{mr} = 279\mu A/V$

Key MOS Equations & Scratch Paper



Saturation: $NMOS\ I_{DS} = \frac{1}{2} KP_N \frac{W}{L} (V_{GS} - V_{TN})^2$

Saturation: $PMOS\ I_{SD} = \frac{1}{2} KP_P \frac{W}{L} (V_{SG} - |V_{TP}|)^2$

Triode: NMOS $I_{DS} = KP_N \frac{W}{L} \left(V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right) V_{DS}$

Triode: $PMOS\ I_{SD} = KP_P \frac{W}{L} \left(V_{SG} - |V_{TP}| - \frac{V_{SD}}{2} \right) V_{SD}$

$$NMOS\ g_m = \frac{\partial I_{DS}}{\partial V_{GS}},\quad PMOS\ g_m = \frac{\partial I_{SD}}{\partial V_{SG}}$$

$$NMOS\ g_o = \frac{\partial I_{DS}}{\partial V_{DS}},\quad PMOS\ g_o = \frac{\partial I_{SD}}{\partial V_{SD}}$$