Texas A&M University
Department of Electrical and Computer Engineering

ECEN 720 – High-Speed Links

Spring 2019

Exam #1

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are **6** pages in your exam
- You may use <u>one</u> double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		30
2		20
3		30
4		20
Total		**100**

Name: SAM PALERMO

UIN:

Problem 1 (30 points)

a) A 1V step is launched onto the channel below at t=0ns. (20 points)

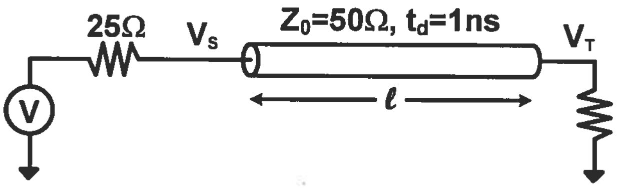
i. Calculate the reflection coefficient at the source, k_{rS}, and the end termination, k_{rT}

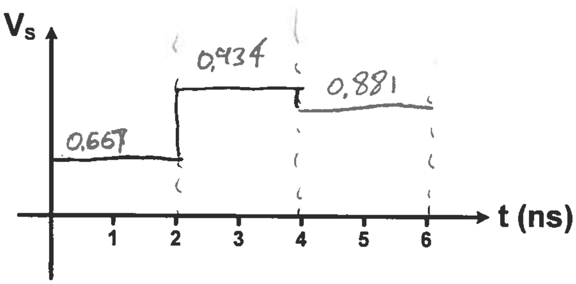
ii. Fill in the lattice diagram below until the source voltage, V_S, has reached to within 20mV of its final value.

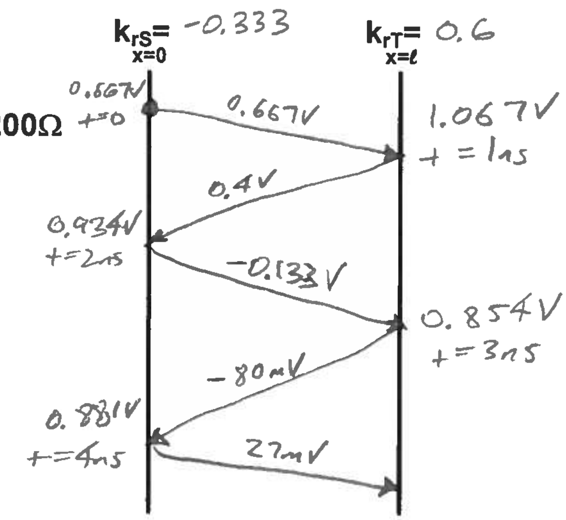
iii. Also plot the source voltage, V_S, and make sure to label the voltage values in the transient plot.

Initial Voltage $= \frac{50}{75} = 0.667V$

Final Voltage $= \frac{200}{225} = 0.889V$

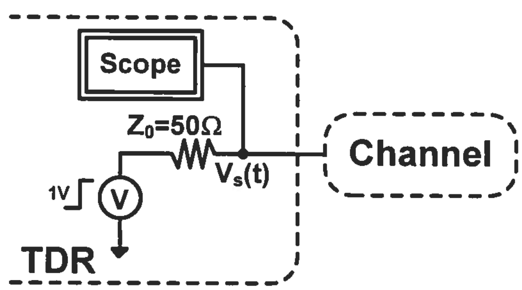


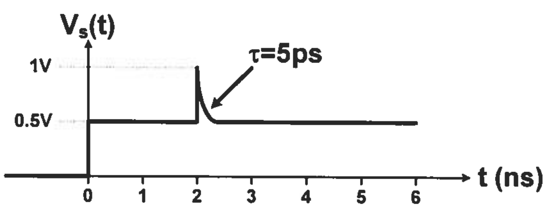


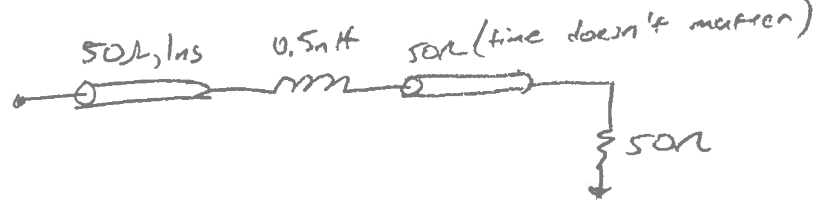


$$K_{rS} = \frac{25-50}{25+50} = -0.333, \quad K_{rT} = \frac{200-50}{200+50} = 0.6$$

b) An ideal TDR (t_r~0) measurement of an unknown channel displays the following waveform below. Sketch the channel model and give values for any lumped elements and transmission line characteristic impedance and length (in time). Assume all transmission lines are loss-less. (10 points)







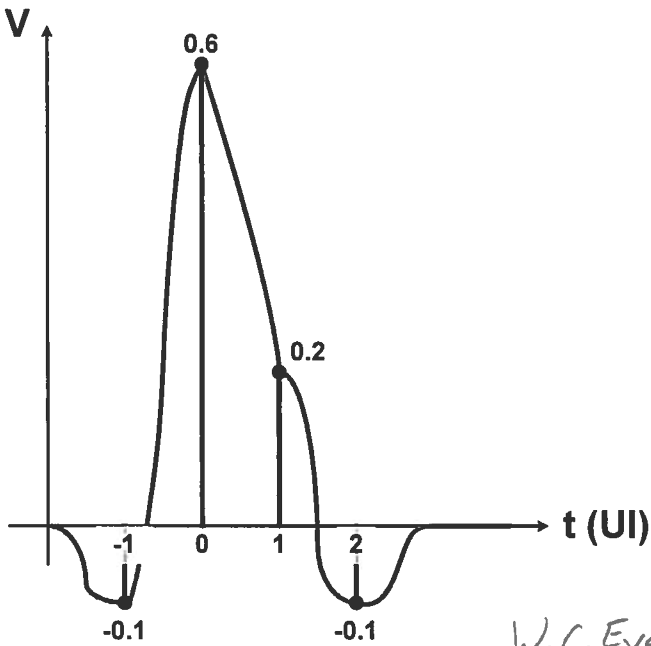
Upward spike means inductive discontinuity

$$\tau = \frac{L}{2Z_0} = \frac{L}{2(50\Omega)} = 5ps$$

$$L = 2(50\Omega)(5ps) = 0.5nH$$

Problem 2 (20 points)
A channel has the pulse response, $y^{(1)}$, below for a "1" bit.

a. Find the channel's worst-case eye height at this bit rate.
b. Give the channel's worst-case bit pattern at this bit rate.



$y_0^{(1)} = 0.6$

$\sum_{k \neq 0} y^{(1)} \Big|_{y<0} = -0.1 - 0.1 = -0.2$

$\sum_{k \neq 0} y^{(1)} \Big|_{y>0} = 0.2$

W.C. Eye Height $= 2(0.6 - 0.2 - 0.2) = 0.4$

To find W.C. Bit Pattern:

Flip about cursor and invert all but cursor

$[-0.1 \ \ 0.6 \ \ 0.2 \ \ -0.1] \Rightarrow [0.1 \ \ -0.2 \ \ 0.6 \ \ 0.1]$

Then take sign

$[0.1 \ \ -0.2 \ \ 0.6 \ \ 0.1] \Rightarrow [1 \ \ -1 \ \ 1 \ \ 1]$

Worst-Case Eye Height = 0.4

main cursor

Worst-Case Bit Pattern = $[1 \ \ -1 \ \ 1 \ \ 1]$ (Worst-Case "1")

$[-1 \ \ 1 \ \ -1 \ \ -1]$ (Worst-Case "-1")

by linearity

Problem 3 (30 points)

This problem involves the design of a voltage-mode driver to meet the given peak-to-peak differential output voltage swing specifications. For part (a) and (b) choose the driver (#1 or #2) which is best suited for the given output voltage swing, give the output stage supply, and give the output stage transistors aspect ratios (W/L) to implement proper source termination.

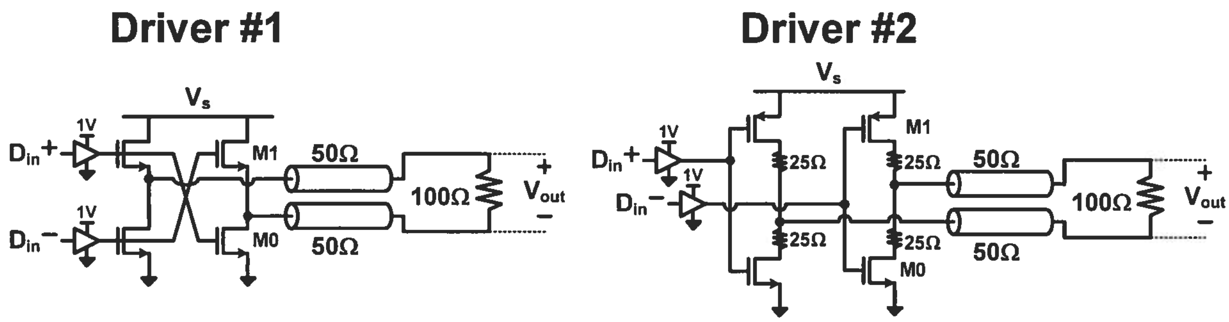
Assume that it is sufficient to optimize the source termination for transmitting a static "1" or "-1" bit and that the predrive buffers swing from 0 to 1V. Include V_{DS} and V_{SD} effects.

For all circuits below, use the following NMOS parameters

$KP_N=\mu_n C_{ox}=600\mu A/V^2$, $V_{TN}=0.35V$, $\lambda_N=0V^{-1}$

and the following PMOS parameters

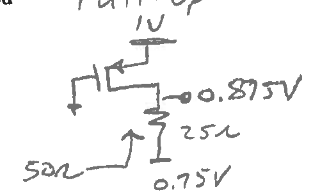
$KP_P=\mu_p C_{ox}=150\mu A/V^2$, $V_{TP}=-0.35V$, $\lambda_P=0V^{-1}$

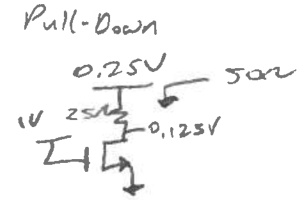


a) Output voltage swing = **1V$_{ppd}$**

In both pull-up and pull-down transistors are in deep triode

$R_{tran} = \frac{1}{g_{ds}}$





NMOS : $R_0 = \frac{1}{KP_N\left(\frac{W}{L}\right)_0 (V_{GS} - V_{TN} - V_{DS})}$

$\frac{W}{L_0} = \frac{1}{(600\mu)(25)(1-0.35-0.125)} = 127$

PMOS : $R_1 = \frac{1}{KP_P\left(\frac{W}{L}\right)_1 (V_{SG} - |V_{TP}| - V_{SD})}$

$\frac{W}{L_1} = \frac{1}{(150\mu)(25)(1-0.35-0.125)} = 508$

Driver = 2

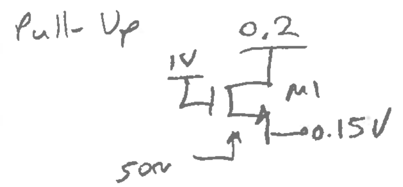
V_S = 1V

$(W/L)_0$ = 127

$(W/L)_1$ = 508

b) Output voltage swing = **200mV$_{ppd}$**

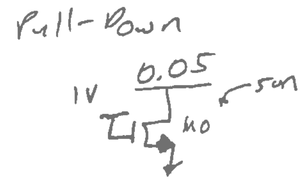
Both Transistors in Deep Triode



$R = \frac{1}{g_m + g_{ds}} = 50\Omega$

$R = \frac{1}{KP_N\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TN})}$

$\left(\frac{W}{L}\right)_1 = \frac{1}{(600\mu)(50)(0.85-0.35)} = 66.7$



$R = \frac{1}{g_{ds}} = 50\Omega$

$R = \frac{1}{KP_N\left(\frac{W}{L}\right)_0 (V_{GS} - V_{TN} - V_{DS})}$

$\left(\frac{W}{L}\right)_0 = \frac{1}{(600\mu)(50)(1-0.35-0.05)} = 55.6$

Driver = 1

V_S = 0.2V

$(W/L)_0$ = 55.6

$(W/L)_1$ = 66.7

Problem 4 (20 points)

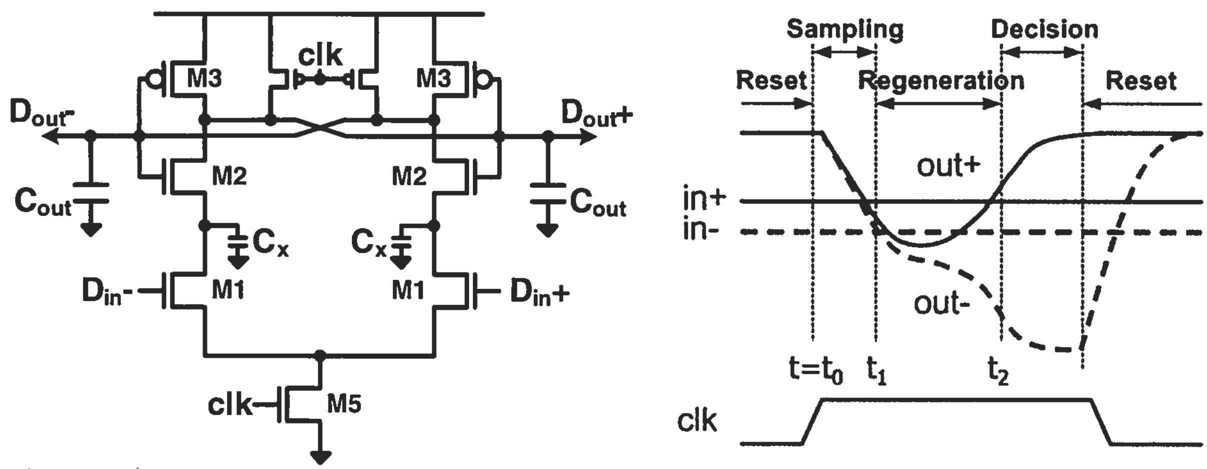
This problem involves analyzing the maximum performance of the comparator below. Assume that the **Sample Time=25ps, C_{out} = C_x = 10fF,** and that all capacitors are represented by the explicitly drawn capacitors.

i. Assume that in sampling mode the effective transconductance of M1 and M2 are equal, i.e. $g_{m1}=g_{m2}=g_{m,samp}$. What is the required effective sampling transconductance to realize a small-signal sampling gain of 2 for a constant differential input voltage over the 25ps sampling time?

Hint: During sampling-mode the small-signal transfer function can be approximated as

$$\frac{v_{out}(s)}{v_{in}(s)} \cong \frac{g_{m1}g_{m2}}{s^2 C_{out} C_x} = \frac{g_{m,samp}^2}{s^2 C_{out} C_x}$$

ii. Given the effective total regeneration transconductance g_{mr}=500μA/V, a sampling gain of 2, and it is required to amplify a constant 10mV differential input voltage to 500mV for a reliable decision, what is the minimum time required to make a decision ($t_2 - t_0$)?



In sampling mode

i. $\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{m,samp}^2}{s^2 C_{out} C_x}$ w/constant input $\Longrightarrow$ $\frac{V_{out}(t)}{V_{in}} = \frac{g_{m,samp}^2}{C_{out} C_x} \frac{t^2}{2}$

For sampling gain of 2

$\frac{g_{m,samp}^2}{C_{out}C_x}\frac{t^2}{2} = 2 \Longrightarrow g_{m,samp} = \sqrt{\frac{4 C_{out} C_x}{t^2}} = \sqrt{\frac{4(10f)(10f)}{(25ps)^2}} = 800 \mu A/V$

ii. Given a sampling gain of 2, the comparator will need to regenerate

$2(10mV) = 20mV$ to 500mV to make a decision.

Regen Time $= \frac{C_{out}}{g_m} \ln\left(\frac{500mV}{20mV}\right) = \left(\frac{10fF}{500\mu A/V}\right)\ln\left(\frac{500mV}{20mV}\right)$

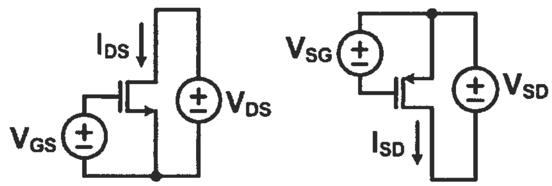
Decision Time = Sample Time + Regen Time =

$25ps + 64.4ps = 89.4ps$

$g_{m1} = g_{m2} = g_{m,samp} =$ 800μA/V

Min ($t_2 - t_0$) = 89.4ps

Key MOS Equations & Scratch Paper



$$\text{Saturation: } NMOS\ \ I_{DS} = \frac{1}{2} KP_N \frac{W}{L} (V_{GS} - V_{TN})^2$$

$$\text{Saturation: } PMOS\ \ I_{SD} = \frac{1}{2} KP_P \frac{W}{L} (V_{SG} - |V_{TP}|)^2$$

$$\text{Triode: NMOS } I_{DS} = KP_N \frac{W}{L} \left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right) V_{DS}$$

$$\text{Triode: } PMOS\ I_{SD} = KP_P \frac{W}{L} \left(V_{SG} - |V_{TP}| - \frac{V_{SD}}{2}\right) V_{SD}$$

$$NMOS\ g_m = \frac{\partial I_{DS}}{\partial V_{GS}},\quad PMOS\ g_m = \frac{\partial I_{SD}}{\partial V_{SG}}$$

$$NMOS\ \ g_o = \frac{\partial I_{DS}}{\partial V_{DS}},\quad PMOS\ \ g_o = \frac{\partial I_{SD}}{\partial V_{SD}}$$