To generate 2.5Gbps data, 2.5GHz Clock has to be connect to the clock of DFF.

Ideal Logic components (DFF, XNOR, and XOR gate) have in ahdLib, which we are getting for random generation component

\[
\begin{align*}
\text{Data } 1[n-1] &= D5[n] \\
\text{Data2 } [n-1] &= \text{XNOR}(\text{Data1}[n], \text{Data3}[n]) \\
\text{Data3 } [n-1] &= \text{XOR}(\text{Data2}[n], \text{Data4}[n]) \\
\text{Data4 } [n-1] &= \text{XOR}(\text{Data3}[n], \text{Data5}) \\
\text{D5 } [n-1] &= \text{XOR}(\text{Data4}[n], \text{XNOR}(\text{Data1}[n+1], \text{Data3}[n+1])) \\
\end{align*}
\]

D5 internally used for 4 bit Parallel PRBS generation.
4 bit Parallel PRBS Detection

Simulation Result

*2.5GHz Clock has to be connect DFF