ECEN 720 High-Speed Links: Circuits and Systems

Lab6 – Link Modeling with ADS

Objective

To learn statistical bit-error-rate (BER) simulation, BER link noise budgeting and using ADS to model high speed I/O link circuits

Introduction

Previously, the throughput of a SPICE-like simulator was thousands of bits per minute of simulation time when only design parameters were the channel characteristics, in addition to a few settings on the TX and RX. In contrast, when the transient simulation is performed with logic blocks containing 10-50,000 transistors for today's transceivers that contain deskew circuitry, various equalizers, and RX clock data recovery (CDR) as shown in Figure 1, the throughput drops dramatically: only tens or at best hundreds of bits per minute of simulation time. It can take tens of hours or even several days to collect enough result bits to form a useful eye diagram.

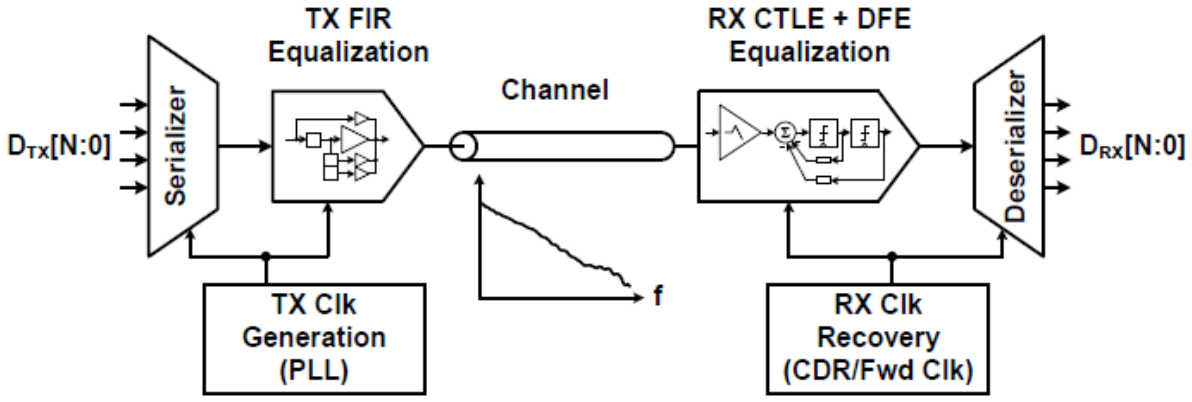
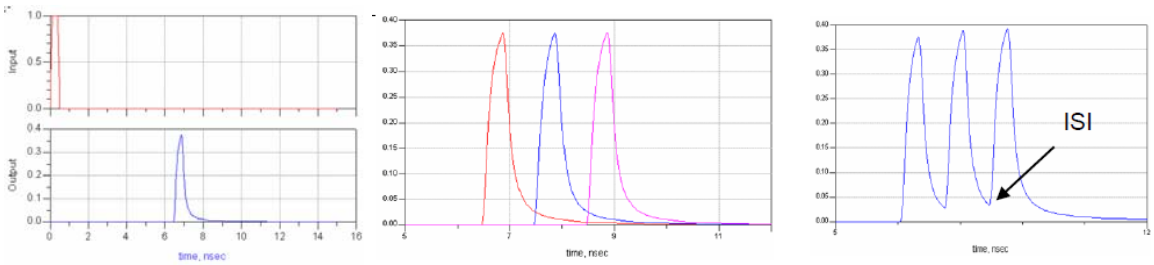


Figure 1 High-Speed Electrical Link with Equalization Schemes

To find optimum integration of the link system for a data channel, signal integrity (SI) engineers must run hundreds of long running simulations each of which must provide a figure of merit based on eye height/width, and ultra-low bit error rate (BER) contours. To minimize computation time, the traditional channel characterization is being replaced by innovative algorithms. Today, channels are characterized by a step or (im)pulse response—a method that is used by ADS Channel Simulator in statistical mode as shown in Figure 3. Instead of performing a long time-domain simulation with a PRBS source, only a single rising/falling edge is simulated.



(a) (b)

Figure 2 (a) Step Response. (b) Bit-by-Bit Mode: Superposition of Bits

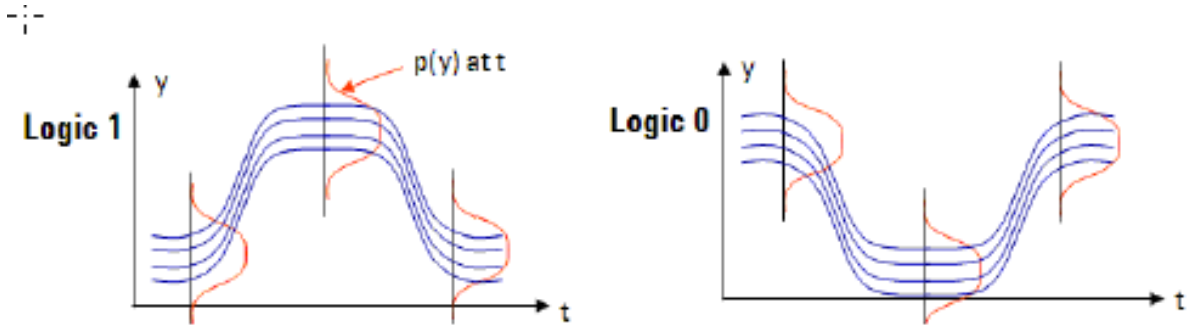


Figure 3 Statistical Mode for BER Simulation

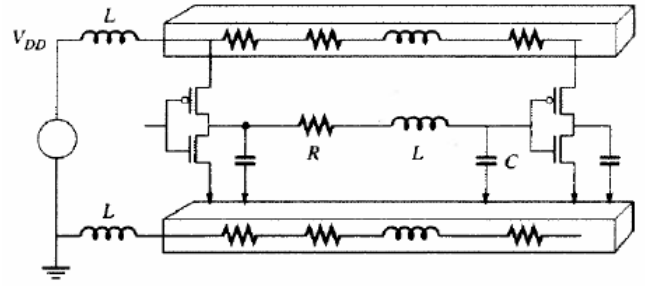
This approach results in short simulation time. The Agilent's ADS offers the big advantage of this method. This statistical tool can add random jitter for TX and RX and calculate BER contours and bathtub curves. Pre-emphasis/de-emphasis in TX and other equalization methods in RX can be incorporated. The Table below summarizes the pros and cons of traditional transient simulator as well as Channel Simulator in Bit-by-bit and Statistical modes [3].

Table 1 Comparison of Traditional Transient Simulator and Channel Simulator in Bit-by-Bit and Statistical Modes

	Transient Simulator	**Channel Simulator: Bit-by-bit mode**	**Channel Simulator: Statistical mode**
Method	Modified nodal analysis of Kirchoff's current laws for every time step	Bit-by-bit superposition of step responses	Statistical calculation based on step response
Applicability	Linear and non-linear circuits	LTI, any specific bit pattern, adaptive eq. taps, IBIS AMI	LTI, fixed (general) bit patter, fixed eq. taps
BER floor in 1-minute-simulation	~1e-3	~1e-6	Arbitrarily low

Power Supply Noise

Power supply is one of the largest noise sources in a typical digital system. Insufficient supply grid and fast switching circuit may cause IR drop and dI/dt noise. Power supply noise can affect signaling in many ways. It may cause signals to fall outside the receiver operating range due to common-mode voltage shifts between supplies. It may corrupt the signals that use a power supply as a voltage reference. Local power supply variation may result in transmitter and receiver offsets and jitter. Figure 4 shows an example of finite supply impedance. The supplies seen by the inverter are no longer the ideal voltage. Instead, parasitic resistance and inductance are inserted into the supply distribution network.



[Hodges]

Figure 4 Finite Supply Impedance

Bonding wire and Pad Parasitic

Wire bonding is extremely used in IC packaging. Parasitic inductance and capacitance of IC packages impose limits on the performance of circuits at high frequency or data rate [1]. Packaging can result in significant impedance discontinuity due to self-inductance (~1nH/mm), mutual inductance (up to ~50% of self-inductance depending on the separation of the wires), and series-resistance from the bonding wire (~0.1 Ohm/mm) as shown in Figure 5.

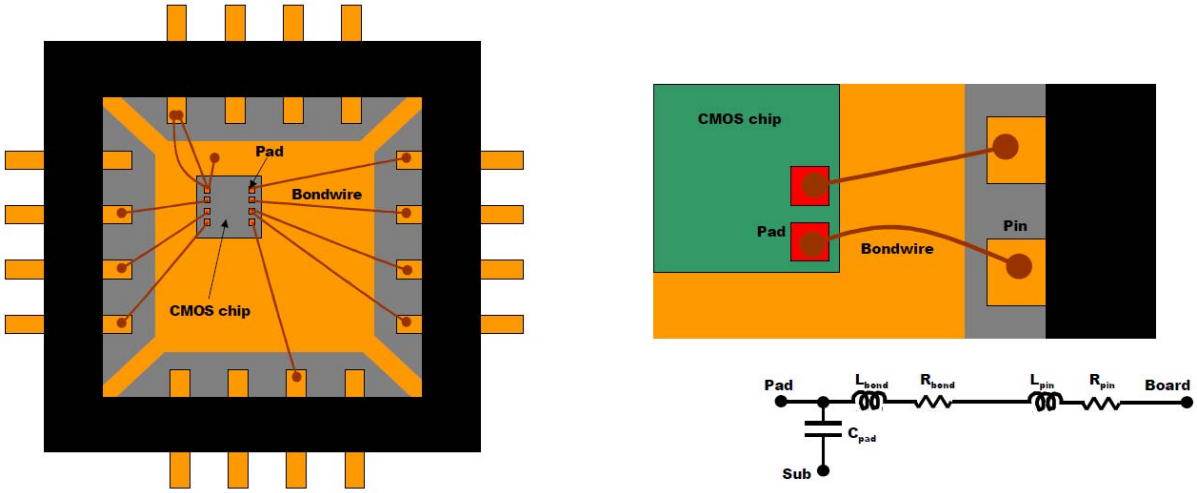


Figure 5 VLSI Packaging Diagram and Equivalent Parasitic Circuit

System Noise and Jitter Budget

During link design, signal swing and data rate are budgeted against noise sources both bounded and unbounded. For the bounded noise, in most digital system design, worst-case analysis is used. All bounded noise sources are added simultaneously at the worst possible extreme value.

$$system\ total\ noise_{bounded} = \sum_i noise_{bounded}\,(i) \tag{1}$$

For the unbounded noise, statistical noise analysis is applied to estimate the probability distributions of the statistical noise sources. When considering unbounded Gaussian noise sources (normal distribution), several Gaussian noise sources can be combined into a single noise source through summing the variance of each source and taking the square root of it as follows:

$$\sigma_{RMS}(sys) = \left(\sum_i \sigma_{RMS}^2\right)^{0.5} \tag{2}$$

During the system jitter budget, for a system to achieve a minimum BER performance, the total jitter should be less than one UI as follows

$$UI \geq DJ_{\delta\delta}(sys) + Q_{BER}\sigma_{RMS}(sys) \tag{3}$$

where $DJ_{\delta\delta}(sys)$ is the total deterministic jitter, and Q is calculated from the target BER. The following tables show an example of system jitter budgeting.

TABLE 13-2. PCI Express 2.5-Gb/s Jitter Budget at 10^{-12} BER

Component	Term	σ_{RJ} (ps)	$DJ_{\delta\delta}$ (ps)	TJ (ps)
Reference clock	TJ_{clock}	4.7	41.9	108
Transmitter	TJ_{TX}	2.8	60.6	100
Channel	$TJ_{channel}$	0	90	90
Receiver	TJ_{Rx}	2.8	120.6	160
Linear TJ				458
RSS TJ	6.15 * 14.069 = 86.5		313.1	399.6

TABLE 13-1. Q_{BER} as a Function of the Bit Error Rate

BER	Q_{BER}	BER	Q_{BER}	BER	Q_{BER}
1×10^{-3}	6.180	1×10^{-10}	12.723	1×10^{-17}	16.987
1×10^{-4}	7.438	1×10^{-11}	13.412	1×10^{-18}	17.514
1×10^{-5}	8.530	1×10^{-12}	14.069	1×10^{-19}	18.026
1×10^{-6}	9.507	1×10^{-13}	14.698	1×10^{-20}	18.524
1×10^{-7}	10.399	1×10^{-14}	15.301	1×10^{-21}	19.010
1×10^{-8}	11.224	1×10^{-15}	15.882	1×10^{-22}	19.484
1×10^{-9}	11.996	1×10^{-16}	16.444	7.7×10^{-24}	20.000

[Hall]

For the noise budget calculation, please refer to our lecture notes.

Near-End and Far-End Cross Talk

The capacitive and inductive coupling between lines A and B result in cross talk at both ends of line B. An example is shown in Figure 6. Assuming a step signal is generated on line A at point u, it propagates to the receiver side point v. The unwanted signal is coupled to line B from x to y. The forward-traveling wave on line B induced by line A arrives at point z at the far-end of line B. So, it is called Far-End Cross Talk (FEXT). The reverse-traveling wave induced on line B arrives at point w at the near-end of line B. Thus, it is called Near-End Cross Talk (NEXT).

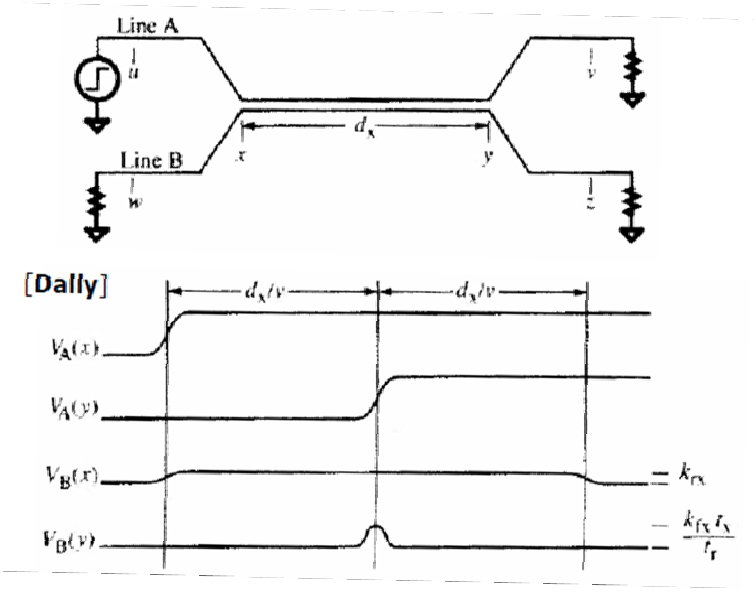


Figure 6 Line Geometry (Up) and Waveforms (Down) for a Cross Talk Example

Initial ADS Setup and Creating a Workspace

The ADS is installed in the ECE's Apollo/Hera server. Make sure your default shell is the C shell. To change the shell from bash to csh, type "csh" on the prompt. To launch the ADS, edit the ".cshrc" file in the root directory of your UNIX account by adding a line,

source /softwares/setup/ads/setup.ads2015.linux

Then, create your ADS work directory before launching the software by executing "ads" as follows,

```
>>mkdir  ADS_works
>>cd  ADS_works
>>ads
```

Figure 7 Getting Started with ADS Window

When the “Getting started with ADS” window pops up click on the “Create a new workspace” as shown in Figure 7.

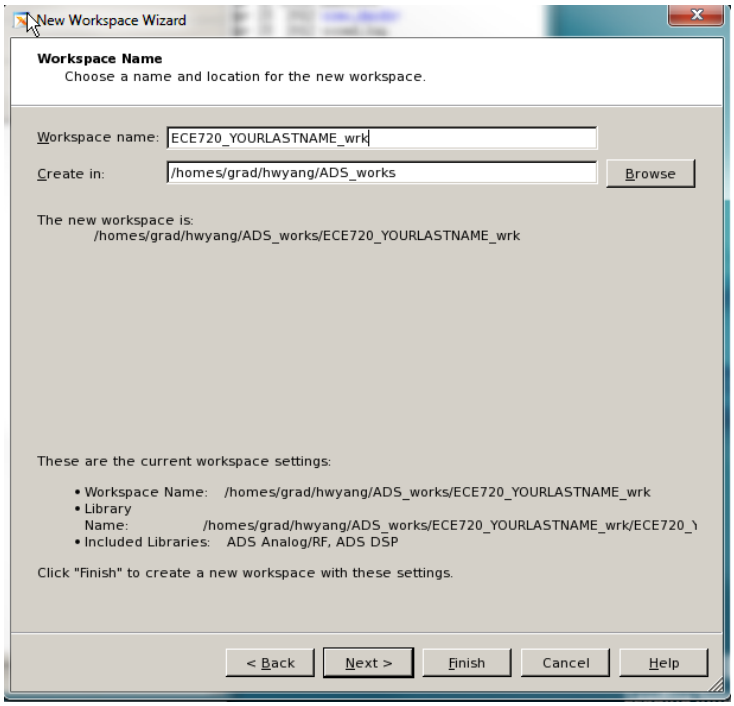


Figure 8 Workspace Wizard Window

Edit the workspace name with your last name for the electronic submission as shown in Figure 8. Finally, make a library name and finish the process by clicking the finish button as shown in Figure 9. In this example, you don’t need to move on to Next in order to attach any technology.

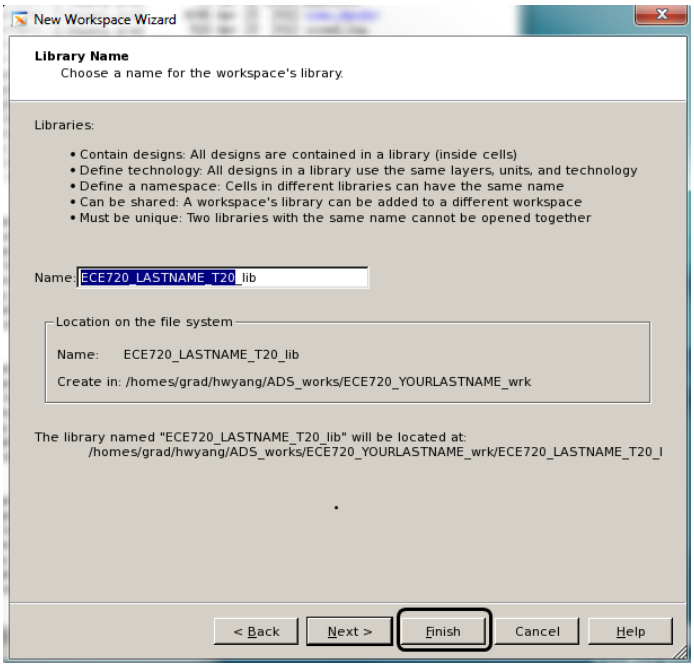


Figure 9 Creating a Library from New Workspace Wizard

Example 1

In this first example, a simple ADS channel modeling simulation will be performed at 4Gb/s. 20" backplane channel with RJ and duty-cycle distortion (DCD) in TX with 2-tap TX equalization 3dB de-emphasis. Channel frequency response and eye diagram will be plotted. We use T20 channel (THRU, NEXT1, and FEXT1) for link modeling. The 4-channel scattering parameters in Touchstone format can be downloaded from the course website. Copy those files into the workspace or library directory.

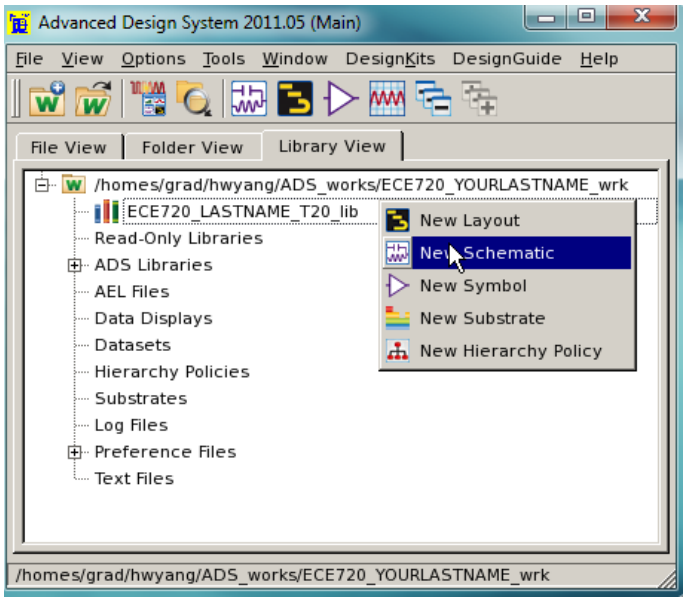


Figure 10 Creating a New Schematic from The Main ADS Window

On the ADS main window, create a new schematic by right-clicking the library name as shown in Figure 10. When the schematic window pops up, name the cell (for example "T20_thru") and press OK.

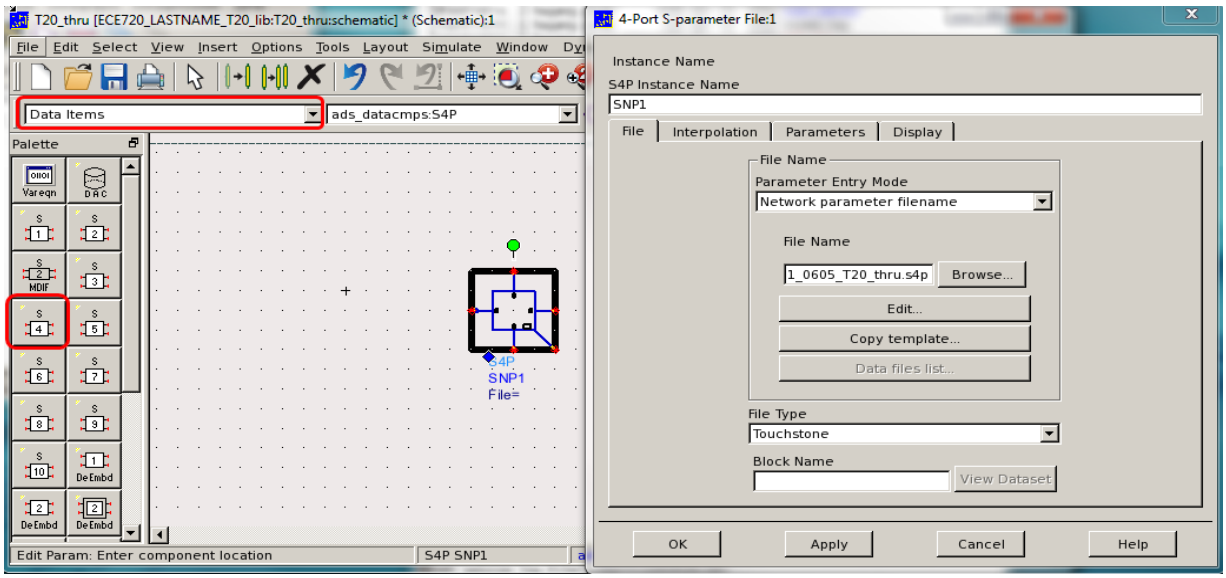


Figure 11 Importing a Scattering Parameter

The first cell in this example includes a schematic and a symbol. This cell is used for importing S-parameter for the 20" backplane forward channel. Import "peters_01_0605_T20_thru.s4p" touchstone file after dragging the S4P cell in the Data Items library as highlighted in Figure 11.

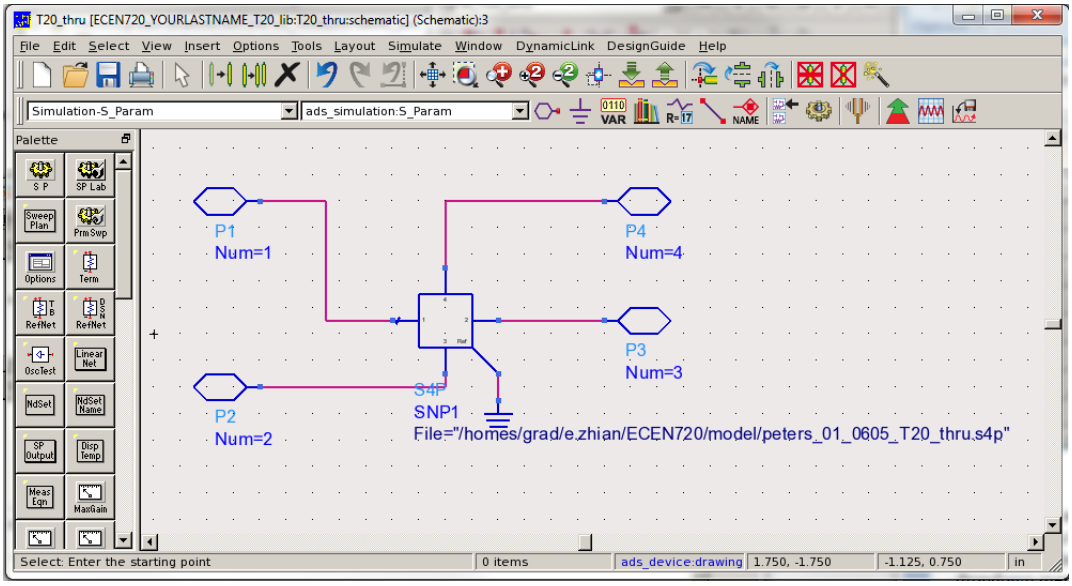


Figure 12 Schematic of The T20 Channel Using S4P Block

Complete the schematic with pins as shown in Figure 12. Note, channel ports are differential and they are mapped in these Touchstone s4p files by (1,3) as the input port and (2,4) as the output port. Close the schematic and create the symbol for the cell by right-clicking the cell name and choosing *New Symbol* from the dropdown menu as shown in Figure 13.

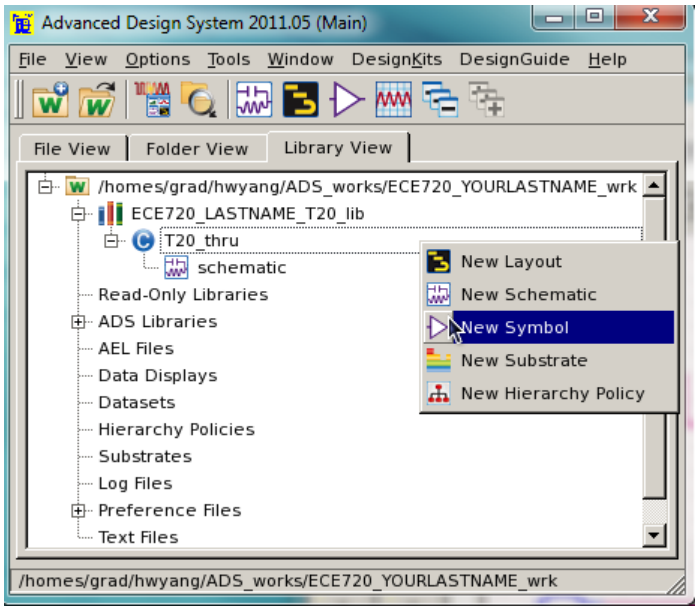


Figure 13 Creating a Symbol from The ADS Main Window

From the *Symbol Generator* you can predefine the symbol as shown in Figure 14.

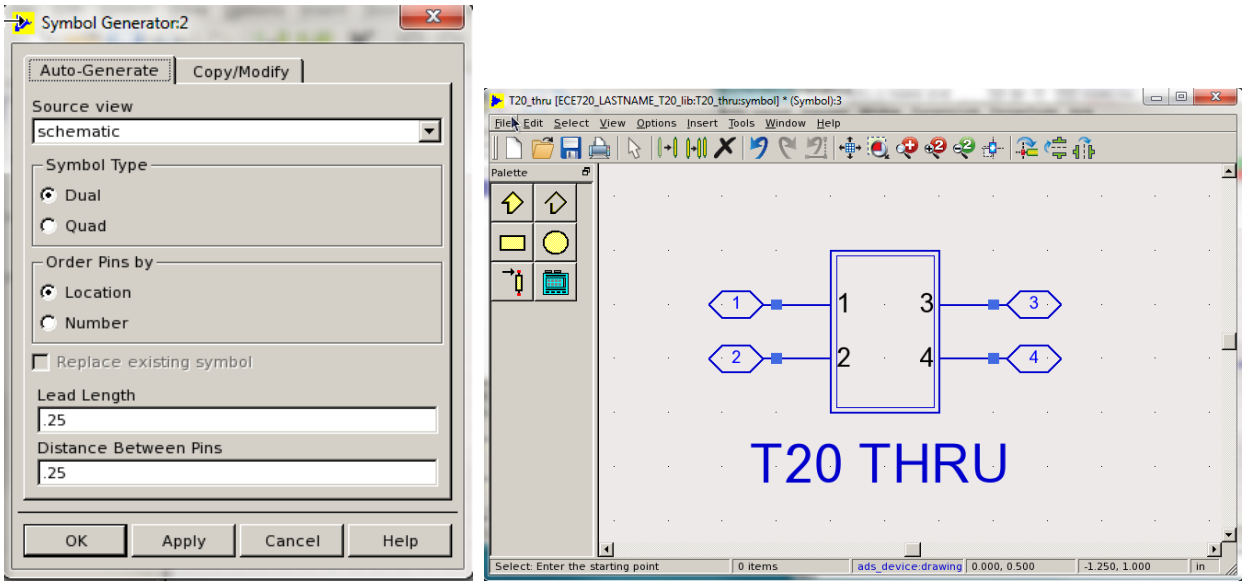


Figure 14 Creating Symbol for T20 Cell

Save and close the symbol after confirming the symbol shape.

As you created the cell, you can instantiate the cell in the higher level of hierarchy. Create a new schematic and drag the symbol to the new schematic from the library view in the main ADS window. And place input/output termination resistors from *Simulation-S_Param* library, which are set to 50 ohm by default. Since the s-parameter block is fully-differential differential, change the termination resistors to 100Ω and connect all building blocks together. Then, in order to set up S-parameter simulation, place the "*S P*" from the same library as shown in Figure 15. You can modify the frequency range and other S-parameter simulation parameters as shown in Figure 16.

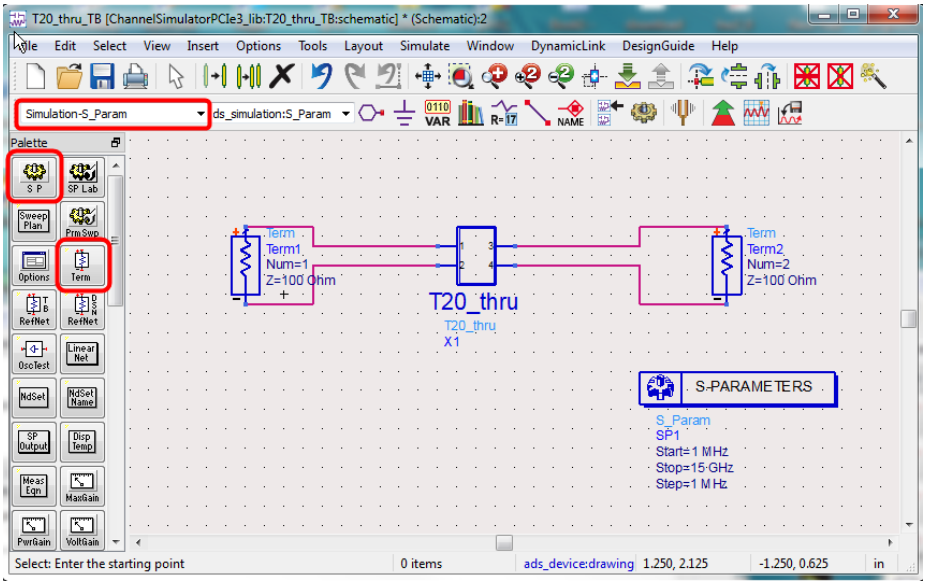


Figure 15 The Test Setup for The T20 Channel S-Parameters Simulation

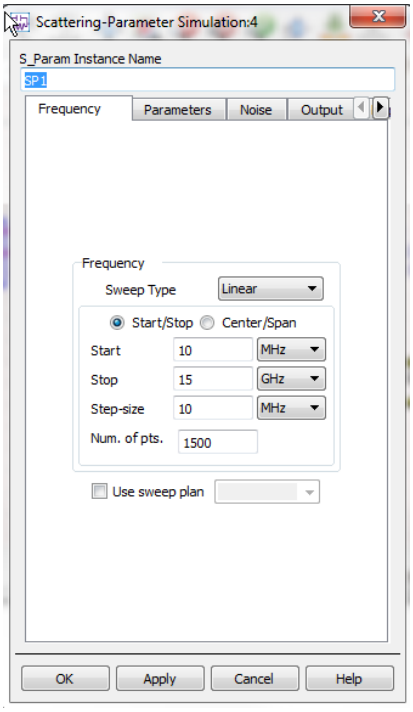


Figure 16 S-Parameter Simulation Setup

When the Data Display window pops up after the initial simulation, select Rectangular Plot from the Palette and add dB(S(2,1)) and dB(S(1,1)) for plotting the insertion loss and return loss, respectively. After completing the simulation setup, run the simulation by selecting *Simulate* -> *Simulate* from the menu or pressing F7.

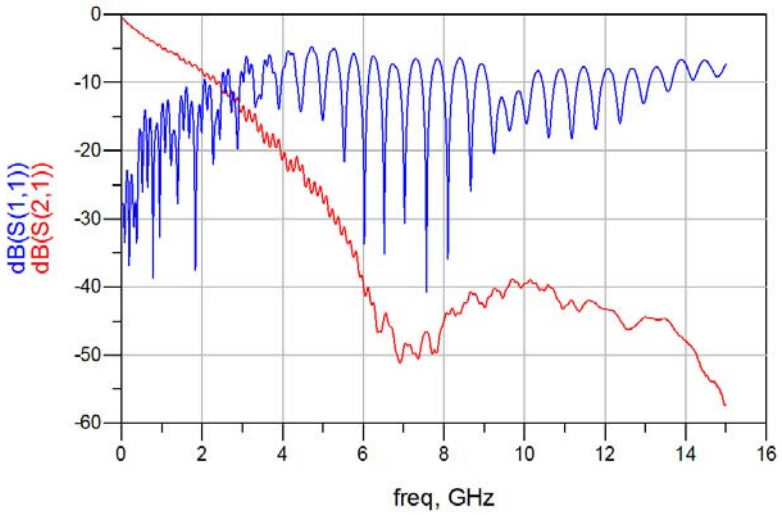


Figure 17 Insertion Loss and Return Loss of The T20 Channel

Observe the Insertion Loss and Return Loss of the channel as shown in Figure 17. Repeat the same process for the FEXT1 and NEXT1 s4p responses for your exercise.

EXAMPLE 2

The second fundamental ADS example for the channel simulation is including practical TX and RX that account for random jitter (RJ). Place the *Diff Tx and Diff Rx* from *Simulation-ChannelSim* library, as shown in Figure 18.

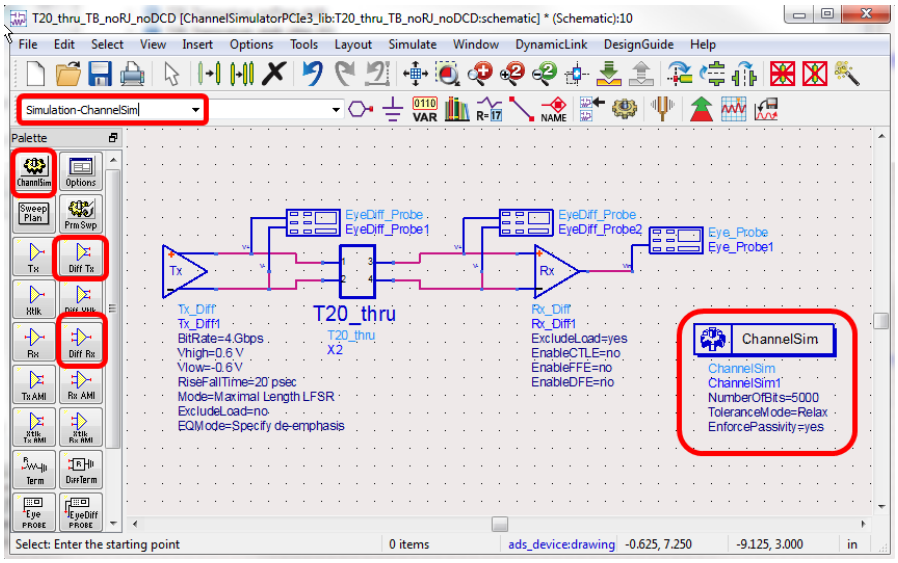


Figure 18 The Schematic Diagram of The Channel Simulation with TX and RX

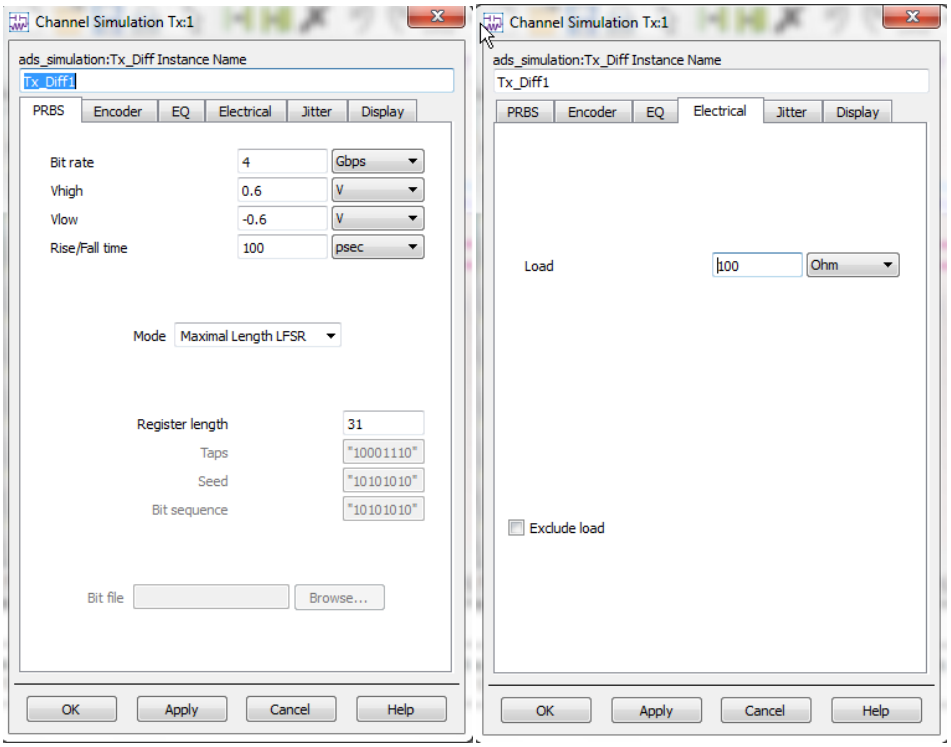


Figure 19 Input PRBS and Load Impedance Setup for Tx_Diff1

Figure 19 and Figure 20 depict the differential TX setup for this example. From the PRBS tab, the data rate, voltage swing, and rise/fall times are defined.

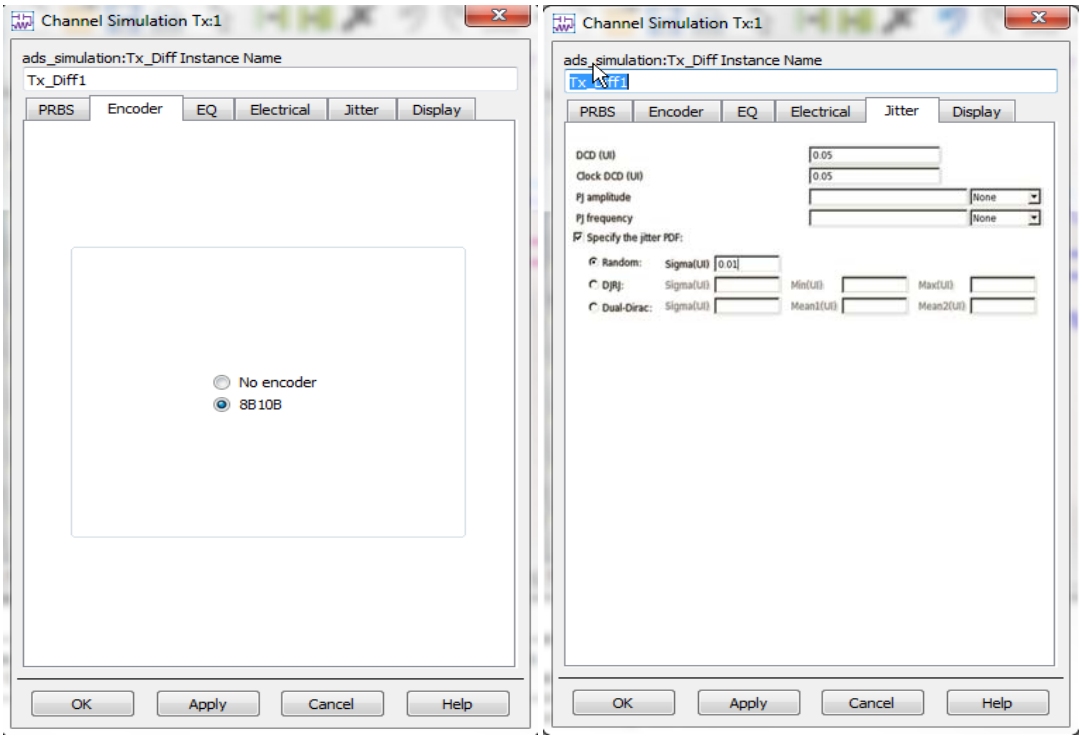


Figure 20 Tx_Diff1 Encoder and Jitter Setup

On the Analysis tab of the dialog box select statistical/bit-by-bit depending on the situation. You may select the “relax” tolerance on the Convolution tab as shown in Figure 21

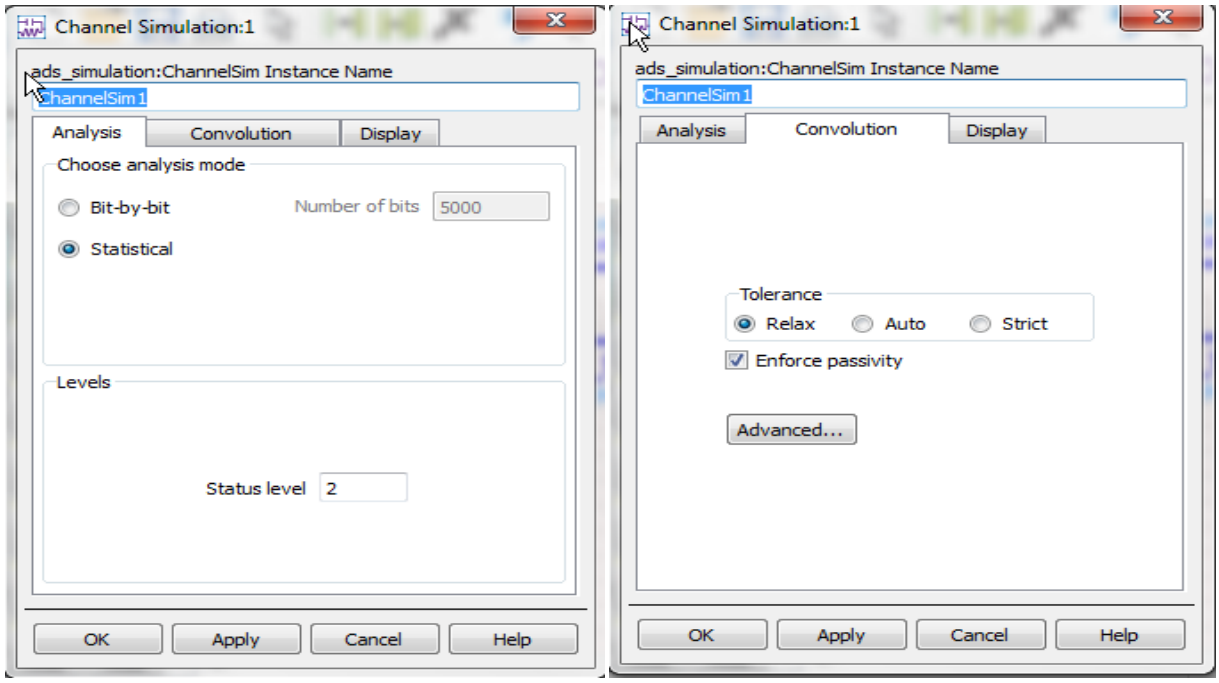
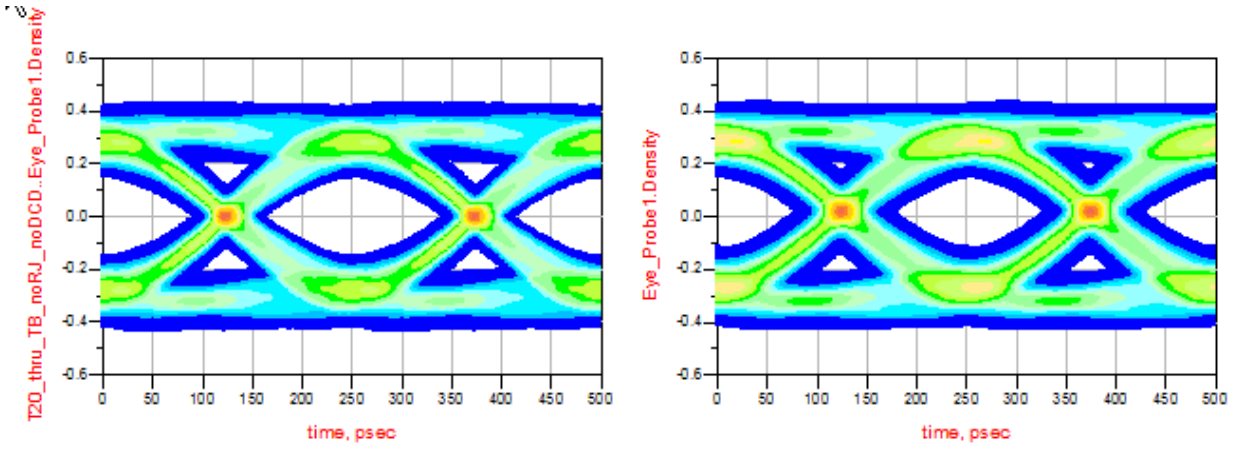


Figure 21 ChannelSim Setup

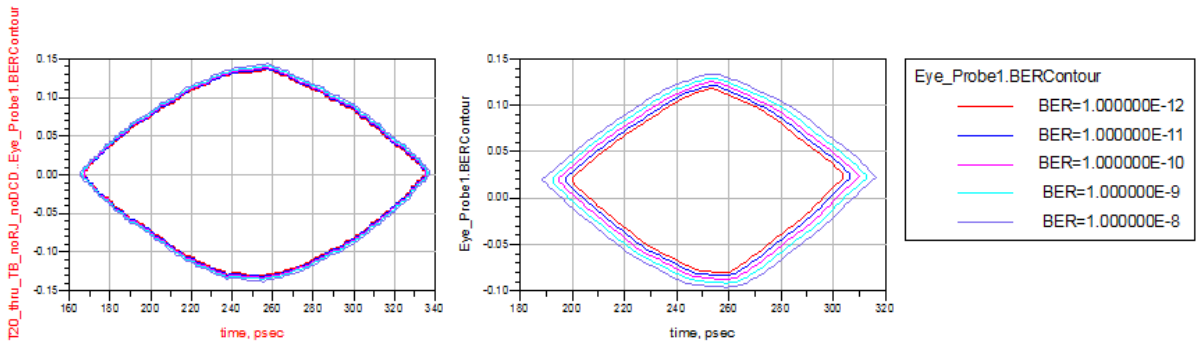
To simulate this circuit, select simulate -> simulate or simply press F7.



(a) (b)

Figure 22 Received Data Eye Diagram after the T20 BP Channel (a) w/o RJ and DCD, and (b) w/ RJ and DCD

As shown in Figure 22, due to the channel ISI, RJ and DCD from TX, reduced amplitude and timing margins are observed at the front-end of the RX. Applying 5% (UI) DCD and 1% (Sigma UI) RJ, cause worse ISI as expected. Figure 23 shows the BER contour at different BER levels defined by the worst case eye. Note, including RJ and DCD is what spreads and shrinks eye height and eye width for various target BER. Time and voltage BER bathtub curves with and without RJ and DCD are shown in Figure 24. Please note that BER contour and time/voltage bathtub measurements may not be enabled by default. In order to include those results you have to add them in Measurements tab in each Eye_Probe block properties.



(a) (b)

Figure 23 BER Contours from the Statistical Simulations (a) w/o RJ and DCD, and (b) w/ RJ and DCD

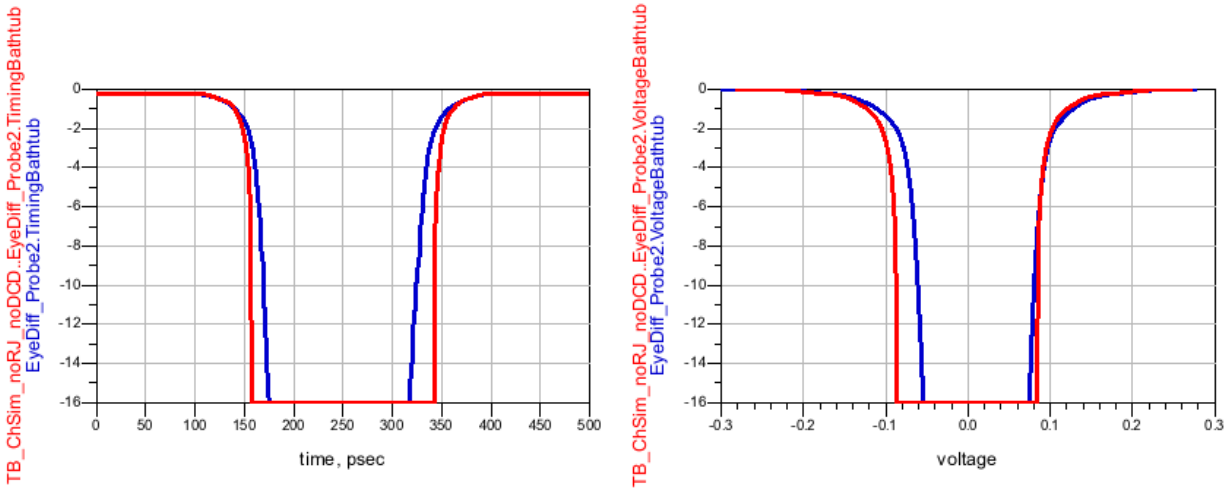


Figure 24 BER Bathtub Curves from ADS Statistical Simulation in (a) Time, and (b) Voltage

Figure 25 illustrates the noise coupling route when a TX channel is placed next to an RX channel. The NEXT generated on the victim flows directly into the receiver of the victim channel. This increases the noise floor of the victim receiver and degrades the victim channel performance.

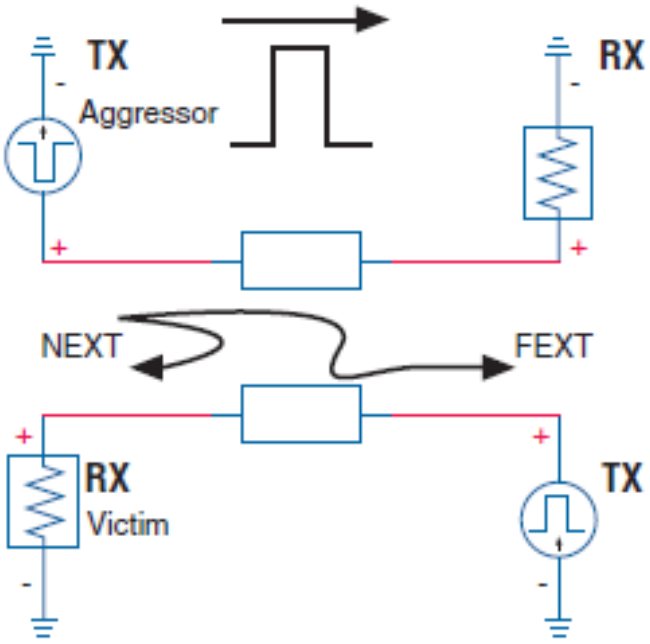


Figure 25 Noise Coupling Route in The Case of RX and TX Channel in Parallel

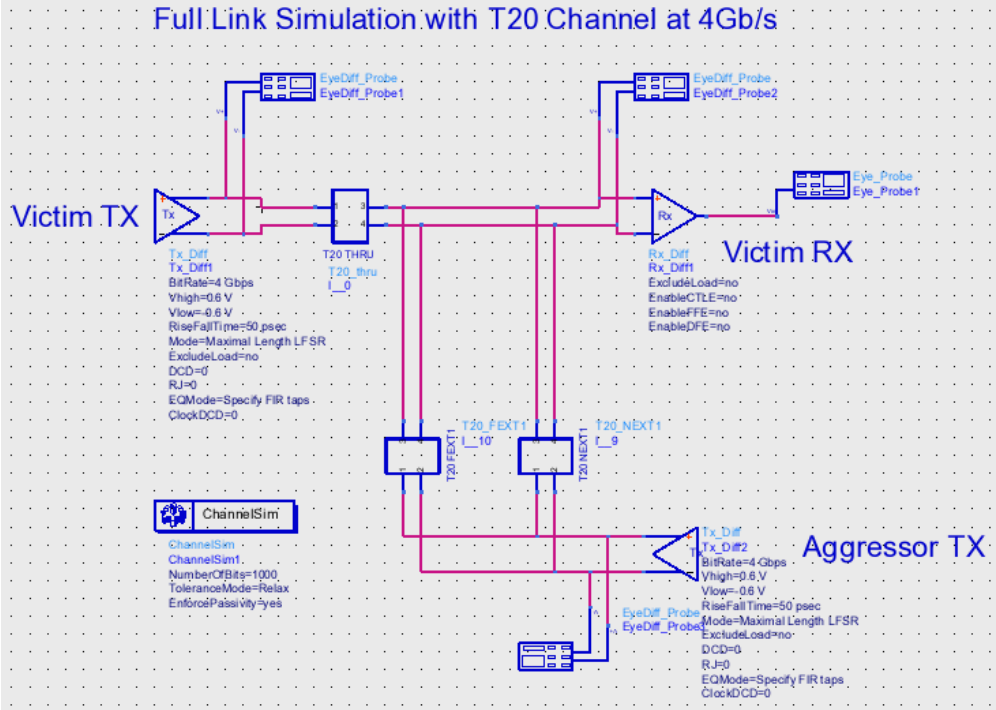


Figure 26 Schematic Diagram of T20 Channel Simulation Including NEXT1 and FEXT1 from Aggressor Channel

Figure 26 shows the schematic diagram of the statistical channel simulation for the T20 BP channel including near-end- and far-end-crosstalk at 4Gb/s data rate. Adding realistic RJ and DCD to the TX and RX and applying TX 2-tap FIR at TX and optimized 5-tap DFE at the RX, Figure 27 shows the eye diagrams measured at the victim RX with NEXT1, FEXT1 and without any crosstalk.

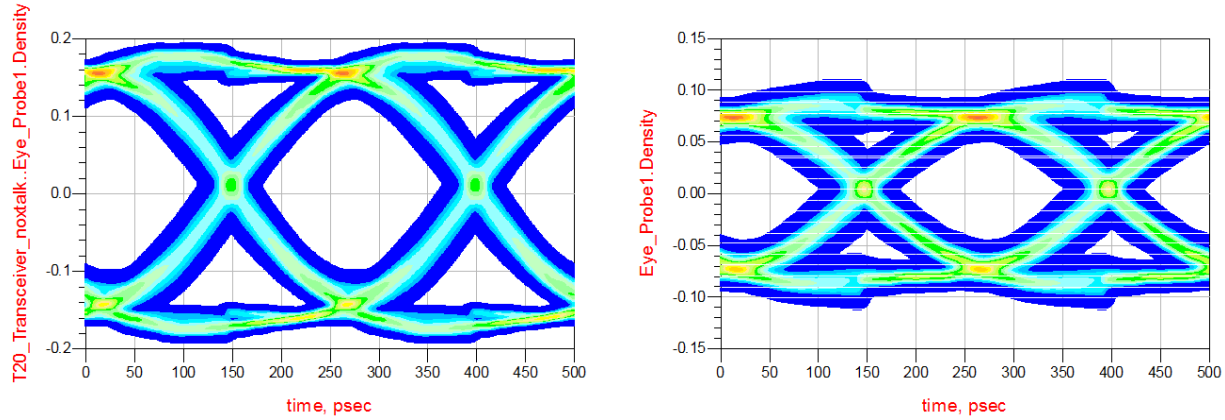


Figure 27 Received Data Eye Diagram after The 20" BP Channel (a) w/o Crosstalk, and (b) w/ NEXT1&FEXT1

Several scenarios for different TX FIR setting, RX CTLE and DFE settings with packaging parasitics are left for your exercise in this lab. Channel frequency response, BER contours, BER bathtub curves, and eye diagrams will be plotted. Optimized TX FIR taps and DFE taps will be used. For more ADS functionalities associated with Signal Integrity Design refer to [2].

Pre-Lab

1. In digital circuit design, there are many switching signals. Finite supply impedance causes switching output noise. Build the circuit shown in Figure 28 with supply inductance and decoupling capacitance. Use Case 1: CLK (i.e. 1010 pattern) and Case 2: 7-bits PRBS as the input sources. CLK frequency is set to be 2.5GHz with 20ps rise/fall time. PRBS date rate is 5Gb/s with 20ps rise/fall time. Please plot the output eye diagrams. Compare the results with the case having ideal supply (zero supply impedance by removing all parasitics).

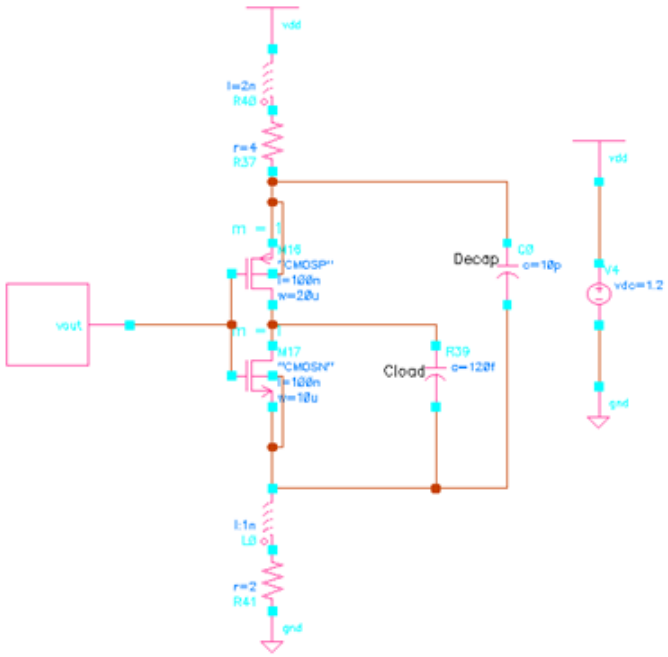


Figure 28 Finite Supply Impedance Simulation

2. Complete the noise and jitter budget tables.

Table 2 Noise Budget (V)

Parameter	Kn	RMS	Value (BER=10^{-12})
Peak Differential Swing			1
RX Offset + Sensitivity			0.005
Power Supply Noise			0.004
Residual ISI	0.03		?
Crosstalk	0.02		?
Random Noise		0.002	?
Attenuation	12dB		?
Total Noise			?
Differential Eye Height Margin			?

Table 3 Jitter Budget (ps)

Component (BER=10^{-12})	**RJ**	**DJ**	**TJ**
TX+PLL	1	12	?
Channel	1.5	25	?
RX+CDR	2	12	?
RSS TJ	?	?	?

Questions

1. Using the ADS, analyze the following test cases. Use 1" Backplane s-parameter (B1). At 8Gb/s, include packaging parasitic as depicted in Figure 5 for chip-to-chip interconnect. Assume 500um Bonding wire with bonding pad capacitance of 200fF, and neglect the mutual wire inductance and pin parasitic for realistic termination modeling. Please, refer to [2] for step-by-step guide on using ADS for Signal Integrity Design. For all test cases use 1Vpp swing at TX.

   (a) Using ADS, plot Insertion Loss and Return Loss from 50MHz to 15GHz. Compare with MATLAB plot.
   (b) Show eye diagrams, and BER contours, and BER bathtub curves both in time and voltage for the following test cases. Include all schematics on the lab report.

   - Case 1: Only the forward channel (thru channel) including TX and RX with ideal 100Ω differential terminations without any cross talk.
   - Case 2: Use the forward channel in Case 1 with an aggressor (FEXT1, NEXT1) terminated with an ideal 100Ω differential load.
   - Case 3: Use the forward channel in Case 1 with realistic terminations (i.e. including parasitics).
   - Case 4: Use the forward channel with an ideally terminated aggressor similar to Case 2 with realistic terminations (i.e. including parasitics).

   (c) Repeat (b) with non-ideal transceiver jitter properties,
   - TX
     - DCD = 0.04UI; Clock DCD = 0.04UI
     - RJ = 0.01UI
     - Load = 100 Ohm
     - De-emphasis = 3dB
   - RX
     - No FFE, No DFE
     - Load = 100 Ohm
     - RJ = 0.01 Sigma
     - Amplitude noise = 1mV

2. Use ADS to model a 5Gb/s link that operates on 20" BP channel (T20_thru) with various equalization schemes including crosstalk aggressors (NEXT1 & FEXT1). Include the same jitter properties and packaging parasitics as Problem 1 for all test cases. You should provide your own CTLE poles and zero(s) in the RX block. Also, include TX FIR taps. For all test cases use 1Vpp swing at TX.

   Show eye diagrams, BER bathtub curves, BER contours in the following cases in Table 3. Plot the eye heights vs. Case # at BER of 10^{-12}.

Table 3 Test Cases

	TX FIR	RX
case 1	1 Pre	2 Taps DFE
case 2	1 Post	1 Taps DFE
case 3	1 Pre	CTLE+1 Taps DFE
case 4	1 Post	CTLE+1 Taps DFE
case 5	1 Pre-1 Post	1 Taps DFE
case 6	1 Pre-1 Post	3 Taps DFE
case 7	1 Pre-1 Post	5 Taps DFE

Note: RX DFE taps can be optimized by checking the "optimized" in the *Rx_Diff* dialog box. Unfortunately, the ADS does not have optimization function for the TX FIR taps. Alternatively, fixed TX FIR taps can be optimized by MATLAB post-processing of the pulse response with zero forcing (ZF) or minimum mean square error (MMSE) algorithms. Refer to the lecture slides dealing with TX FIR equalization and *tx_eq.m* from the course website.

References

[1] *Digital Systems Engineering*, W. Dally and J. Poulton, Cambridge University Press, 1998.

[2] *Quick Start for Signal integrity Design Using Agilent ADS,* Sanjeev Gupta and Colin Warwick, Agilent Technologies.

[3] *Using ADS for Signal Integrity Optimization,* White Paper, Agilent Technologies.

[4] *Advanced Signal Integrity for High-Speed Digital Designs*, S. H. Hall and H. L. Heck, Wiley, 2009.