ECEN 720 High-Speed Links: Circuits and Systems

Lab3 – Transmitter Circuits

Objective

To learn fundamentals of transmitter and receiver circuits.

Introduction

Transmitters are used to pass data stream through transmission lines in either current or voltage mode. In high data rate applications, the output impedance of transmitters should match the transmission lines' characteristic impedance and should be tunable in order to compensate the process, voltage, and temperature variations. The multiplexing technique can be used to extend transmitters signaling bandwidth.

Transmitter Automatic Termination Adjustment

On-chip termination resistance suffers from process, voltage, and temperature variations. It is very difficult to obtain an accurate termination resistance value. Therefore, in high performance link designs, automatic termination adjustment is often implemented. Figure 1 shows an example of automatic termination adjustment. PMOS transistors are the on-chip terminator replica (slave). In practical chip design, the replica is located near the main PMOS termination resistor (master) in order to reduce device mismatch. External reference resistor is equal to the characteristic impedance of the transmission line. Both reference resistor and PMOS termination resistors are connected to one reference voltage (VDD in this case) and two identical current sources. A clocked comparator is used to measure the voltage difference across the resistors. An up/down signal is produced and drives the counter to tune the PMOS termination resistors. Since the tuning circuit can run at very low frequency, power consumption is not significant. A window reference can be created in order to eliminate the "dither" effect.

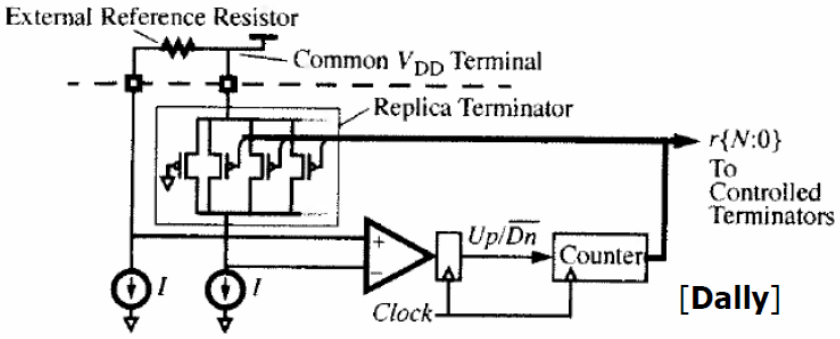

Figure 1 Termination Adjustment Servo Loop

Voltage Mode Driver

Voltage-mode driver acts as a switch selectively connecting to a transmission line as shown in Figure 2(a). Since matching output impedance is required, the switch should have output impedance equal to the characteristic impedance of the transmission line. In high voltage swing application as shown in Figure 2(b), the size of the transistors, especially PMOS, must be made very large so that transistors can have an on resistance of about Z_0. In small voltage swing application, both transistors can be NMOS with the upper transistor connecting to a reference voltage as shown in Figure 2(c). The use of PMOS can be avoided. Figure 3 shows the differential voltage-mode driver schematics.

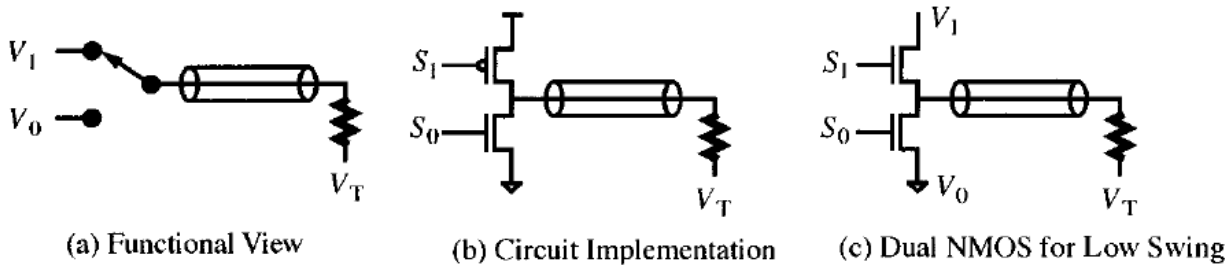

Figure 2 Voltage Mode Driver

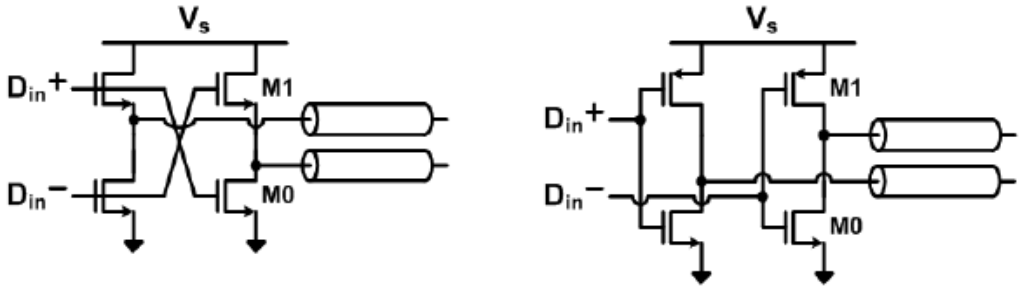

Figure 3 Differential Voltage-Mode Driver (a) Low Swing (b) High Swing

Low-Swing Voltage-Mode Driver Impedance Control

Low-swing voltage-mode driver impedance control can be implemented as shown in Figure 4. Vr Regulator produces a regulated supply voltage for the pre-driver. The regulated Vr is produced in a feedback loop, based on the impedance matching between M1+R/2+M2 and R. The output swing of the pre-driver is set by Vr, which also controls the voltage-mode driver's output impedance. The voltage-mode driver's output swing is regulated by Vs Regulator. The sizes of M1 and M2 are the duplicates of the voltage-mode driver transistors. This design also inherently cancels resistance process variation.

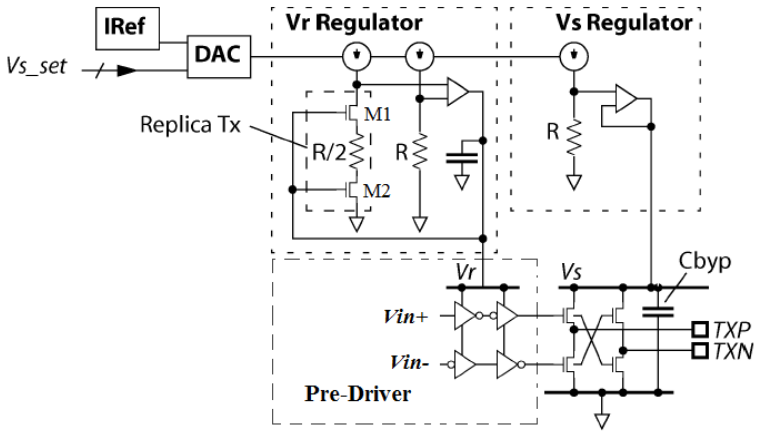

Figure 4 Low-Swing Voltage-Mode Driver [3]

Current-Mode Driver

Current-mode drivers are used in most high performance serial links and use Norton-equivalent parallel termination. Figure 5 shows the push-pull current-mode driver which is used in low-voltage differential signaling (LVDS). Since the current commutes between the differential input pair, low dI/dt noise can be achieved. Duel current sources could be a problem in low-voltage technology application.

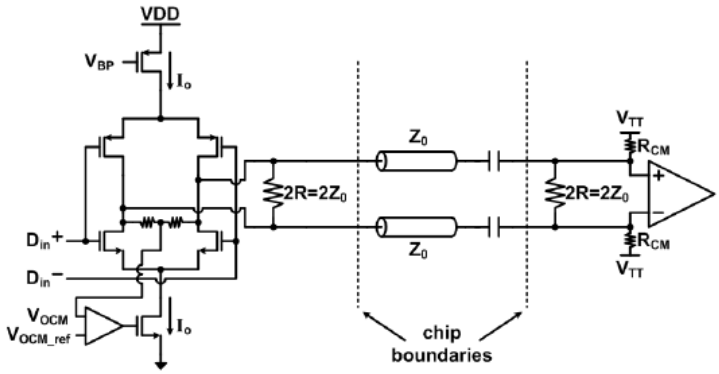

Figure 5 Push-Pull Current-Mode Driver

Figure 6 shows the current-mode logic (CML) driver. It requires lower supply voltage for operation compared to LVDS. CML structure is usually preferred in the newer technologies designs.

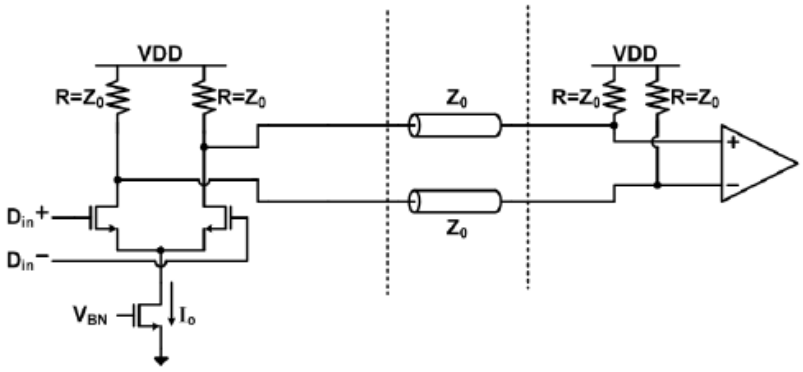

Figure 6 Current-Mode Logic (CML) Driver

Output Driver Rise-Time

The rise time of an output driver must be carefully chosen to avoid excessive ISI. A very fast edge rate may result in reflections from any impedance discontinuities. Unlike TDR's spatial resolution requirement, in output driver design, being very sensitive to small impedance discontinuities is not desired. On the other hand, a long rise time will reduce timing budget, which could cause ISI. Figure 7 shows a method of rise-time control used in current-mode driver. The driver is divided into four current-mode drivers, each with one-quarter of the peak current. The delay elements are used so that the drivers can be turned on sequentially. In order to avoid the stair-step output wave form, the individual current drivers are designed to turn on with a linear ramp.

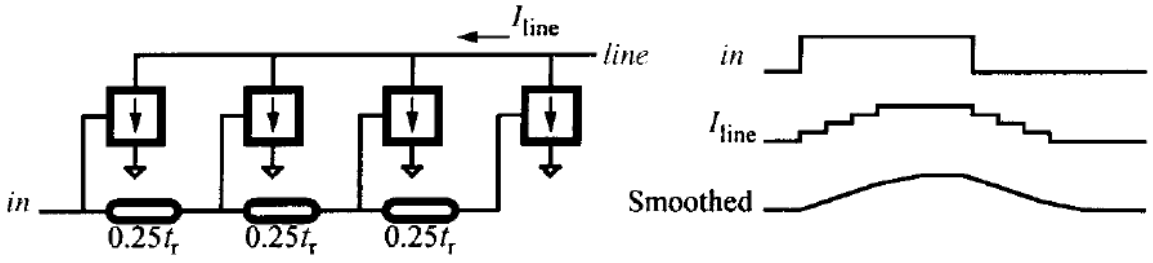

Figure 7 Rise-Time Control with a Segmented Current-Mode Driver [Dally]

Pre-Lab

1. CMOS Technology Characterization.

In order to estimate what level of performance is achievable with a given process technology, it is useful to run some initial characterization simulations.

For both NMOS and PMOS transistors with dimensions W=1μm and L=L_{min}, **plot the transition frequency (f_T) versus $|V_{GS}|$ and also versus I_{DS} – 4 plots total (2 per transistor)**. Use the test circuits in

a. Figure 8. The easiest way to do this is to run a DC sweep with $|V_{GS}|$ varying from 0 to VDD and plot the following equation.

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (1)$$

Where C_{gg} is the total gate capacitance. Comment on the results. For the f_T plot versus $|V_{GS}|$, use a linear scale for both axes. For the f_T plot versus $|I_{DS}|$, use a log scale for the x-axis (current) and a linear scale for the y-axis (frequency). Discuss how this characterization data impacts the design of high-speed circuits.

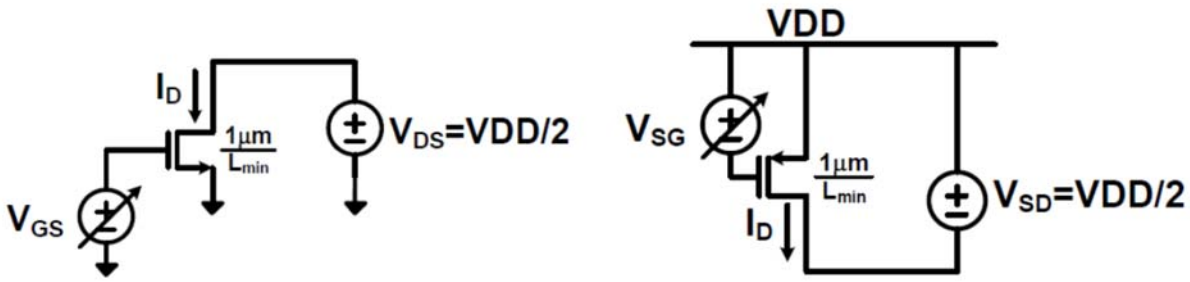

Figure 8 (a) NMOS f_T Test Circuit (b) PMOS f_T Test Circuit

b. **Find the FO4 inverter delay**. The bit-rate of transmitters is often limited by the bandwidth of clock buffering. For minimum propagation delay to drive a given capacitive load, a fan-out of four inverter buffer chain (FO4 inverter delay) is often used [5]. Refer to the instructions on how to use the default 90nm CMOS technology models for more details on how to setup the test circuit. For the inverters use minimum channel length and an NMOS unit finger width of 1μm. Size the PMOS/NMOS ratio of the inverter for equal rise and fall delays, measured from 50% of the input to 50% of the output. However, don't exceed a PMOS/NMOS ratio of 3, i.e., if the simulations show that a ratio greater than 3 is required for equal delay then just use 3 and accept the slight delay difference.

   i. Specify the process technology that you use.
   ii. Sweep the supply voltage (VDD) from 0.7V to 1.2V with 50mV step size in order to include FO4 delay [ps] vs. VDD [V].
   iii. For the design of half-rate TX architecture, find optimal VDD for maximizing power efficiency at 5Gb/s data rate.

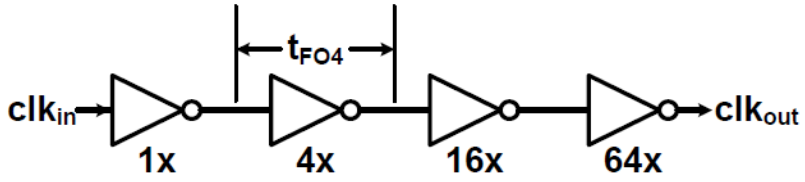

Figure 9 FO4 Delay Test Circuit

Questions

1. Transmitters can operate in voltage-mode or current-mode with single-ended termination or differential termination as shown in Figure 10. Please calculate the power consumption for (a) current-mode with single-ended, (b) current-mode with differential, (c) voltage-mode with single-ended, and (d) voltage-mode with differential termination, assuming V_d is the output swing and termination is 50Ω.

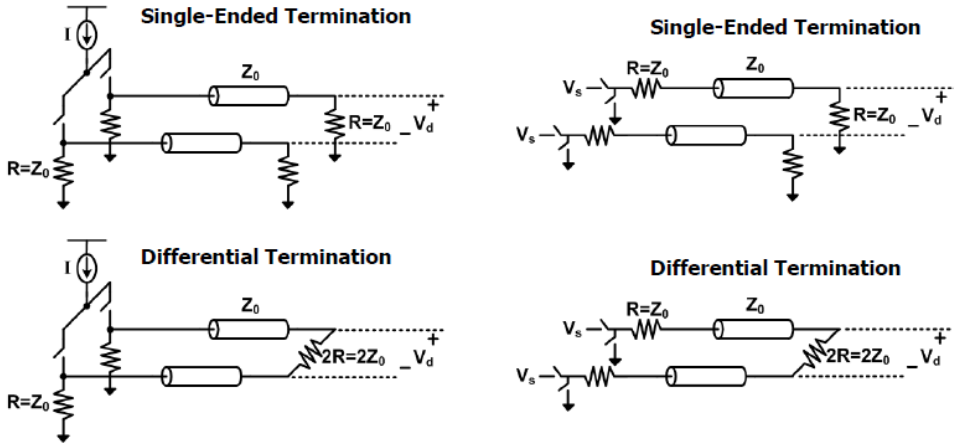

Figure 10 Current Mode and Voltage Mode Transmitters

2. A multiplexer (MUX) is often used to serialize parallel low speed data into one single stream of high speed data. It can be implemented before the transmitter output driver stage. Design a 4:1 MUX that serializes 4 parallel 2.5Gb/s data into a 10Gb/s bit-stream. Figure 11 is an example of 2:1 MUX with re-timer (please refer to [4] as a reference).

   a. Use behavioral models for D-flip flops and latches. The AB select can be implemented using a transmission gate 2:1 MUX. Design the AB selector in transistor level.
   b. Verify the MUX operation and show your schematic and simulation results.

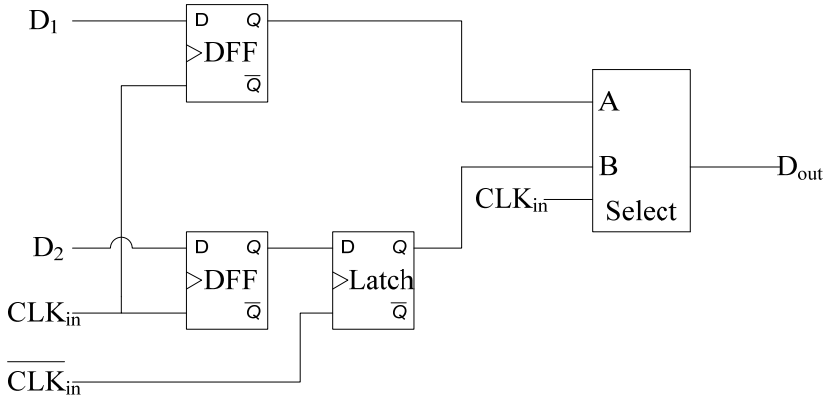

Figure 11 2:1 Data MUX [4]

3. 10Gb/s Low-Swing Driver and Termination Design.

a. Design both a differential current-mode CML driver and a differential low-swing voltage-mode driver to support an output swing of 300mVppd. For the Low-Swing Voltage-Mode Driver, please refer to [2] [3].
   i. For the CML driver, the output tail current source should be implemented at the transistor level, but you may use a current mirror that has an ideal current source to produce the bias for the output stage tail current source.
   ii. For the voltage-mode driver, design the regulator and driver circuit. If op-amps are needed, feel free to use behavioral op-amp models.

b. Include one pre-driver stage (in transistor level) before the driver output stage. This may be a simple inverter pre-driver or something more complex if you want.

c. The driver should be terminated on-chip both at the transmitter and the receiver as shown in Figure 12. The termination should be designed to handle a temperature variation from 0 to 100°C **OR a variation of ±30% from the nominal 27°C value if the temperature variation simulation doesn't work**. Passive termination may be used, however a realistic model including parasitic capacitance must be used, i.e., from a design kit or taken from the table in lecture 5. Choose whichever termination scheme you think is most appropriate (AC vs DC-coupled, single-ended vs differential) and briefly explain your choice.

d. Since the emphasis of this problem is the driver design, in your simulations use a simple channel consisting of TX output cap = RX input cap = 100fF and an ideal 50Ω, 1ns transmission line.

e. **Turn-in the following for your design**
   i. Schematics with details of transistor sizing.
   ii. A 10Gb/s eye diagram at the RX. Use a pseudo-random input sequence of 2^7-1 or higher to produce the eye diagram.
   iii. Plot the return loss versus frequency looking back into the transmitter at 0, 27, and 100°C. For this, program the termination to yield the best performance at each temperature. **Note: if your temperature variation simulations don't work, then just turn in one plot at 27°C and data showing that your termination can tune ±30%[1].**
   iv. Compare the power consumption of the two drivers. Break down the power into pre-driver and output stage power.

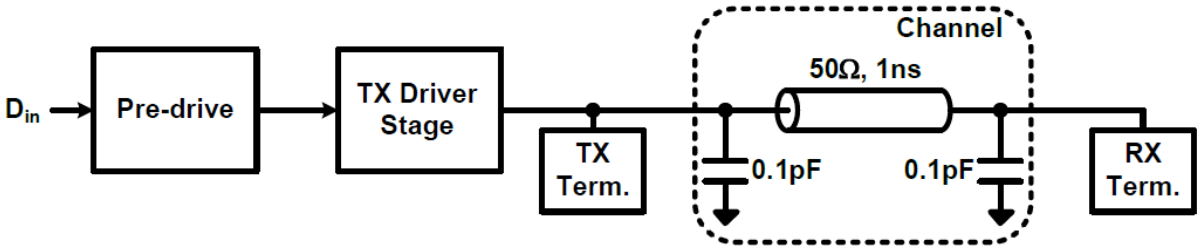

Figure 12 Schematic of the Link Circuit

[1] Note: ±15% is probably sufficient for only temperature variations. To handle process, voltage, and temperature variations, you would probably need to increase this range to ±30%.

References

[1] *Digital Systems Engineering*, W. Dally and J. Poulton, Cambridge University Press, 1998.

[2] K.-L. J. Wong, H. Hatamkhani, M. Mansuri, and C.-K. K. Yang, "A 27-mW 3.6-Gb/s I/O transceiver," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 602-612, Apr. 2004.

[3] J. Poulton, R. Palmer, A. M. Fuller, T. Greer, J. Eyles, W. J. Dally, and M. Horowitz, "A 14mV 6.25-Gb/s transceiver in 90nm CMOS," IEEE J. Solid-State Circuits, vol. 42, no. 12, pp. 2745-2757, Dec. 2007.

[4] J. Cao, M. Green, A. Momtaz, K. Vakilian, D. Chung, K.-C. Jen, M. Caresosa, X. Wang, W.-G. Tan, Y. Cai, I. Fujimori, and A. Hairapetian, "OC-192 transmitter and receiver in standard 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1768–1780, Dec. 2002.

[5] Chih-Kong Ken Yang, Ph.D Dissertation, Stanford University, 1998