November 2, 2023

ECEN-620: Broadband Circuit Design

Course Projects

Project teams can consist of 1-3 students.
Preliminary report: Due on November 16, 2023
Final report: Due on December 4, 2023
Power Point presentation: December 12, 2023 1:00PM-3:00PM

For all projects discussed below, you may use behavioral models for some parts, but critical components (discussed with the professor) must be simulated at transistor level. As a graduate student, you must be able to explain very well the main issues in your project, and what the contributions are.

Suggestions:

Project #1: Design of a 3.2GHz Frequency Synthesizer for Wireless Communications with spurs under -70 dBc

The main specs are:
Frequency step = 8 MHz
VCO continuous tuning range > 5%
Phase noise < -110 dBc at 1 MHz offset
Note: An advanced PLL architecture (advanced PFD/CP interface, loop filter, frac-N synthesizer with $\Sigma-\Delta$ modulation, etc…) must be used to achieve the target spur performance. Just designing an optimized charge pump will most likely not meet the spur specification.

Project #2: Frequency Synthesizer for DTV with channels spread in a 800MHz bandwidth.

The main specs are:
Frequency step = 6 MHz
Frequency range of operation ={50MHz-850 MHz}
Phase noise < -120 dBc at 3 MHz offset

Project #3: High-Performance Quadrature Clock Generator

Frequency = 1 GHz
Quadrature outputs with phase error less than 1°
Jitter < 1 ps_{rms}
Spurs under -50 dBc
Minimize power consumption
Load impedance = 2.5 pF

Project #4: 10Gb/s Clock Generator Data Recovery System

Your choice of sampling clock frequency (1.25GHz – 10GHz)
Compliant with OC-192 mask
Minimize power consumption

Project #5: 10Gb/s Limiting Amplifier

Small-Signal Gain ≥ 50dB
Small-Signal Bandwidth ≥ 10GHz
Integrated Input Referred Noise ≤ 0.5mV_{rms}
Include offset correction
Minimize power
Show eye diagrams before and after limiting amplifier

Project #6: Low-Jitter Wideband 5-10GHz PLL

This project involves the design of a low-jitter wideband PLL. The main specs are:
Output Frequency Range = 5 - 10GHz (All frequencies)
Fixed N=16 loop division factor with a scalable reference clock (312.5 – 625MHz)
Loop Bandwidth between 4 - 5MHz
Output Jitter < 100fsrms integrated over a 10kHz – 10MHz bandwidth

Project #7: 20Gb/s Current-Mode Wireline Serializing Transmitter

This project involves the design of a 20Gb/s differential current-mode wireline transmitter. The transmitter should serialize 20 bits of parallel 1.25Gb/s data up to the full 20Gb/s. The output driver should provide $1V_{ppd}$ swing on a controlled impedance (100Ω differential) channel. On-die termination should also be utilized that is programmable to account for process and temperature variations.

Project #8: Any other suggestion is more than welcome.

Preliminary Report Required Sections

1. Motivation and Project Overview
2. Literature Survey
3. Proposed Architecture
    a. This can change for the final report
4. Initial Simulation Results
5. Plan of Work
    a. A description of what will be completed for the final report

Final Report Required Sections

1. Motivation and Project Overview
2. Literature Survey
3. Architecture
4. Simulation Results
    a. This section must include a Table comparing your design with current references
5. Conclusion

The Project Presentation should include the same sections as the final report.