A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors

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***Abstract*—A microprocessor clock generator based upon an analog phase-locked loop (PLL) is described for deskewing the internal logic control clock to an external system clock. This PLL is fully integrated onto a 1.2-million-transistor microprocessor in 0.8-μm CMOS technology without the need for external components. It operates with a lock range from 5 up to 110 MHz. The clock skew is less than 0.1 ns, with a peak-to-peak jitter of less than 0.3 ns for a 50-MHz system clock frequency.**

I. Introduction

A FULLY integrated phase-locked loop (PLL) has been designed for application and integration on high-clock-frequency microprocessors. The motivation for doing this comes from three areas.

First, as microprocessors increase clock frequency to 50 MHz and higher, it is necessary to eliminate the delay between external and internal clock (clock skew) caused by the on-chip clock driver delay (Fig. 1(a)). As the microprocessor increases in size to 1 million transistors and beyond, the capacitive load from the logic circuits on the clock driver (Fig. 1(b)) has grown to values of several nanofarads. Therefore, the delay through the clock driver can be 2 ns or more. This delay causes large setup and hold times for the input/output signals and is a limitation on the design of systems at high clock frequencies. An on-chip PLL can eliminate this clock skew.

Also, many microprocessors use logic that requires a precise 50% duty cycle clock. To generate this clock, a clock source at twice the logic operating frequency is needed. Instead of generating this high-frequency signal on the system board and bringing it into the chip, an on-chip PLL can synthesize this multiple of the external clock.

Finally, clocking a microprocessor internally faster than the external bus is an option that is attractive for system integration. A clock generator based upon a PLL can synthesize the internal clocking frequency to be greater than the external frequency, for example, twice the external frequency.

However, integrating a PLL on a microprocessor chip is difficult because of noise. This involves integrating an analog circuit (that is required to generate precision timing) on a die that has a large amount of generated digital noise.

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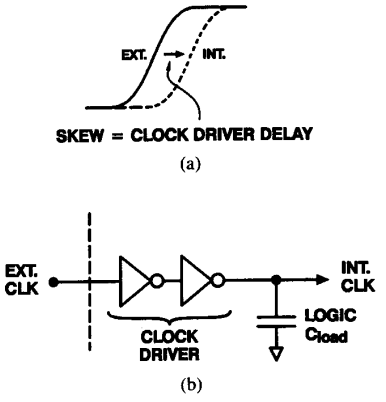


Fig. 1. Clock skew definition.

This paper describes a PLL-based deskewed clock generator that has been fully integrated on a microprocessor [1], i.e., no external components are used. This PLL circuit has a wide range of frequency of lock, from 5 to 110 MHz, and minimum sensitivity to process, supply, and temperature changes. This paper also describes what was done to reject the digital noise to achieve a skew of less than 0.1 ns with peak-to-peak jitter of 0.3 ns.

II. The Phase-Locked-Loop Clock Generator

A block diagram of the deskewed clock generator is shown in Fig. 2. The external clock goes through an input buffer to the phase-frequency detector (PFD). The feedback of internal clock is compared to the external clock for phase and frequency error. The input offset phase error of the PFD determines the skew between internal and external clock.

The PFD generates UP/DOWN pulsed signals to the charge pump which is followed by a loop filter. The loop filter stabilizes the PLL even with component variation due to the manufacturing process. The output of the loop filter is a control voltage for the voltage-controlled oscillator (VCO). The VCO is followed by a divide-by-2 circuit that generates an accurate 50% duty cycle clock waveform for the microprocessor. The VCO output frequency is, therefore, operating at twice the microprocessor clock

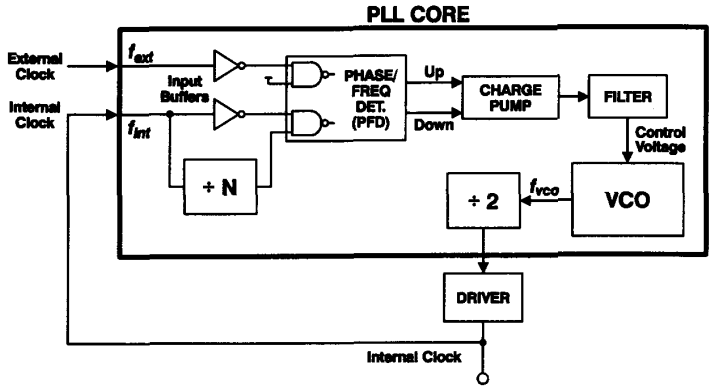


Fig. 2. Functional block diagram.

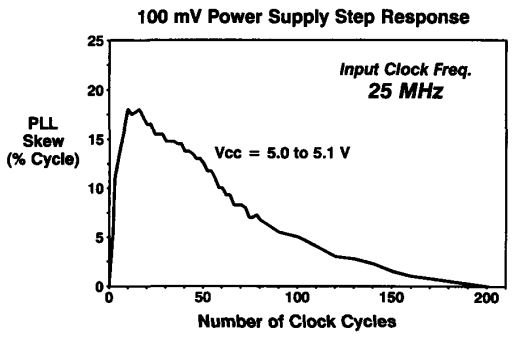


Fig. 3. Conventional PLL clock generator.

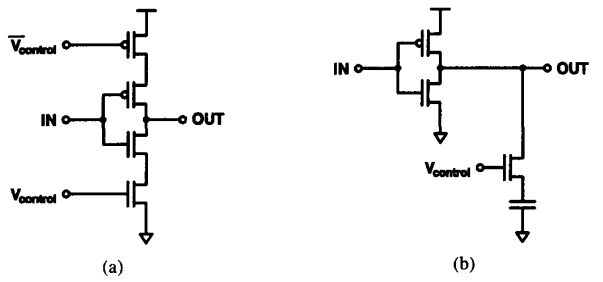


Fig. 4. Conventional delay elements. (a) Current-starved inverter. (b) Variable C_{load}.

frequency. The driver circuit buffers the clock signal to drive the logic of the microprocessor.

The divide-by-N circuit allows the feedback internal clock to be N times the external clock. For example, $N = 2$ makes the internal clock twice the external clock frequency. The divide-by-N circuit creates a signal that enables only one out of N feedback internal clock pulses to propagate into the PFD. This circuit, since it simply masks out clock cycles, does not introduce any additional delay in the feedback clock. The largest value for N is a function of the minimum stable operating input frequency for the PLL, and the maximum VCO output frequency.

Since the PLL is on the same chip as the microprocessor, it is difficult to isolate the PLL from the digital noise generated by the core logic and output buffers. The performance of a conventional PLL clock generator when it experiences a 100-mV step voltage on the power supply is shown in Fig. 3. This figure shows the skew between internal and external clock over time measured in clock cycles after the step voltage. The measurement shows that the skew or phase error accumulates to as much as 18% of the clock cycle (65°) before the PLL has time to correct this error through the feedback. Clearly this is unacceptable since at least 100 mV of power supply noise is very likely to occur in a microprocessor. Over an order of magnitude improvement in the power supply noise rejection of this conventional PLL clock generator is needed to achieve the acceptable level of less than 2% of cycle (0.72°). Fig. 4 shows some commonly found delay elements used in conventional ring-oscillator-based VCO designs used for PLL's. These show the high sensitivity to power supply noise of Fig. 3.

III. PLL Components

A. Phase-Frequency Detector

The conventional sequential frequency and phase detecting logic circuit is used as shown in Fig. 5. This circuit has a monotonic phase error transfer characteristic over the range of input phase error up to ± 1 cycle (360°). It also is insensitive to duty cycle. This circuit can operate up to very high frequency (approximately 400 MHz in this process), since the critical path is limited by just three gate delays: two from the cross-coupled, two-input NAND's, and one from the four-input RESET NAND.

B. The Charge Pump

The charge pump which is based on one described in [3] is shown in Fig. 6. The UP and DOWN signals switch current sources I_{up} and I_{dn} onto node $V_{control}$, thus delivering a charge to move $V_{control}$ UP or DOWN. I_{up} and I_{down} need to be equal. When nodes $N1$ and $N2$ are not switched to $V_{control}$ they are biased by the unity-gain amplifier. This suppresses any charge sharing from the parasitic capacitance on $N1$ or $N2$ that can cause mismatch between the UP and DOWN current sources.

The PFD and charge-pump circuits provide a transfer function of input phase error to output charge per clock

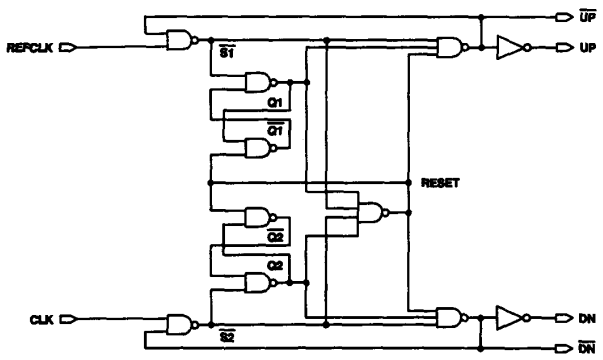


Fig. 5. Phase-frequency detector.

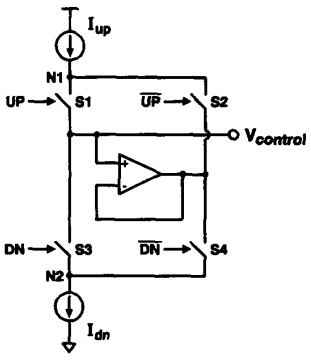


Fig. 6. Charge pump.

cycle. This transfer characteristic must be controlled over supply, temperature, and process variations since it determines the clock skew.

C. The Loop Filter

The loop filter shown in Fig. 7 consists of two capacitors made with MOSFET gate oxide and one resistor made with the n-well implant. For low-jitter PLL design, the frequency jumps inherent to simple *RC* low-pass filter compensation are a concern [5]. By adding capacitor C_3 in parallel to the series *RC* impedance, we form a second-order filter with impedance of

$$Z(s) = \left(\frac{b-1}{b}\right)\frac{(s\tau_2 + 1)}{sC_1\left(\frac{s\tau_2}{b} - + 1\right)} \tag{1}$$

where $b = 1 + C_1/C_3$ and $\tau_2 = R_2 C_1$.

This filter realizes two poles and one zero, which makes the PLL a third-order system with a continuous-time transfer function of

$$H(s) = \frac{K\left(\frac{b-1}{b}\right)\left(s + \frac{1}{\tau_2}\right)}{\frac{s^3\tau_2}{b_2} + s^2 + K\left(\frac{b-1}{b}\right)s + \frac{K(b-1)}{b\tau_2}} \tag{2}$$

where K is the open-loop gain of the PLL.

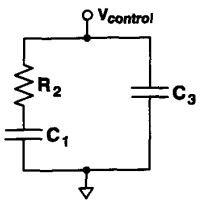


Fig. 7. Loop filter.

Stability of the system is maintained even with the process variation of these on-chip components, which is approximately $\pm 10\%$ for both the capacitance and resistance. While the large-size capacitor C_1 was around 200 pF, this was not a limitation on die size since the total area occupied by this PLL was 0.4% of the total microprocessor die area.

IV. Voltage-Controlled Oscillator (VCO) Issues

A. Power Supply Coupling

Fig. 8 shows what the power supply noise looks like if displayed on a time scale of many clock cycles. The noise consists of high-frequency noise at the clock frequency or higher. This noise comes from cycle-to-cycle switching of large-capacitance nodes within the chip, i.e,. nodes switching every cycle. There is a second component of noise, this one with a lower repetition rate that occurs at over an order of magnitude lower frequency. However, this noise changes the power supply voltage from one cycle to the next in a step-like manner. The cause of this noise is the variation of the circuit activity within the microprocessor. This is a function of the software program that is running. The processor can have intervals when there is heavy circuit activity in switching large amounts of capacitance within the chip, and intervals when there is very little circuit activity. This noise appears as steps or impulses on the power supply of the PLL. If the rejection of the noise coupling into the PLL is not high, then the PLL clock skew (phase error) will display a transient impulse response in Fig. 8(b). The time constant of the settling response is determined by the loop gain of the PLL and can be on the order of microseconds. Note that the actual peak-to-peak jitter in this case becomes dominated by the peaks in the impulse transient noise response, instead of the high-frequency cycle-to-cycle dithering jitter. The jitter would be determined by the latter if there was no supply variation due to the processor activity.

Power supply noise can directly change the VCO output frequency and phase. This is a function of the VCO's stability with changes in the supply (the power supply rejection). Fig. 9 shows how power supply sensitivity of the VCO couples noise into the PLL closed-loop system. Sensitivity of the VCO to power supply changes will cause a direct change in the VCO output frequency, represented as an error frequency f_n away from the VCO operating frequency f_{vco}. Note that the VCO has the transfer function $1/s$, hence the frequency noise source has to be added

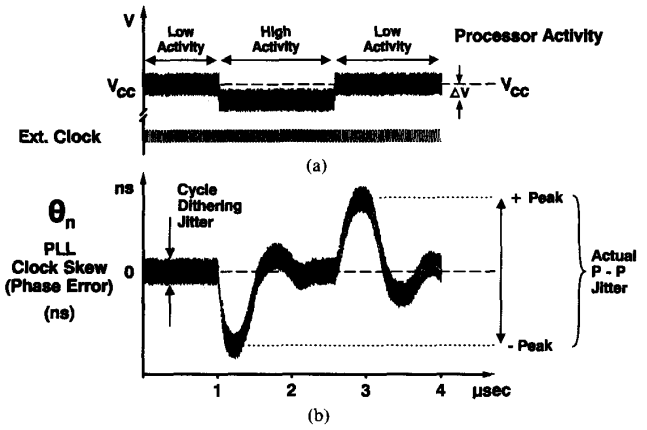


Fig. 8. Power supply coupling.

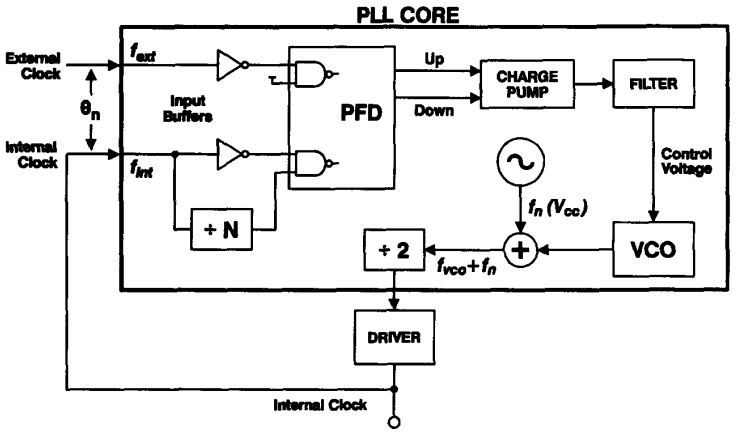


Fig. 9. Power supply noise coupling.

at the output of the VCO and not its input. Since the VCO output frequency divided by 2 is the processor core operating frequency, the processor has to operate at the frequency $[f_{vco} + f_n]/2$.

At the input to the PFD circuit, this internal clock frequency signal is compared to the external clock frequency for phase error. Initially, on the first cycle after the noise step in the power supply voltage, this frequency error causes a phase error (delta) = $[f_n/f_{vco}] \cdot 360°$ of cycle. Since the PLL system has a long time constant compared to the clock period, it takes a number of clock cycles before the feedback can adjust the control voltage to correct the VCO output frequency and phase error. This accumulation of phase error by the PLL over a number of cycles before the maximum phase error occurs makes it a requirement that the initial frequency error f_n, due to the VCO sensitivity to power supply voltage, must be minimized. Therefore, if the power supply rejection of the VCO circuit is not high enough, it can be the dominant source of PLL jitter.

Note also that without any external filtering of the VCC onto the chip, noise on the VCC coming from the motherboard also influences the PLL jitter.

B. VCO Frequency versus Control Voltage Characteristic

When choosing a VCO circuit approach it is important to consider the control voltage versus frequency (V–f) characteristic. A linear characteristic will minimize the VCO sensitivity (i.e., characteristic slope) variation as a function of control voltage or operating frequency, providing PLL stability over the widest possible frequency range.

Also, it is desirable for the V–f characteristic to have a positive slope as shown in Fig. 10. This means that the maximum operating frequency is achieved at maximum control voltage, which is only limited by the maximum VCC applied. If the slope is negative then the VCO minimum frequency is limited by the maximum VCC, i.e., the minimum frequency actually is increased as the applied VCC is reduced. A VCO implemented with the delay element in Fig. 4(b) has this undesirable negative slope V–f characteristic.

The VCO circuit used in this PLL has a linear, positive slope V–f characteristic. This VCO uses a current-controlled differential delay element and is described in the next section.

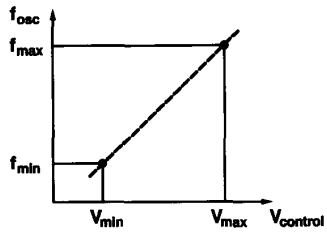


Fig. 10. Oscillator frequency versus control voltage.

V. VCO Circuit Design

A. Current-Controlled Differential Delay Element

The VCO is based on a five-stage ring oscillator where each stage is a current-controlled differential delay cell as shown in Fig. 11.

The delay cell is based on a P-MOSFET source-coupled pair with voltage-controlled resistor (VCR) load elements. The n-well containing the P-MOSFET devices is biased at a voltage referenced to V_{SS}. This eliminates noise coupling from the power supply to the signal nodes. The use of P-MOSFET devices makes the signals referenced to V_{SS}, eliminating frequency shifts due to nonlinear capacitances. Tail current sources are cascoded for high impedance to V_{CC}.

Delay through this cell is a function of the tail current I_{source}, the differential voltage swing, and the capacitance at OUT and OUT#. By controlling signal R_{control} to the VCR load, the voltage swing is held constant and independent of supply voltage. If the capacitance is constant, then the delay is inversely proportional to the variable I_{source}. The frequency of a ring-oscillator VCO is, therefore, directly proportional to I_{source}, with the desirable positive linear slope.

Note that for high rejection of power supply noise the differential signal is referenced to V_{SS} and the variable current source is cascoded for high impedance to V_{CC} supply.

B. Voltage-Controlled Resistor (VCR)

Fig. 12 describes the circuit used as a VCR. The voltage applied to R_{control} controls the impedance of MOSFET devices $M1$ and $M3$ and thus the current into node "IN" for a given voltage at "IN." For a V_{IN} range from 0 to 1.0 V, varying R_{control} voltage produces a family of I_{IN} versus V_{IN} curves shown in Fig. 12(b). These I–V characteristics provide the load for the differential delay element.

The VCR is a key component in the delay cell. What is required is an element that is suitable as a load resistor for source/drain voltages between 0 and 0.8 V (V_{ref}) and having the widest possible range of resistance to maximize the VCO frequency range of operation. As shown in Fig. 12, the VCR uses a combination of three N-MOSFET's to provide a more linear I_d versus V_d characteristic than a single MOSFET. This VCR circuit configuration has been able to achieve higher dynamic range than another VCR reported recently [4], due to the series $M3$ MOSFET. With the techniques described, the delay cell improved the power supply noise rejection of the VCO by six times to 0.7%/V compared to 4.5%/V previously reported [2].

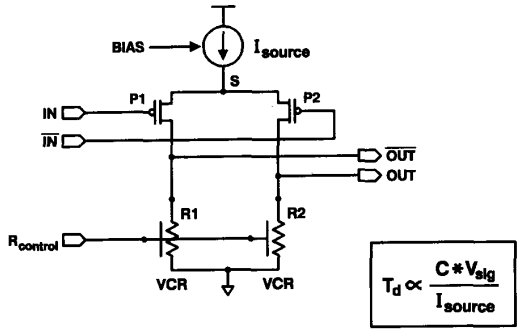


Fig. 11. Differential delay element.

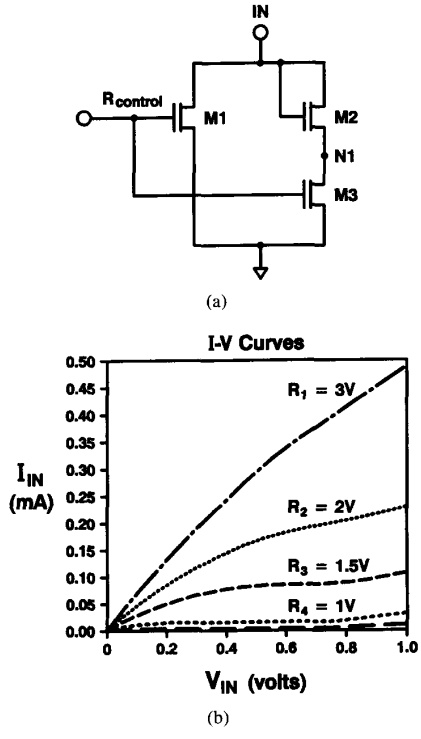


Fig. 12. Voltage-controlled resistor.

C. V–I Converter

Fig. 13 shows the additional circuits for the VCO using the differential delay element. To control the frequency with a voltage input signal, a voltage-to-current converter is realized using an NMOS source follower, applying the voltage across an n-well resistor. This transconductance is very linear and has a positive slope. The current sources are cascoded.

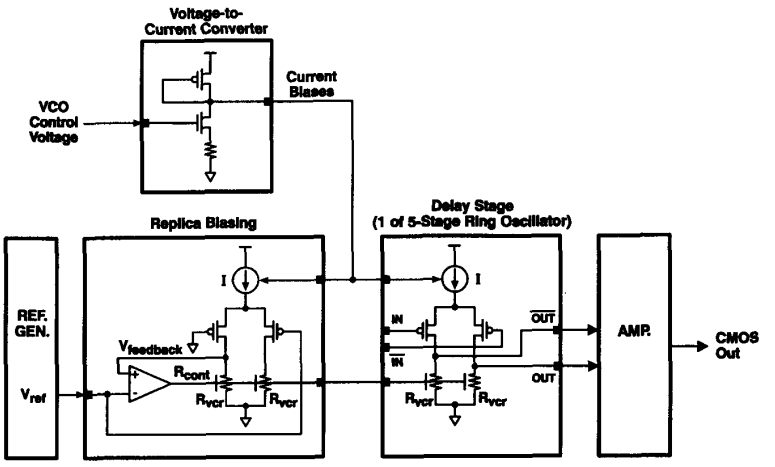


Fig. 13. Differential delay element VCO.

D. Replica Biasing

The signal amplitude is held constant by means of replica biasing and a power supply independent reference generator (V_{ref}). The replica biasing circuit uses an op amp and a copy of the delay cell to generate the appropriate bias to the VCR [2]. The replica biasing uses the same delay cell as the VCO, together with a differential amplifier. One input to the source-coupled p-channel pair is grounded (left input), while the other input is connected to V_{ref}. All the current I flows on the left side of the differential pair. This is the maximum signal condition. The amplifier gain is high enough to cause the feedback (drain of the VCR) to be equal to V_{ref}. Since $R_{control}$ is also used to bias the resistors in the VCO delay stages, the signal amplitude in the VCO is equal to V_{ref}. The V_{ref} voltage is about 0.8 V. The amplifier at the output of the ring oscillator converts the small-signal swing to CMOS levels.

The voltage swing reference generator (V_{ref}) in Fig. 13 is a self-biasing supply-independent MOSFET current source, based on the mobility difference between two N-MOSFET's with different current density. This current source is mirrored into a diode-connected N-MOSFET to generate a voltage bias that tracks with the N-MOSFET based VCR's process variation.

VI. CMOS Process Technology

This PLL clock generator was realized using a 0.8-μm n-well CMOS technology. The features of this process are shown in Table I. The PLL circuit has been realized in both two- and three-layer metal versions of this process.

The die photograph of the PLL located on a 1.2-million-transistor microprocessor die, using the 0.8-μm CMOS three-layer metal process, is shown in Fig. 14(a). The area occupied by the PLL circuit is 0.31 mm^2, less than 0.4% of this 82-mm^2 processor die [1]. Fig. 14(b) shows the enlarged micrograph of the PLL circuit. It can be seen that digital signals are routed over the circuit in the third layer of metal.

TABLE I
0.8-μm CMOS Parameter Summary

MOSFET Parameters		
	NMOS	PMOS
T_{ox}	150 Å	150 Å
S/D	LDD	LDD
L_{eff}	0.6 μm	0.6 μm
V_t	0.6 V	0.6 V
I_{dsat}	0.4 mA/μm	0.2 mA/μm

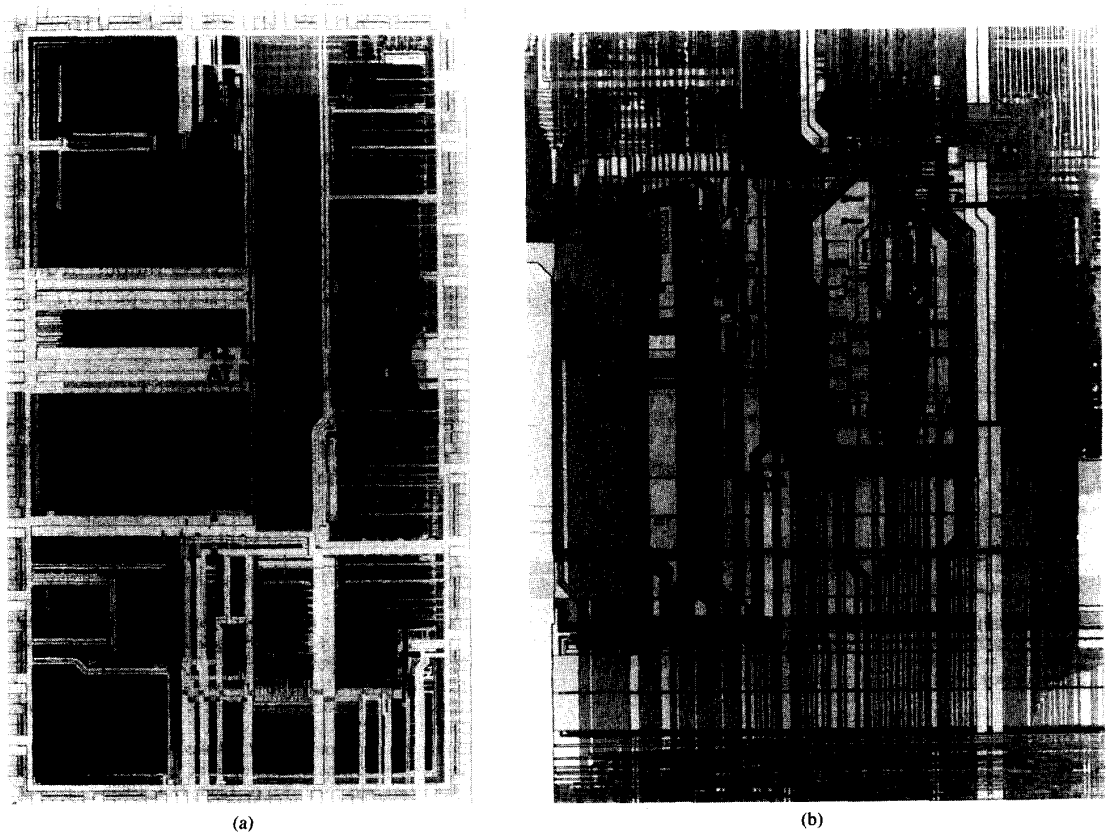
Process Parameter Silicided Source/Drain & Poly	
Metal 1 Pitch	2.0 μm
Metal 2 Pitch	2.4 μm
Metal 3 Pitch	2.4 μm—*optional

VII. Measured Results

Table II shows the measured performance of the clock generator when functioning with the microprocessor running at 50 MHz. Table III summarizes the measured characteristics of the VCO circuit used in this PLL.

To characterize the PLL rejection of power supply noise, Fig. 15 shows the transient phase error response of the PLL to a positive or negative 500-mV step on the V_{CC} level (5.75 to 6.25 V for worst case). The peak-to-peak jitter was found to scale with the size of the step. The same step response over the range of input clock periods is given in Fig. 16.

Fig. 17 shows that the clock skew (of internal clock relative to the external clock) is 88 ps at a clock frequency of 66 MHz. Fig. 18 is a digital oscilloscope display of the rising edge of the internal clock superimposed with a histogram of its jitter. It compares the jitter when the microprocessor is running a quiet pattern to the jitter when it is



(a) (b)

Fig. 14. (a) Microprocessor micrograph. (b) PLL detail photograph.

TABLE II
MICROPROCESSOR RUNNING TEST PROGRAM AT 50 MHz

Peak-to-Peak Jitter	<0.3 ns
Phase Error (Skew)	<0.1 ns @ 50 MHz
PLL Lock-in Time	75 μs
PLL Power Dissipation	16 mW
Silicon Area of PLL (w/o clock driver)	0.31 mm^2/500 mil^2

TABLE III
VCO MEASURED CHARACTERISTICS (5 V, 25°C)

Frequency Range	10 to 220 MHz
Sensitivity Range	43 MHz/V @ 120°C 77 MHz/V @ 0°C
Supply Sensitivity	0.7%/V
Temperature Sensitivity	4700 ppm/°C

running the noisy test pattern. It can be seen that there is not a significant increase in the level of jitter between these two test cases; the peak-to-peak jitter increases from 244 to 280 ps and rms jitter (σ) increases from 36 to 39.3 ps.

The measured schmoo diagram of the PLL clock generator's functional operating frequency versus supply voltage is shown in Fig. 19 (circuit operating with N =

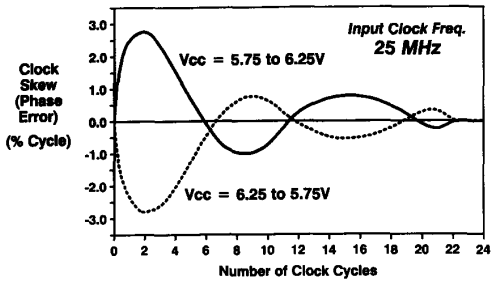


Fig. 15. 500-mV power supply step response.

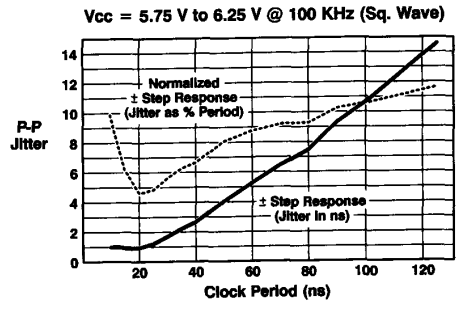


Fig. 16. Power supply rejection test.

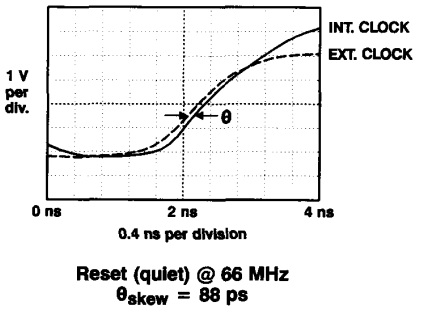


Fig. 17. Clock skew measured results.

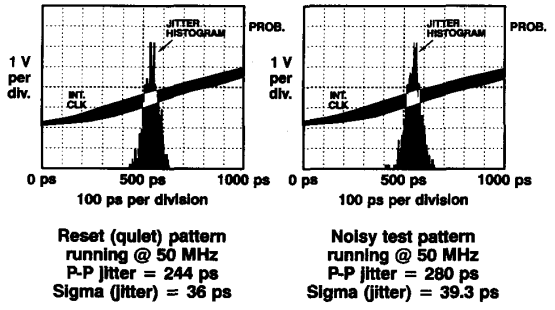


Fig. 18. Jitter measured results.

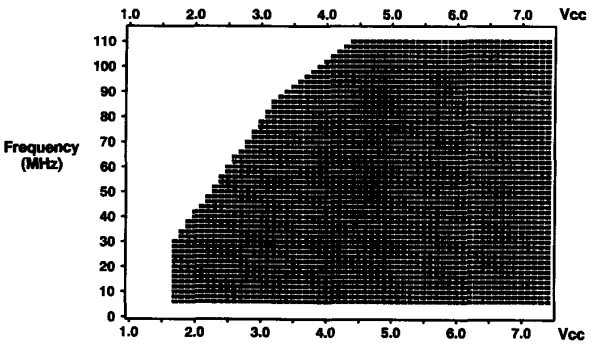


Fig. 19. PLL schmoo plot.

1). The operation of the PLL with external input frequency as low as 5 MHz and as high as 100 MHz has been demonstrated. Since this PLL implementation provides a 50% duty cycle clock regardless of input duty cycle, the PLL VCO is operating as high as 220 MHz.

VIII. Conclusion

This circuit has demonstrated that a PLL analog circuit can be integrated into a large microprocessor chip and provide the deskewing accuracy required for clock frequency synthesis up to more than 100 MHz, with clock skew of less than 0.1 ns and peak-to-peak jitter of less than 0.3 ns (with an rms jitter of less than 40 ps). To achieve this, a PLL with a significantly improved power supply rejection was realized, realizing a 30 times improvement factor compared to conventional PLL implementations.

Low generated internal clock skew and jitter was achieved without the need for any external components. This PLL operates in lock over a wide operating frequency range from 5 to 110 MHz, more than a factor of 20. Internal to the PLL, the VCO output frequency has achieved high-frequency operation, operating up to 220 MHz.

Acknowledgment

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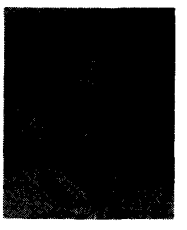
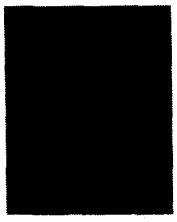


Ian A. Young (S'73–M'78) was born in Melbourne, Australia, on March 5, 1951. He received the B.E. and M.Eng.Sci. degrees in electrical engineering from the University of Melbourne in 1972 and 1975, respectively. He received the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1978.

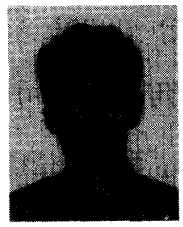
He was a consultant to American Microsystems, Inc. from 1976 to 1978 developing switched-capacitor circuits for telecommunications. He taught at the University of California, Berkeley, in 1977. From 1978 to 1981 he worked for Mostek Corporation, designing MOS integrated circuits for telecommunications applications. From 1981 to 1983 he worked as an industrial consultant designing analog/digital MOS integrated circuits. In 1983 he joined the Technology Development department of Intel Corporation in Portland, OR, where he is currently a Principal Engineer and Program Manager of the Advanced Design group. At Intel he has been involved with the development of high-speed CMOS and BiCMOS circuit design techniques, phase-locked-loop clock generation and distribution, interconnect capacitance and device modeling, and process technology development for advanced microprocessors and high-speed memory. He holds 12 patents.

Dr. Young is a member of the Program Committees for the International Solid-State Circuits Conference and the VLSI Circuits Symposium.



Jeffrey K. Greason received the B.S.E.E. degree from the California Institute of Technology, Pasadena, in 1988.

He joined the Portland Technology Development group of Intel Corporation in Portland, OR, in 1987, and from 1989 to 1990 worked on the 50-MHz version of the i486 microprocessor. During 1991 he was involved in the definition of Intel's first BiCMOS technology. Since then he has been designing high-speed chips early in the development of advanced logic technology, an activity which he now heads. His current interests include high-speed MOS and BiCMOS analog and digital circuit design, design automation, advanced logic process development, and design for reliability.



Keng L. Wong (M'91) was born in Malaysia, in 1962. He received the B.S. and M.Eng. degrees in electrical engineering from Cornell University, Ithaca, NY, in 1985 and 1986, respectively.

He first joined Intel, Chandler, AZ, in 1986, where he was engaged in microcontroller and EPROM design. Since 1988 he has been with Intel's Portland Technology Development, Hillsboro, OR, where he has been involved with advanced microprocessor circuit design. His current interests include phase-lock techniques in clock generation, high-frequency clock distribution, and VLSI analog/digital circuit design.