Lecture 11: Charge Pump Circuits

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Announcements & Agenda

• Exam 1 is on Wed. Oct 3
  • One double-sided 8.5x11 notes page allowed
  • Bring your calculator
  • 2 reference exams posted on the website, but no solutions available 😞

• Charge pump circuits
  • Basic operation
  • Techniques to improve static and dynamic current source matching
References


• Additional PLL/charge-pump papers that I will post on the website
Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider
Charge Pump

- Converts PFD output signals to charge
- Charge is proportional to PFD pulse widths

PFD-CP Gain: \( \left( \frac{1}{2\pi} \right) I_{CP} \)
Charge Pump Implementations

Single-Ended

\[ \text{up}(t) \quad \text{down}(t) \]

\[ I_{cp} \quad I_{out}(t) \]

[Perrott]

Fully Differential

\[ VDD \]

\[ M_3 \quad M_2 \quad M_1 \quad M_1 \quad M_2 \quad M_3 \]

\[ \text{Vo-} \quad \text{UP} \quad \text{Vo-} \]

\[ I_{cp} \quad I_{cp} \]

[Li TCAS1 2008]
Simple Charge Pump

- Issues
  - Skew between UPB and DN control signals
  - Matching of UP/DN current sources
  - Clock feedthrough and charge injection from switches onto $V_{ctrl}$
  - Charge sharing between current source drain nodes’ capacitance and $V_{ctrl}$
Simple Charge Pump Skew Compensation

- Adding a transmission gate in the DN signal path helps to equalize the delay with the UPB signal for better overlap between the UP and DN current sources.

[Razavi]
Charge Pump Mismatch

- Recall that in order to eliminate the PLL deadzone, both UP and DN current sources should be on for a minimum period.
- PLL will lock with static phase error if there is a charge pump mismatch.
- Extra “ripple” on Vctrl.
  - Results in frequency domain spurs at the reference clock frequency offset from the carrier.

[Diagram showing ideal vs. actual locked conditions with charge pump mismatch]
PLL Output Spectrum w/ Spurs

• A 5GHz clock synthesized with a PLL utilizing a 200MHz reference clock
• Spurs appear at $\pm f_{\text{ref}}$ relative to the carrier frequency

[Fischette]
Charge Sharing on $V_{\text{ctrl}}$

- When switches are off, the PMOS current source drain discharges to $V_{DD}$ and the NMOS current source drain discharges to GND.
- When switches are on, charge sharing occurs between the loop filter capacitance and these current source drain nodes, causing a level-dependent disturbance on $V_{\text{ctrl}}$.

[Diagram showing the charge sharing circuit with switches $S_1$ and $S_2$.]
Charge Pump w/ Improved Matching

- Parallel path keeps current sources always on
- Amplifier keeps current source Vds voltages constant resulting in reduced transient current mismatch (charge sharing)

[Young J SSC 1992]
Charge Pump w/ Reversed Switches

- Swapping switches reduces charge injection
  - MOS caps (Md1-4) provide extra charge injection cancellation
- Helper transistors Mx and My quickly turn-off current sources
- Dummy branch helps to match PFD loading
- Helps with charge injection, but charge sharing is still an issue

[Ingino J SSC 2001]
Fully-Differential Charge Pump

- CMFB loop adjusts the top current sources to match $I_{CP}$ at the differential loop filter common-mode level
This fully-differential charge pump uses many techniques to match the UP/DN current sources and mitigate charge injection and charge sharing:

- Dummy path with feedback amplifiers to match current source $V_{DS}$
- Dummy switches M1’ and M3’ provide charge injection cancellation
- CMFB circuit matches UP/DN current at the filter common-mode output
- Left and right-most feedback loop improve matching considering the differential loop filter control voltage
- Additional PMOS current sources M11 & M12 extend matching over a wide voltage range
Improved Matching w/ Differential Output

• The CMFB loop compensates for current source mismatch at the common-mode level
• However, it cannot compensate for current source mismatch due to the differential control output voltage, as this voltage is symmetric with the common-mode
• Additional feedback networks (OP1 & OP2) provide for improved matching with the differential control output voltage

Fig. 4. Output currents with and without mismatch suppression.

[Cheng TCAS2 2006]
Additional Current Variation Suppression

While matching is good at the control voltage extremes, the absolute current value falls due to finite current source output resistance.

Additional PMOS current sources M1 and M2 provide additional NMOS current when the single-ended control voltage is low, which the main PMOS current source then tracks via feedback.

This extends the voltage range over which the absolute charge pump current matches its nominal value.
Next Time

• Loop Filter Circuits