ECEN620: Network Theory Broadband Circuit Design Fall 2023

Lecture 9: Digital PLLs

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Announcements

- HW3 due Oct 31
- HW4 due Nov 7

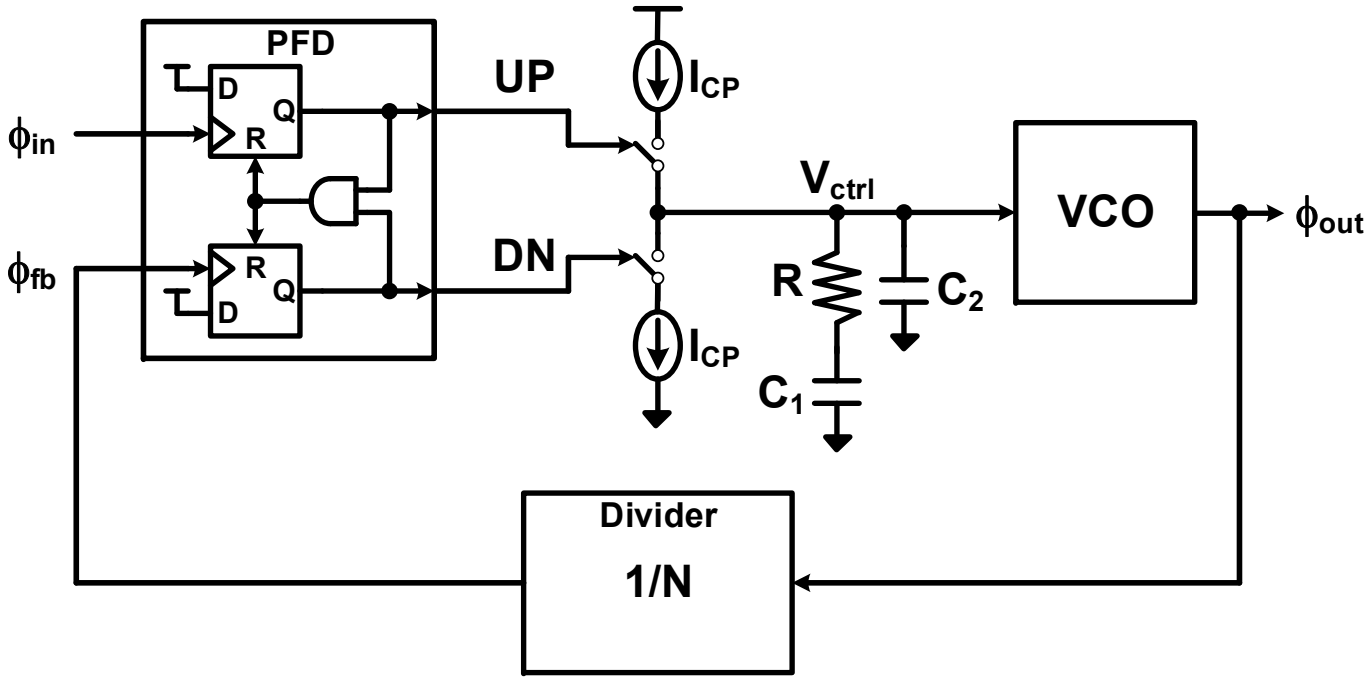
Agenda

- Digital PLL Overview
- Linear Model
- Design Procedure
- Noise Analysis
- Time-to-Digital Converters
- Conclusion

References

- *Techniques for High-Performance Digital Frequency Synthesis and Phase Control*, C.-M. Hsu, MIT Thesis, 2008.
- [Kratyuk TCAS2 2007] provides a nice design procedure
- TDC papers posted on the website

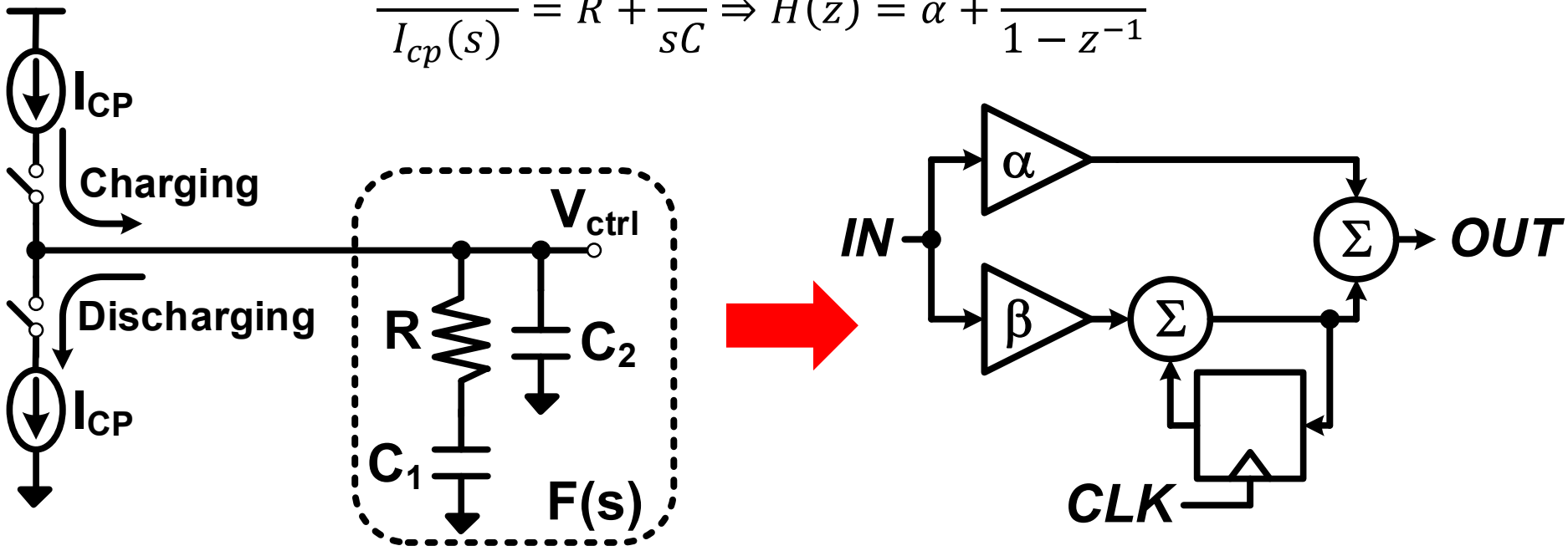
Analog PLL Issues



- Charge pump suffers from UP/DN current mismatch, low output impedance, and leakage
- Loop filter is large area and has noise and leakage
- Can we map this functionality to the digital domain?

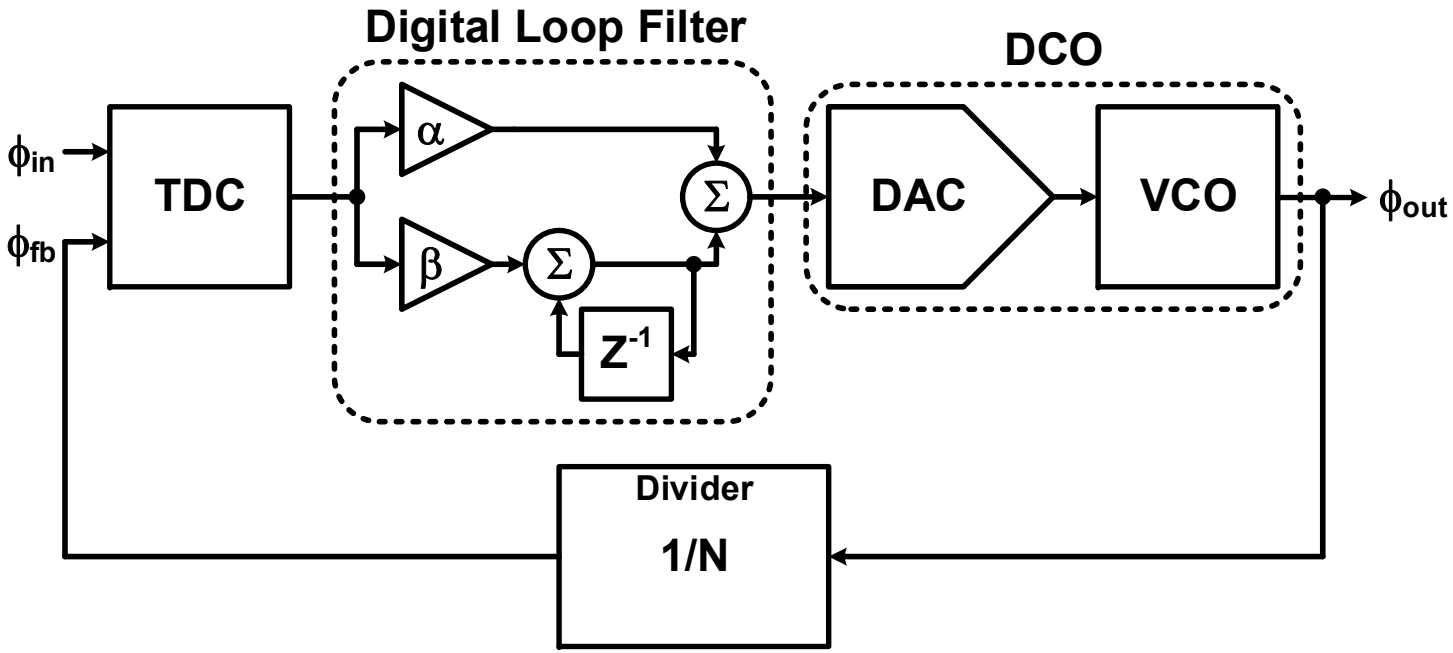
Digital Mapping of CP & Loop Filter

$$\frac{V_{ctrl}(s)}{I_{cp}(s)} = R + \frac{1}{sC} \Rightarrow H(z) = \alpha + \frac{\beta}{1 - z^{-1}}$$



- Analog filter resistive proportional and capacitive integral gain is mapped to a digital filter
- Large filter capacitor is replaced with a small digital accumulator
- Requires a digital input from a phase/time-to-digital converter

Digital PLL



- Time-to-digital (TDC) converts input phase error to a digital word
- Digital loop filter provides PI control to allow for a Type 2 system
- Digitally-controlled oscillator (DCO) produces the output clock signal

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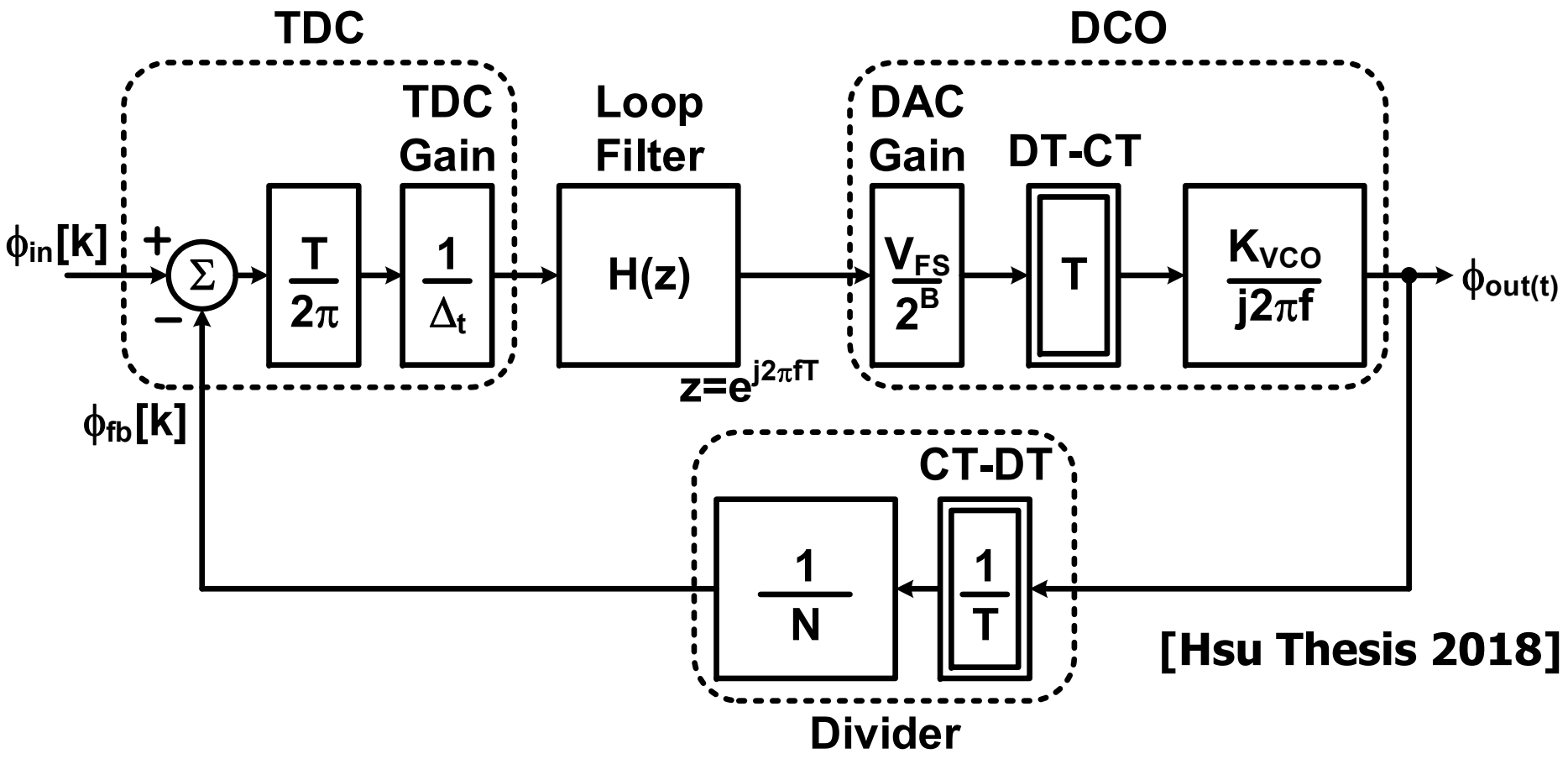
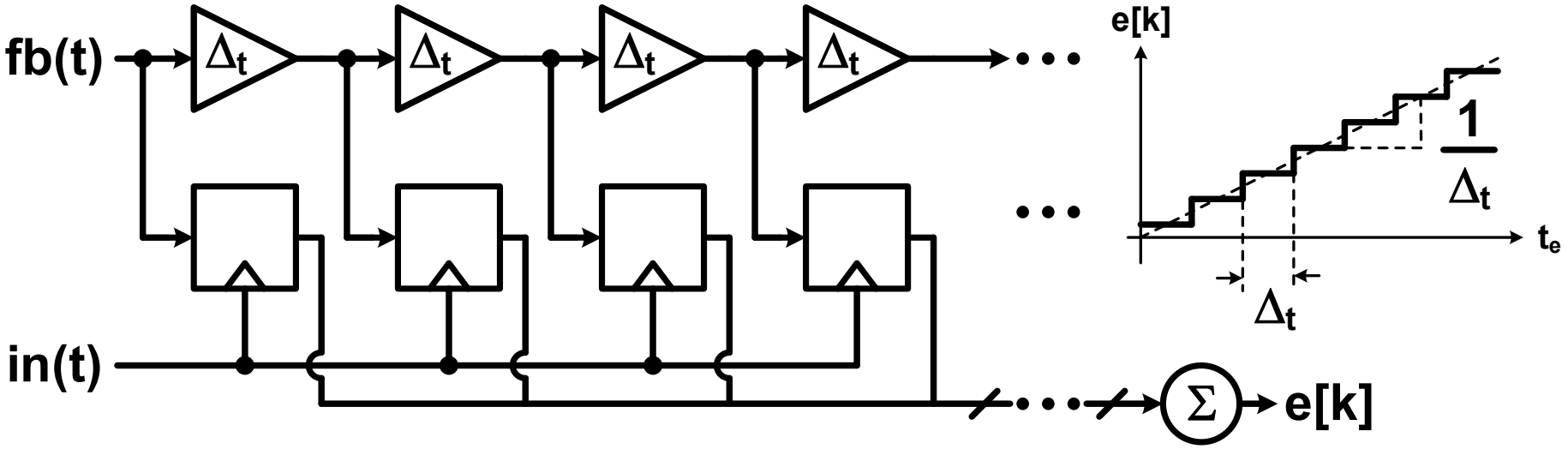
Digital PLL Model



- A hybrid discrete- and continuous-time model is used to capture the effects of important noise sources

TDC Model



- TDC converts the time difference between the input and feedback clocks to a digital code at a resolution Δ_t

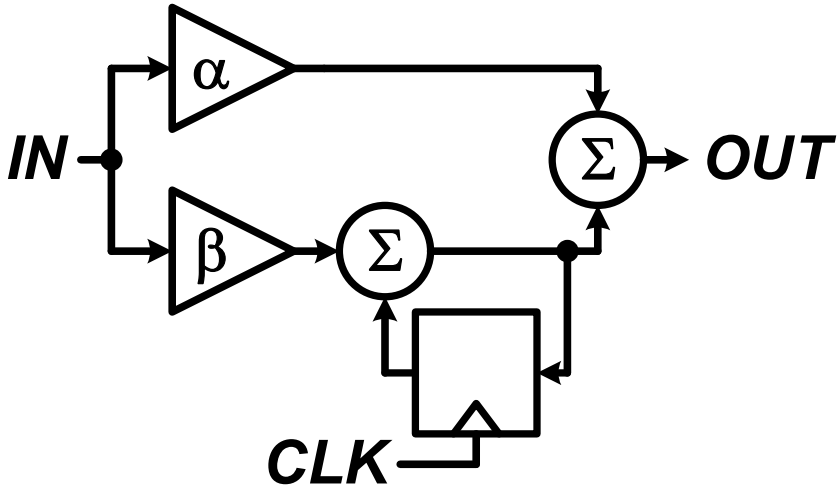
$$\text{TDC Gain} = \frac{1}{\Delta_t} \; with\ units\ of\ s^{-1}$$

- Phase-domain model requires an initial scaling factor to convert the input phase error to a timing error

$$t_e = \phi_e \left(\frac{T}{2\pi} \right)$$

$$\text{Effective TDC Gain} = \frac{T}{2\pi\Delta_t} \; with\ units\ of\ rad^{-1}$$

Digital Loop Filter



Analog Filter Transfer Function

$$F(s) = \frac{R\left(s + \frac{1}{RC}\right)}{s}$$

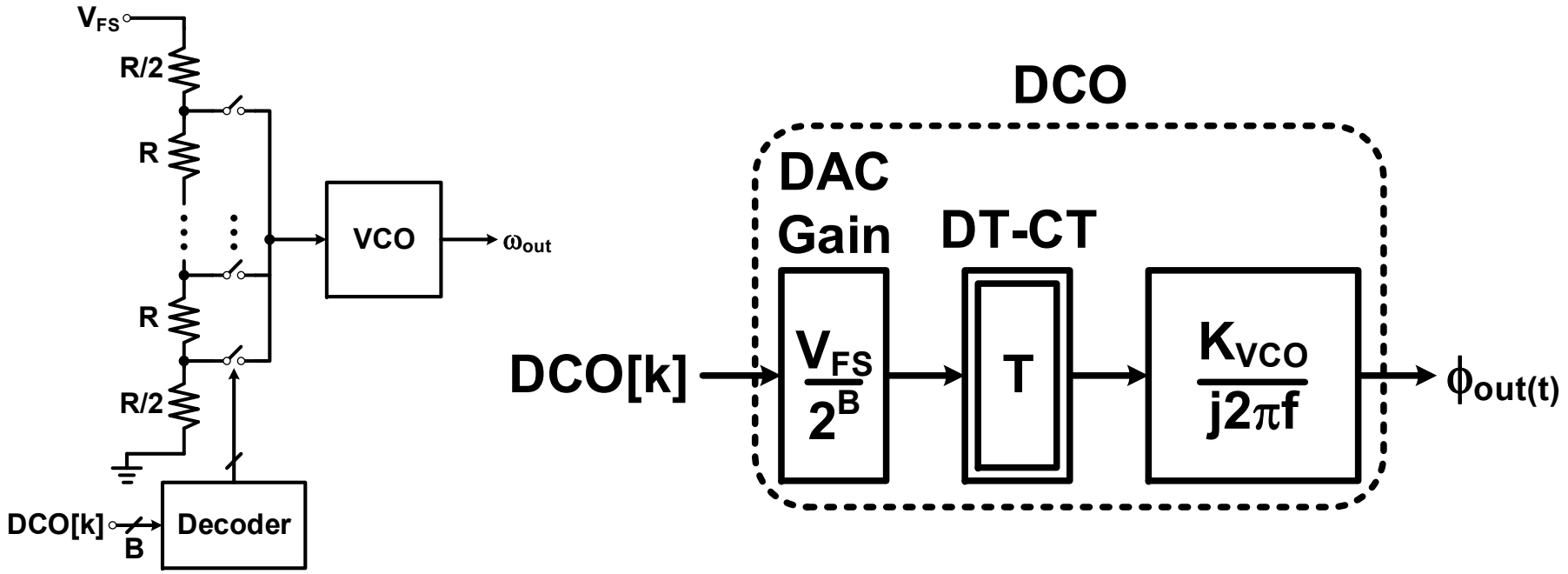
w/ Bilinear Transform

$$H(z) = \frac{OUT}{IN} = \alpha + \frac{\beta}{1 - z^{-1}} \xrightarrow{s=\left(\frac{2}{T}\right)\left(\frac{1-z^{-1}}{1+z^{-1}}\right)} H(s) = \frac{\left[\alpha + \frac{\beta}{2}\right]\left[s + \frac{\beta}{\left(\alpha + \frac{\beta}{2}\right)T}\right]}{s}$$

- Matching the analog filter transfer function results in

$$\alpha = R - \frac{T}{2C} \qquad \beta = \frac{T}{C}$$

DCO Model



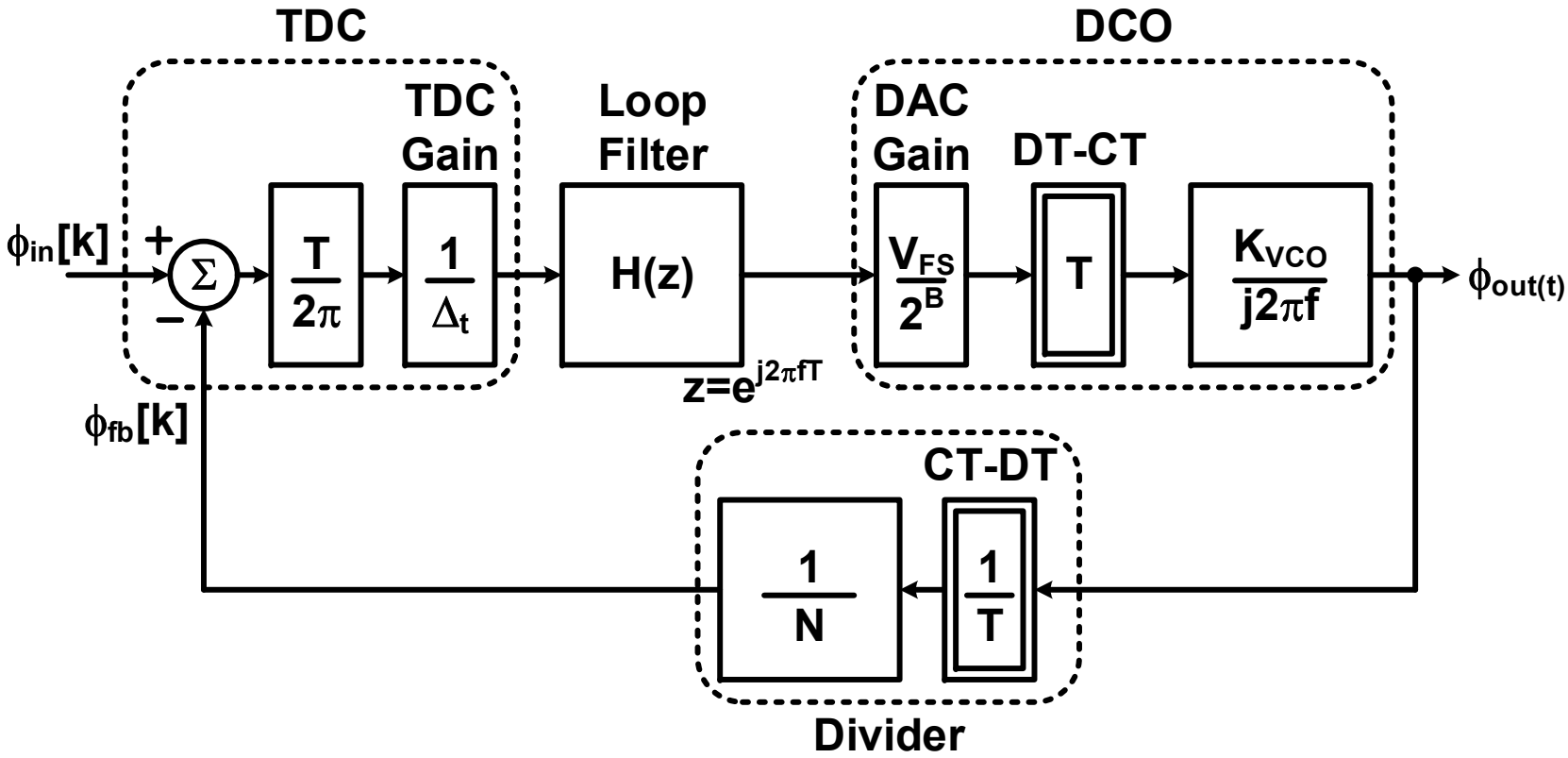
- DCO modelled as a DAC followed by a VCO

$$\text{DAC Gain} = \frac{V_{FS}}{2^B} \quad (V/LSB)$$

- Converting from DT-CT requires scaling by reference period T
- Standard phase-domain VCO model utilized

$$\text{DCO Gain} = \left(\frac{V_{FS}}{2^B}\right) T K_{VCO} \quad \left(\frac{rad}{s \cdot LSB}\right)$$

Linear Digital PLL Model

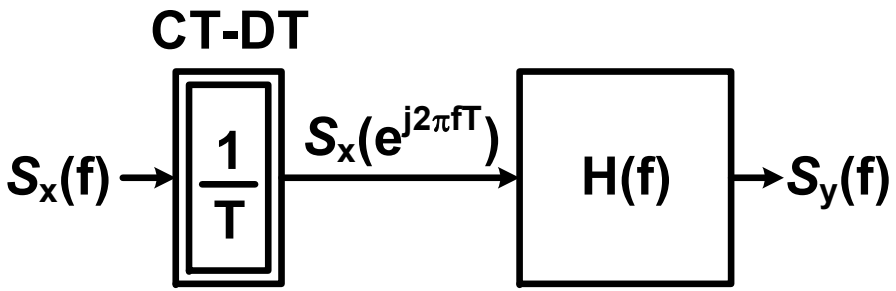


$$H(z) = \frac{(\alpha+\beta) - \alpha z^{-1}}{1 - z^{-1}} \xrightarrow{z=e^{j2\pi fT}} H\left(e^{j2\pi fT}\right) = \frac{(\alpha+\beta) - \alpha e^{-j2\pi fT}}{1 - e^{-j2\pi fT}}$$

$$\frac{\phi_{out}}{\phi_{in}} = \frac{N \cdot T \cdot LG(f)}{1 + LG(f)} = \frac{(T)\left(\frac{T}{2\pi}\right)\left(\frac{1}{\Delta_t}\right)H\left(e^{j2\pi fT}\right)\left(\frac{V_{FS}}{2^B}\right)\left(\frac{K_{VCO}}{j2\pi f}\right)}{1 + \left(\frac{T}{2\pi}\right)\left(\frac{1}{\Delta_t}\right)H(e^{j2\pi fT})\left(\frac{V_{FS}}{2^B}\right)\left(\frac{K_{VCO}}{j2\pi f}\right)\left(\frac{1}{N}\right)}$$

DT & CT Spectral Density Calculations

Since $H(f)$ is computed with a DT input, a CT $S_x(f)$ must be first converted to a DT $S_x\left(e^{j2\pi fT}\right)$ by scaling with $\left(\frac{1}{T}\right)$



$$S_x\left(e^{j2\pi fT}\right) = \left(\frac{1}{T}\right) S_x(f)$$

Computing a CT $S_y(f)$ output with a DT $S_x\left(e^{j2\pi fT}\right)$ input through $H(f)$ requires scaling by $\left(\frac{1}{T}\right)$

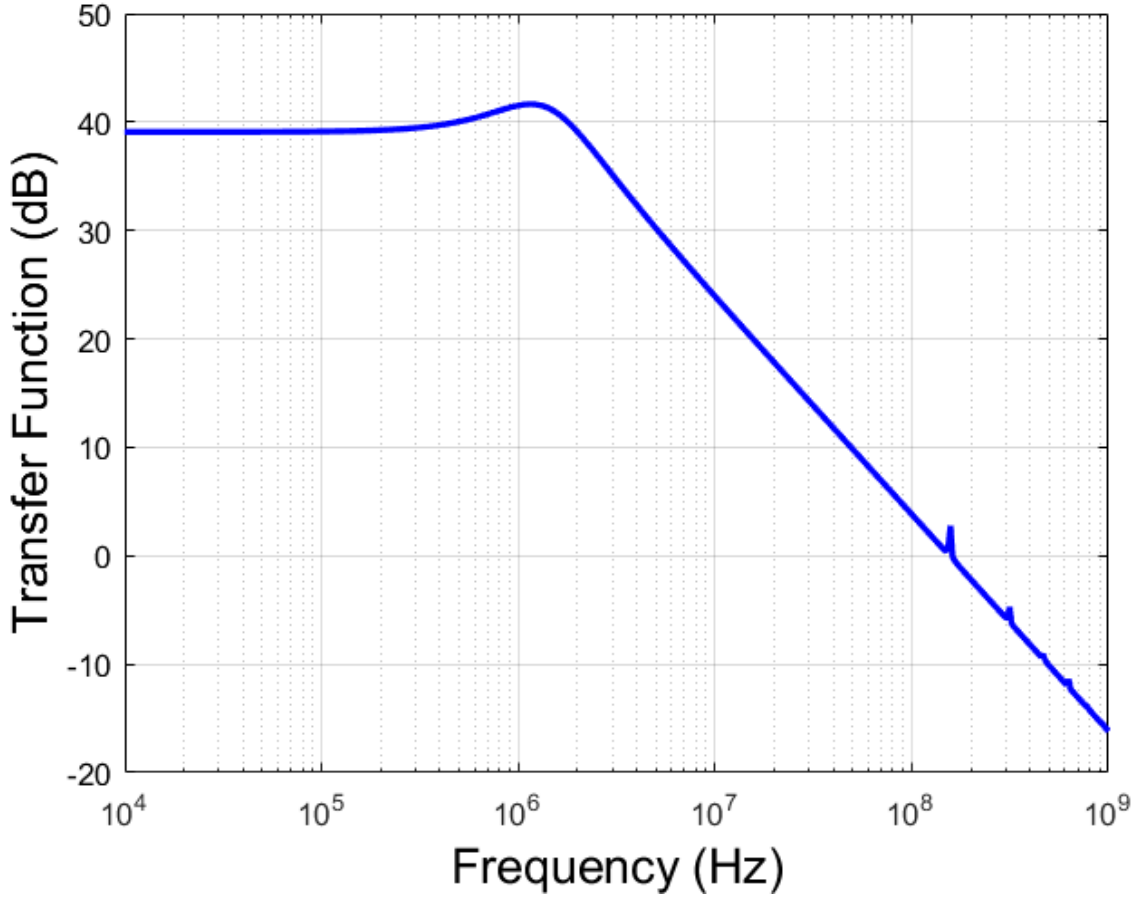
$$S_y(f) = \left(\frac{1}{T}\right) |H(f)|^2 S_x\left(e^{j2\pi fT}\right)$$

Total system output with $S_x(f)$

$$S_y(f) = \left(\frac{1}{T}\right)^2 |H(f)|^2 S_x(f)$$

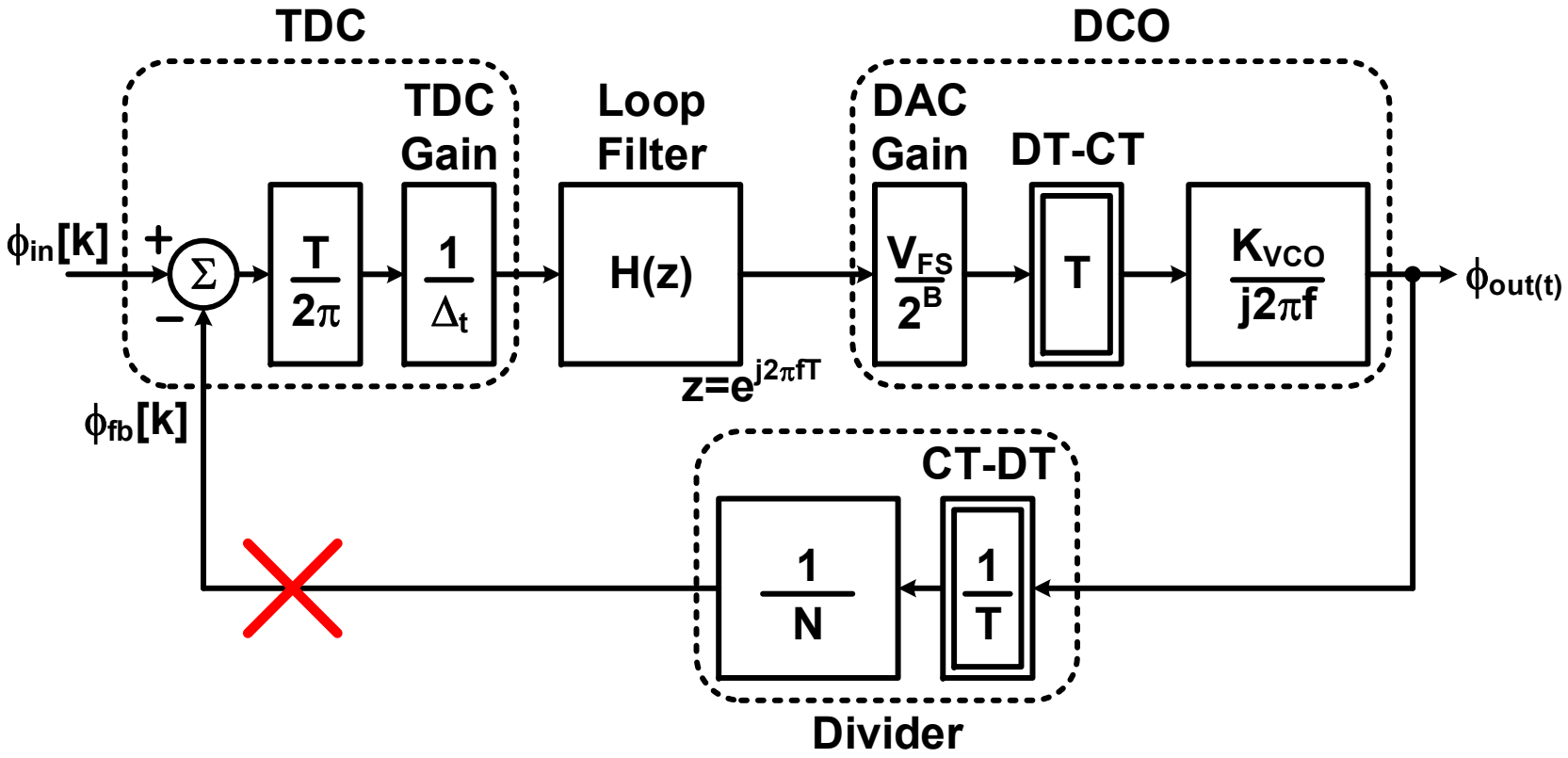
14GHz Digital PLL
Closed-Loop Transfer Function (Initial Design)

Parameter	
Fref	156.25MHz
N	90
Fvco	14GHz
f_u	2MHz
Φ_m	60°
f_{3dB}	2.7MHz
Δ_t	10ps
$(V_{FS}/2^B)Kvco$	2π*1MHz/LSB (10b)
α	1.49
β	7.11e-2



$$\frac{\phi_{out}(f)}{\phi_{in}(f)} = \left(\frac{1}{T}\right)^2 \left| \frac{(T)\left(\frac{T}{2\pi}\right)\left(\frac{1}{\Delta_t}\right)H(e^{j2\pi fT})\left(\frac{V_{FS}}{2^B}\right)\left(\frac{K_{VCO}}{j2\pi f}\right)}{1+\left(\frac{T}{2\pi}\right)\left(\frac{1}{\Delta_t}\right)H(e^{j2\pi fT})\left(\frac{V_{FS}}{2^B}\right)\left(\frac{K_{VCO}}{j2\pi f}\right)\left(\frac{1}{N}\right)} \right|^2$$

Digital PLL Loop Gain



$$LG(f) = \left(\frac{T}{2\pi}\right)\left(\frac{1}{\Delta_t}\right)H\left(e^{j2\pi fT}\right)\left(\frac{V_{FS}}{2^B}\right)\left(\frac{K_{VCO}}{j2\pi f}\right)\left(\frac{1}{N}\right)$$

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Second-Order Digital PLL Design Procedure

- Design the digital PLL to emulate a second-order analog charge-pump PLL [Kratyuk TCAS2 2007]

Digital PLL **Analog PLL**

$$LG(f) = \left(\frac{T}{2\pi}\right)\left(\frac{1}{\Delta_t}\right)H\left(e^{j2\pi fT}\right)\left(\frac{V_{FS}}{2^B}\right)\left(\frac{K_{VCO}}{j2\pi f}\right)\left(\frac{1}{N}\right) \Leftrightarrow LG(s) = \left(\frac{I_{CP}}{2\pi}\right)\left(\frac{R(s+\omega_z)}{s}\right)\left(\frac{K_{VCO}}{s}\right)\left(\frac{1}{N}\right)$$

Digital PLL PDC Gain $\left(\frac{T}{2\pi}\right)\left(\frac{1}{\Delta_t}\right) \Leftrightarrow \left(\frac{I_{CP}}{2\pi}\right)$ **Analog PLL PFD Gain**

Digital PLL Loop Filter $H(z) = \alpha + \frac{\beta}{1-z^{-1}} \Leftrightarrow F(s) = \frac{R(s+\omega_z)}{s}$ **Analog PLL Loop Filter**

Digital PLL Effective DCO Gain $\left(\frac{V_{FS}}{2^B}\right)(K_{VCO}) \Leftrightarrow (K_{VCO})$ **Analog PLL VCO Gain**

Second-Order Digital PLL Design Procedure

1. Set ω_z based on ω_u and Φ_m specs

$$\omega_z = \frac{\omega_u}{\tan(\Phi_m)}$$

$$\omega_u = 2\pi * 2MHz \ \& \ \Phi_m = 60° \rightarrow \omega_z = 2\pi * 1.16MHz$$

2. Compute an equivalent I_{CP} based on TDC gain

$$I_{CP} = \frac{T}{\Delta_t}$$

$$F_{ref} = 156.25MHz \ \& \ \Delta_t = 10ps \longrightarrow I_{CP} = 640A$$

3. Set an equivalent R value to achieve required loop gain

$$R = \left(\frac{2\pi N}{I_{CP}\left(\frac{V_{FS}}{2^B}\right)(K_{VCO})}\right)\frac{\omega_u^2}{\sqrt{\omega_z^2 + \omega_u^2}}$$

$$N = 90 \ \& \ \left(\frac{V_{FS}}{2^B}\right)(K_{VCO}) = \frac{2\pi * 1MHz}{LSB} \rightarrow R = 1.53\Omega$$

PLL Specs

Parameter	
Fref	156.25MHz
N	90
Fvco	14GHz
f_u	**2MHz**
Φ_m	**60°**
Δ_t	10ps
$(V_{FS}/2^B)Kvco$	2π*1MHz/LSB (10b)
α	??
β	??

Second-Order Digital PLL Design Procedure

4. Set an equivalent C value to achieve ω_z

$$C = \frac{1}{\omega_z R}$$

$$C = 90.1nF$$

5. Compute α and β from equivalent R and C values

$$\alpha = R - \frac{T}{2C} \qquad \beta = \frac{T}{C}$$

$$\alpha = 1.49 \;\; \& \;\; \beta = 7.11 * 10^{-2}$$

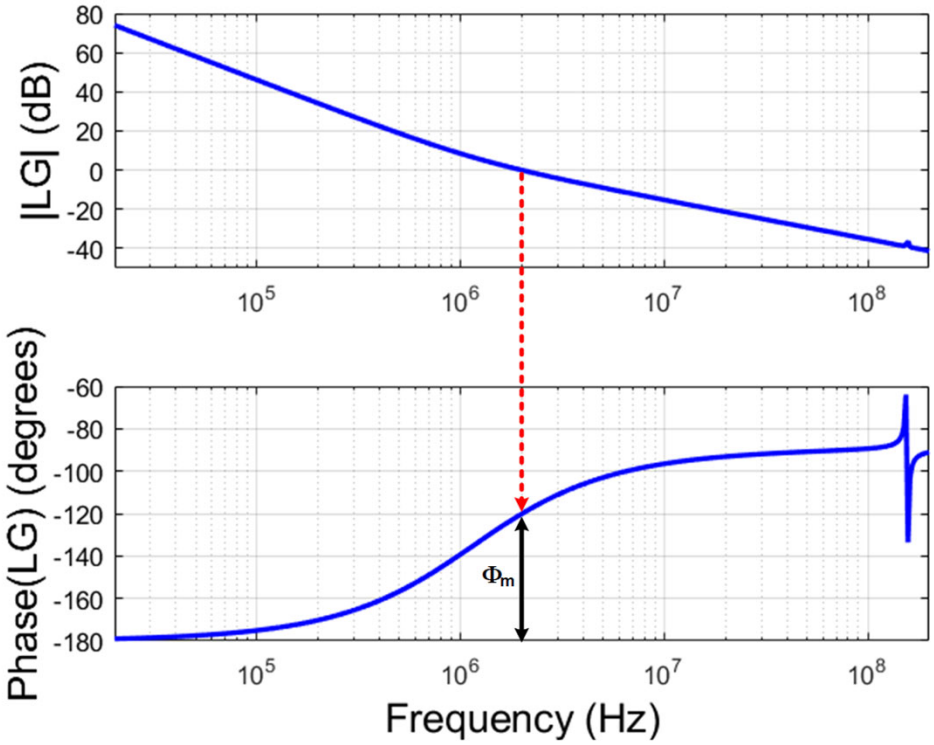
PLL Specs

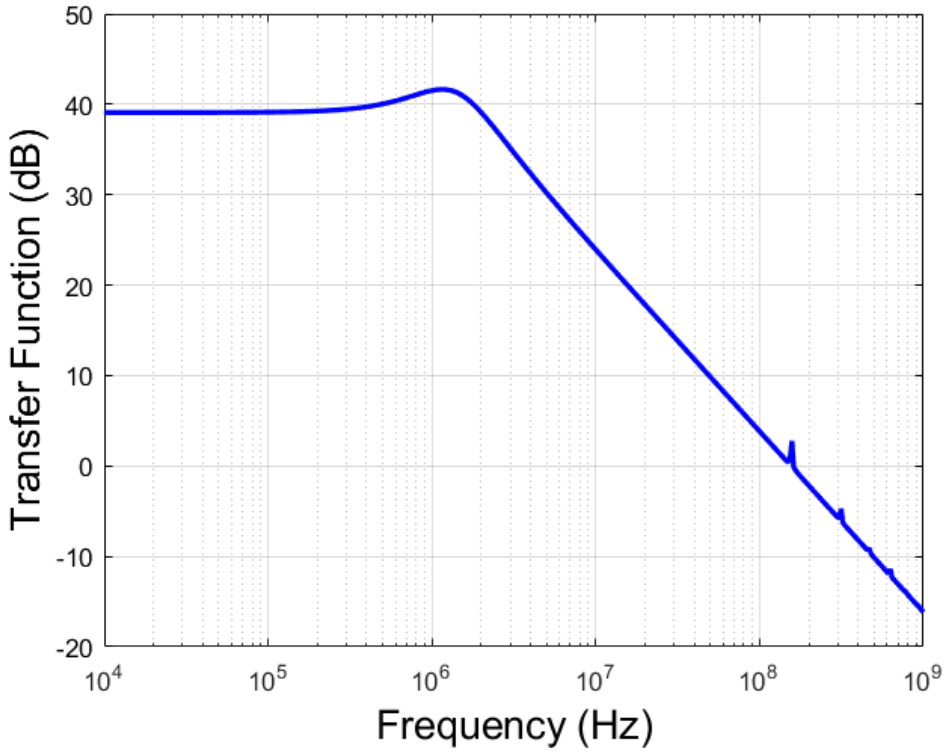
Parameter	
Fref	156.25MHz
N	90
Fvco	14GHz
f_u	2MHz
Φ_m	60°
Δ_t	10ps
$(V_{FS}/2^B)Kvco$	2π*1MHz/LSB (10b)
α	??
β	??

Simulated Responses

$$LG(f) = \left(\frac{T}{2\pi}\right)\left(\frac{1}{\Delta_t}\right)H(e^{j2\pi fT})\left(\frac{V_{FS}}{2^B}\right)\left(\frac{K_{VCO}}{j2\pi f}\right)\left(\frac{1}{N}\right)$$

$$\frac{\phi_{out}(f)}{\phi_{in}(f)} = \left(\frac{1}{T}\right)^2 \left| \frac{(T)\left(\frac{T}{2\pi}\right)\left(\frac{1}{\Delta_t}\right)H(e^{j2\pi fT})\left(\frac{V_{FS}}{2^B}\right)\left(\frac{K_{VCO}}{j2\pi f}\right)}{1+\left(\frac{T}{2\pi}\right)\left(\frac{1}{\Delta_t}\right)H(e^{j2\pi fT})\left(\frac{V_{FS}}{2^B}\right)\left(\frac{K_{VCO}}{j2\pi f}\right)\left(\frac{1}{N}\right)} \right|^2$$





- Design achieves f_u=2MHz and Φ_m=60°
- Closed loop response has f_{3dB}=2.7MHz

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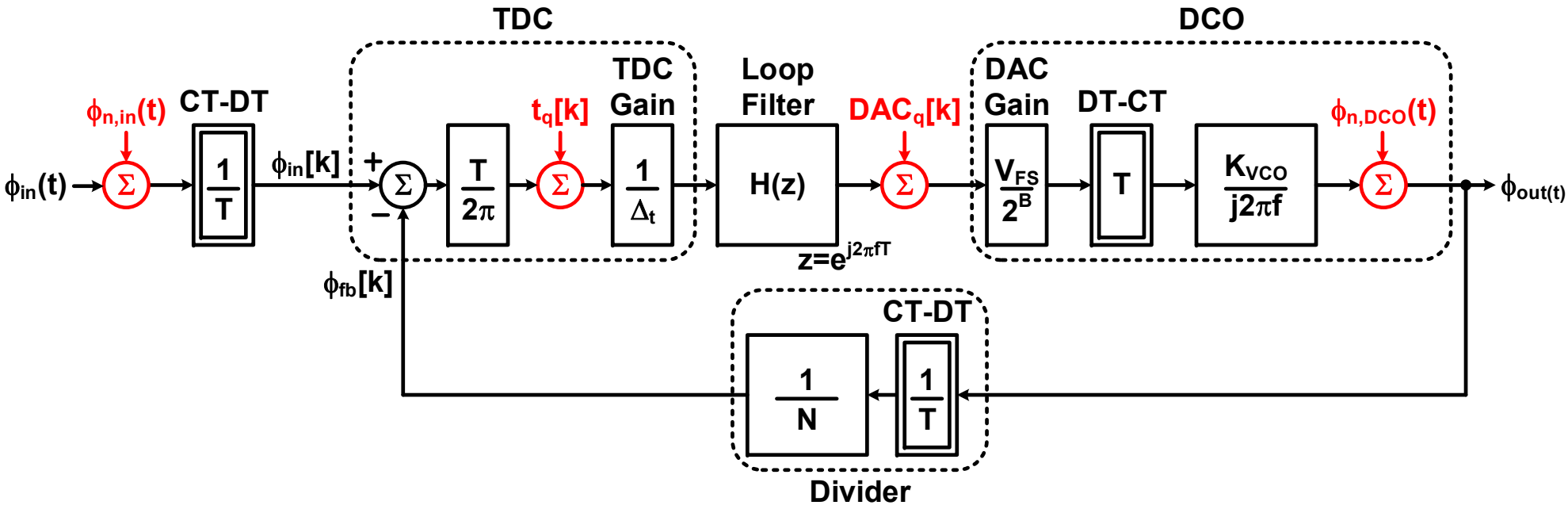
Common Digital PLL Noise Sources



$$S_{\phi_{out}}^{\phi_{in}}(f) = S_{\phi_{in}}(f)\left(\frac{1}{T}\right)^2 |NTF_{IN}(f)|^2$$

$$S_{\phi_{out}}^{t_q}(f) = S_{t_q}(e^{j2\pi fT})\left(\frac{1}{T}\right)|NTF_{TQ}(f)|^2$$

$$S_{\phi_{out}}^{DAC_q}(f) = S_{DAC_q}(e^{j2\pi fT})\left(\frac{1}{T}\right)|NTF_{DACQ}(f)|^2$$

$$S_{\phi_{out}}^{\phi_{DCO}}(f) = S_{\phi_{DCO}}(f)|NTF_{DCO}(f)|^2$$

$$S_{\phi_{out}}^{Total}(f) = S_{\phi_{out}}^{\phi_{in}}(f) + S_{\phi_{out}}^{t_q}(f) + S_{\phi_{out}}^{DAC_q}(f) + S_{\phi_{out}}^{\phi_{DCO}}(f)$$

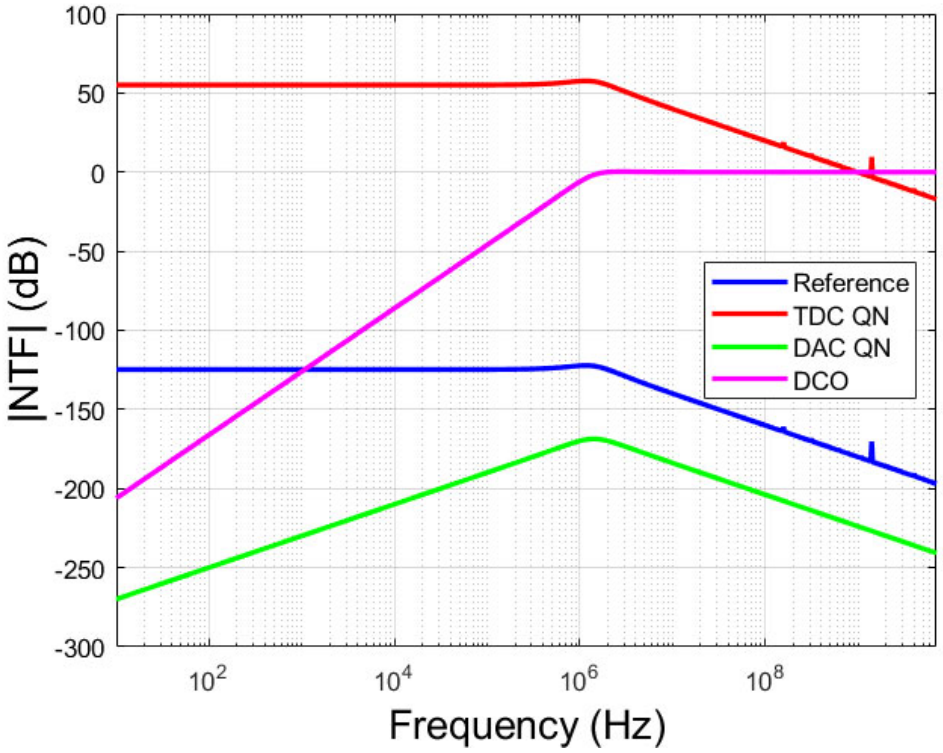
Noise Transfer Functions

$$NTF_{IN}(f) = \frac{\phi_{out}}{\phi_{in}} = \frac{N \cdot T \cdot LG(f)}{1 + LG(f)}$$

$$NTF_{TQ}(f) = \frac{\phi_{out}}{t_q} = \frac{N \cdot 2\pi \cdot LG(f)}{1 + LG(f)}$$

$$NTF_{QDAC}(f) = \frac{\phi_{out}}{q_{DAC}} = \frac{T\left(\frac{K_{VCO}}{j2\pi f}\right)}{1 + LG(f)}$$

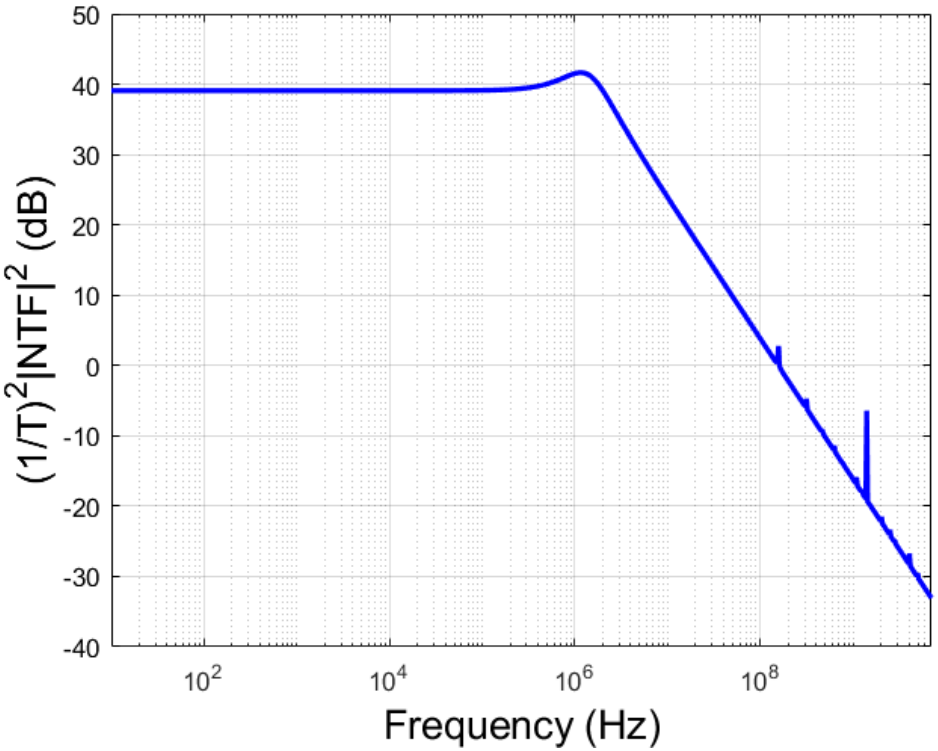
$$NTF_{DCO}(f) = \frac{\phi_{out}}{\phi_{DCO}} = \frac{1}{1 + LG(f)}$$

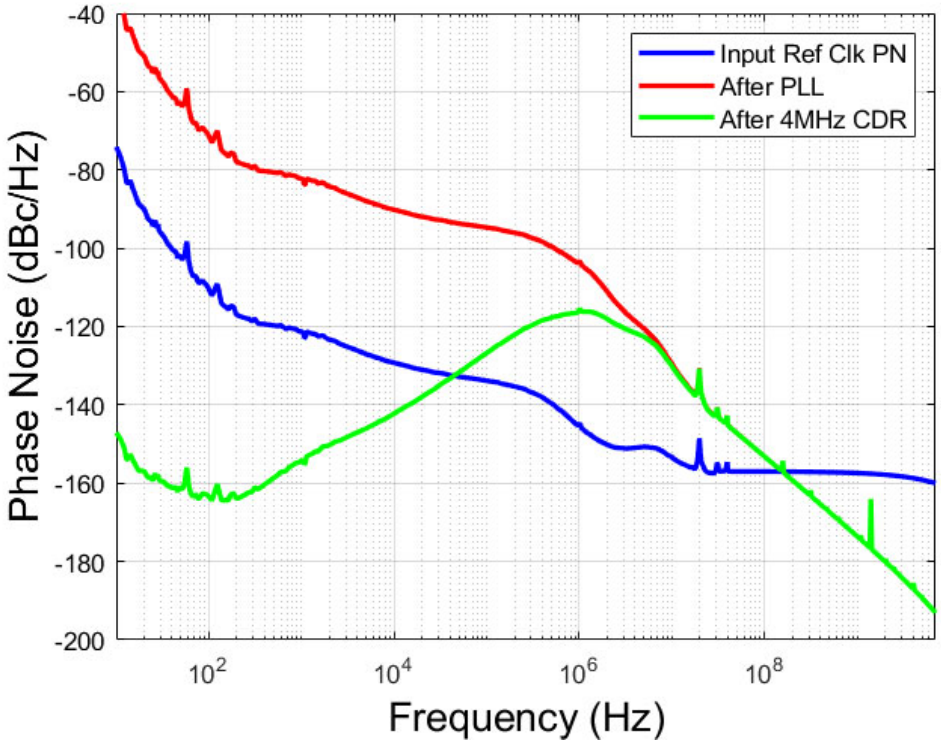


- Input reference and TDC quantization noise is low-pass filtered
- Loop filter output DAC quantization noise (DCO input noise) is band-pass filtered
- DCO output phase noise is high-pass filtered

Input Reference Noise

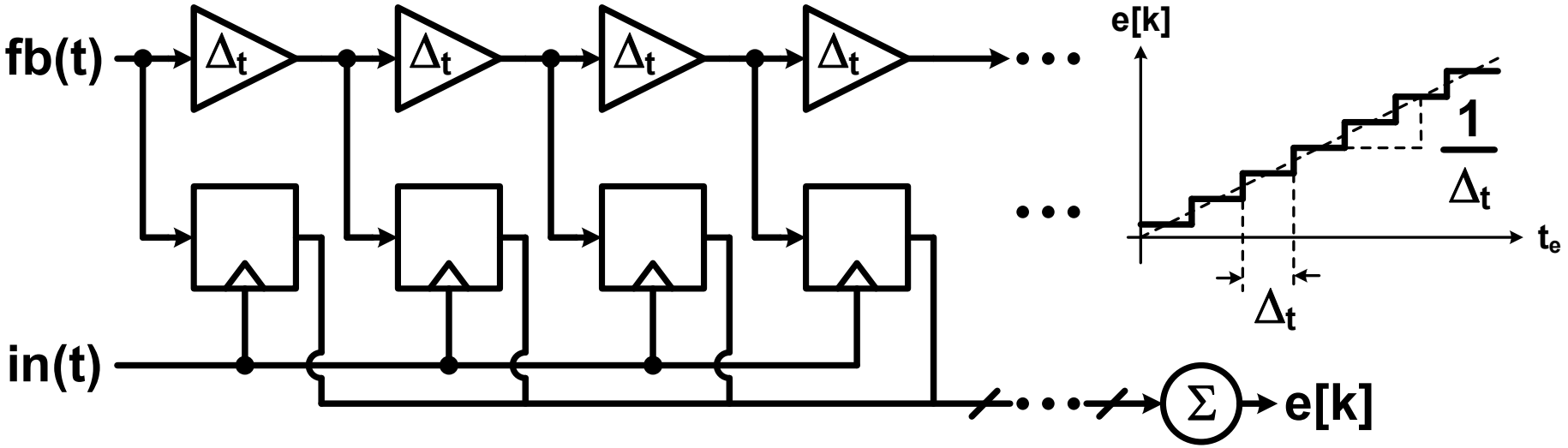
$$S_{\phi_{out}}^{\phi_{in}}(f) = S_{\phi_{in}}(f)\left(\frac{1}{T}\right)^2 |NTF_{IN}(f)|^2 = S_{\phi_{in}}(f)\left(\frac{1}{T}\right)^2 \left|\frac{N \cdot T \cdot LG(f)}{1 + LG(f)}\right|^2$$



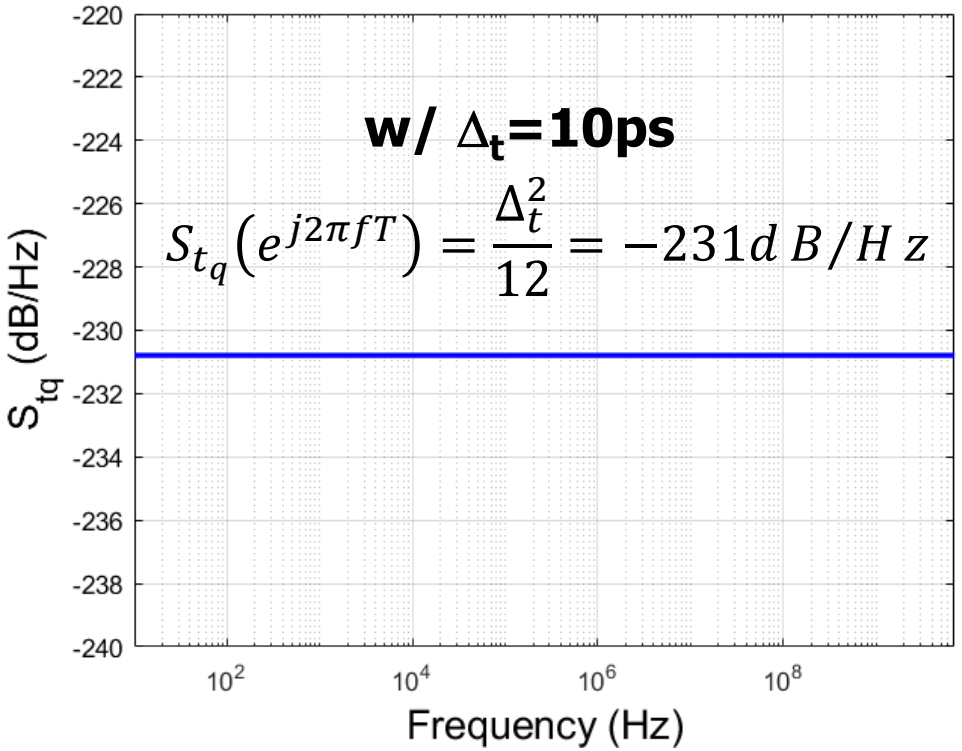


- After PLL: $\sigma_{j,in}$ = 217fs$_{rms}$ (10kHz – 10MHz)
- Including CDR: $\sigma_{j,in}$ = 46fs$_{rms}$ (100Hz – 7GHz)

TDC Quantization Noise

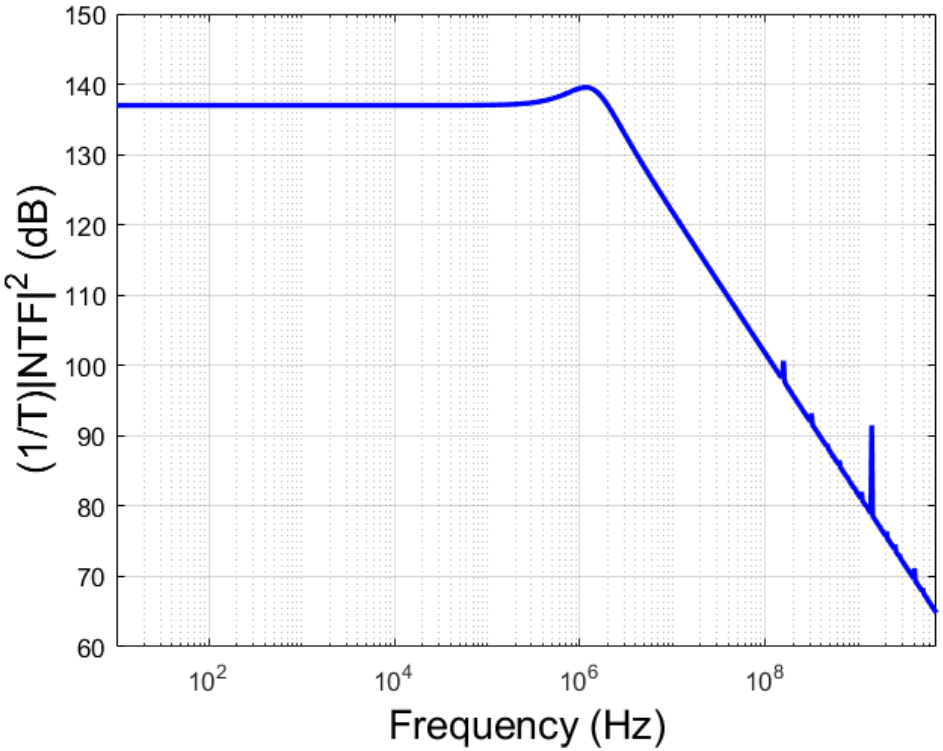


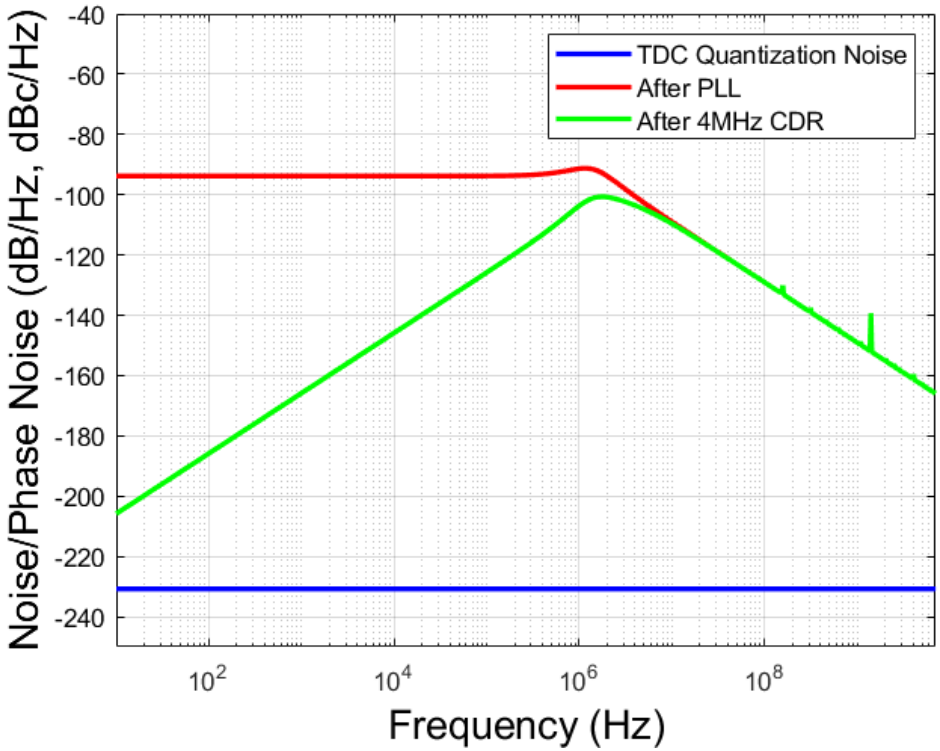
- Using the TDC output directly results in quantization noise with a uniform power spectral density



TDC Quantization Noise

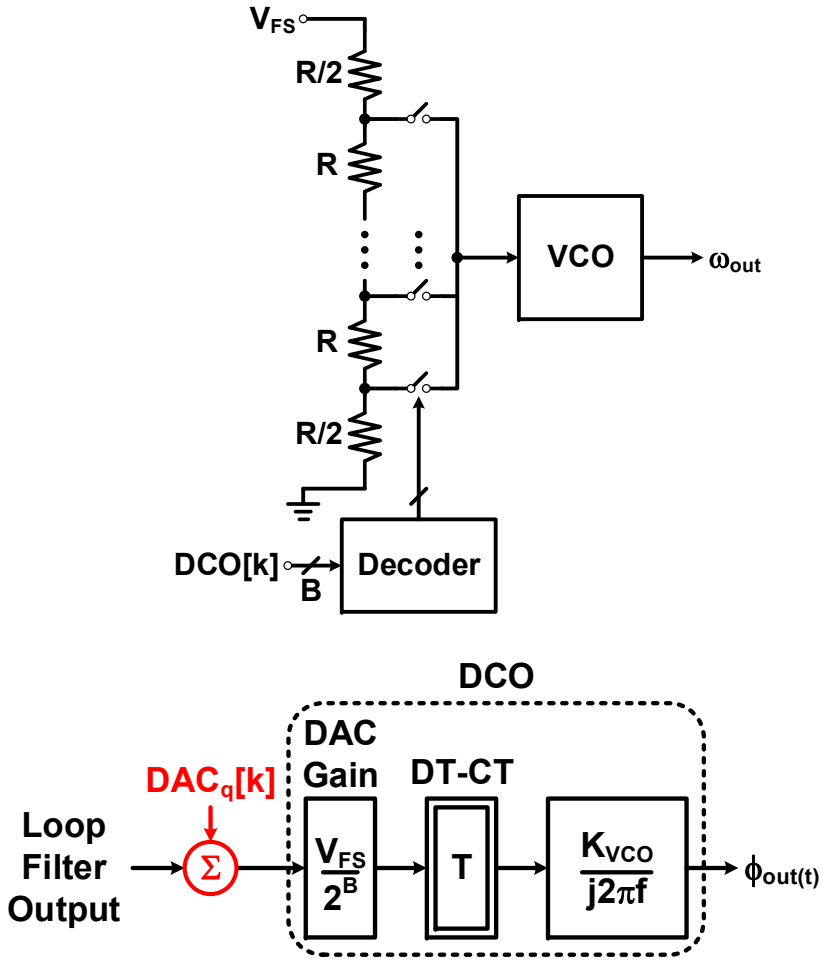
$$S_{\phi_{out}}^{t_q}(f) = S_{t_q}(e^{j2\pi fT})\left(\frac{1}{T}\right)\left|NTF_{TQ}(f)\right|^2 = S_{t_q}(e^{j2\pi fT})\left(\frac{1}{T}\right)\left|\frac{N \cdot 2\pi \cdot LG(f)}{1 + LG(f)}\right|^2$$

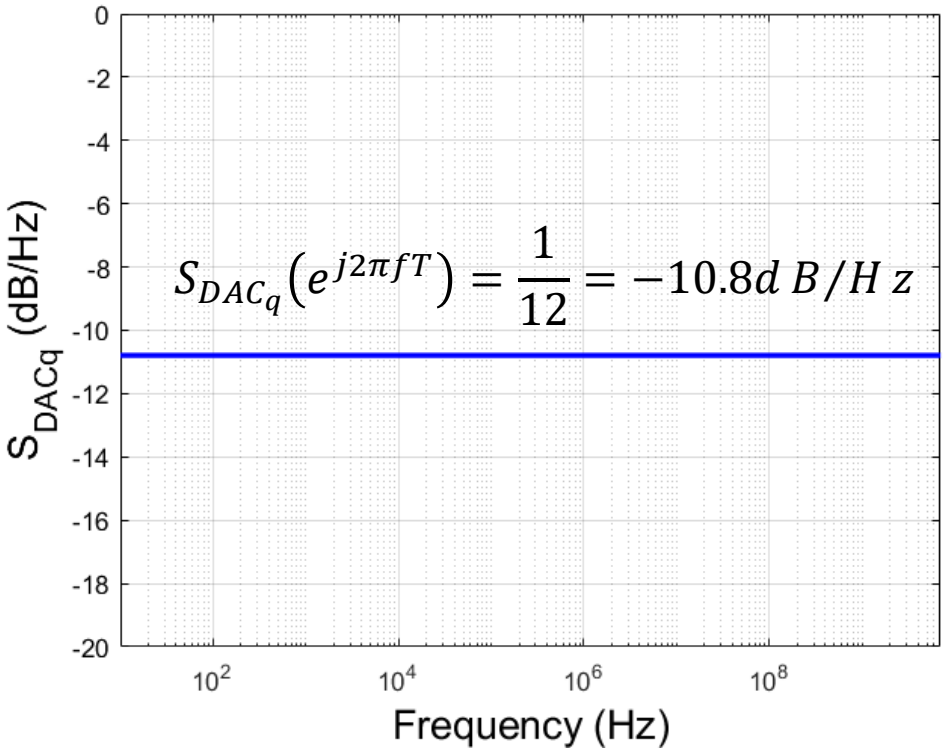




- After PLL: $\sigma_{j,tq}$ = 671fs$_{rms}$ (10kHz – 10MHz)
- Including CDR: $\sigma_{j,tq}$ = 345fs$_{rms}$ (100Hz – 7GHz)
- This is too high! Will need to increase TDC resolution.

Loop Filter DAC Quantization Noise

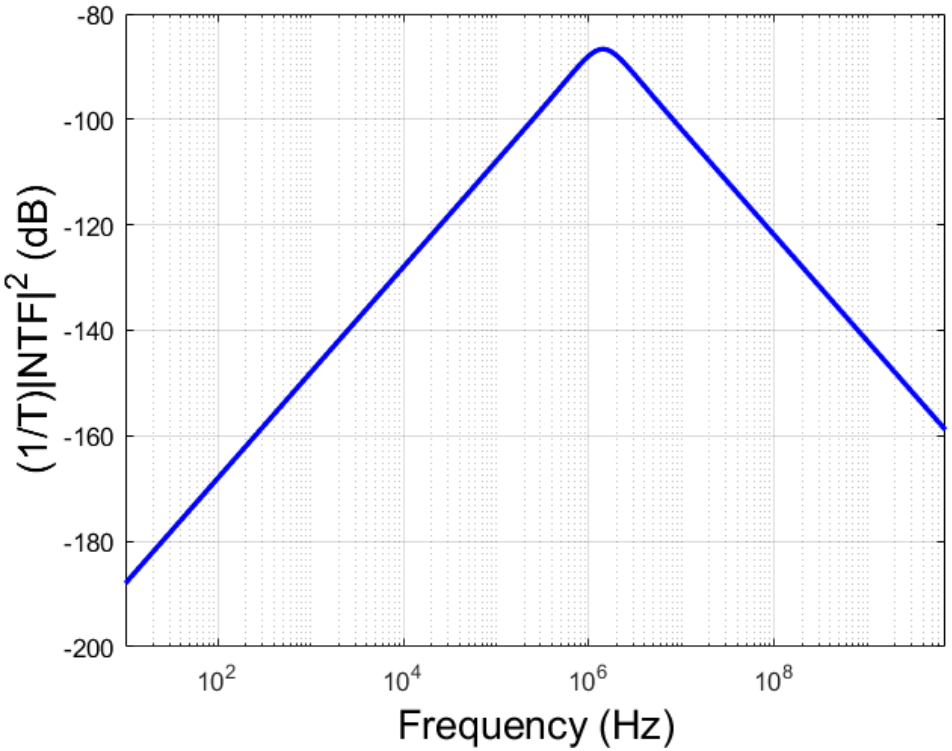


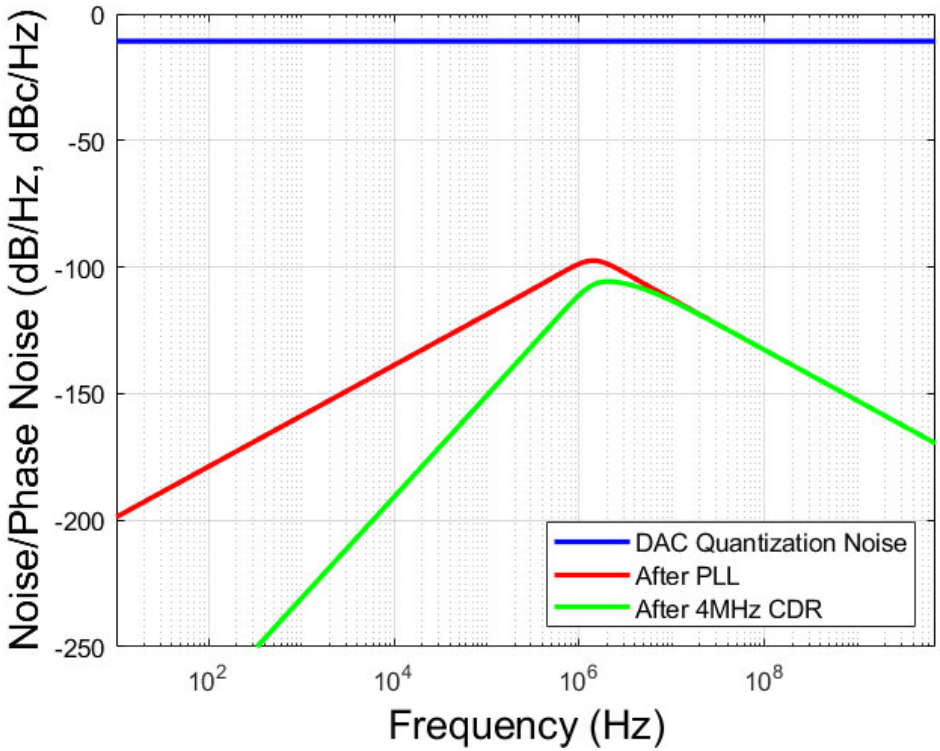


- Truncating the digital filter output at a certain resolution and applying it to the DAC results in quantization noise with a uniform power spectral density

Loop Filter DAC Quantization Noise

$$S_{\phi_{out}}^{DAC_q}(f) = S_{DAC_q}(e^{j2\pi fT})\left(\frac{1}{T}\right)\left|NTF_{DACQ}(f)\right|^2 = S_{DAC_q}\left(e^{j2\pi fT}\right)\left(\frac{1}{T}\right)\left|\frac{T\left(\frac{K_{VCO}}{j2\pi f}\right)}{1+LG(f)}\right|^2$$

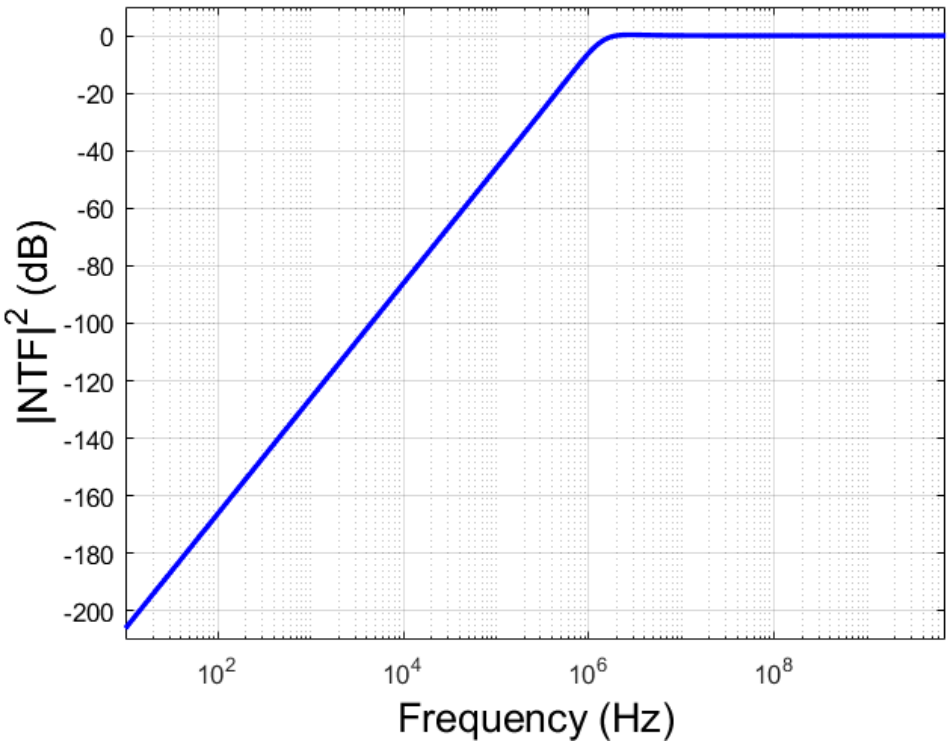


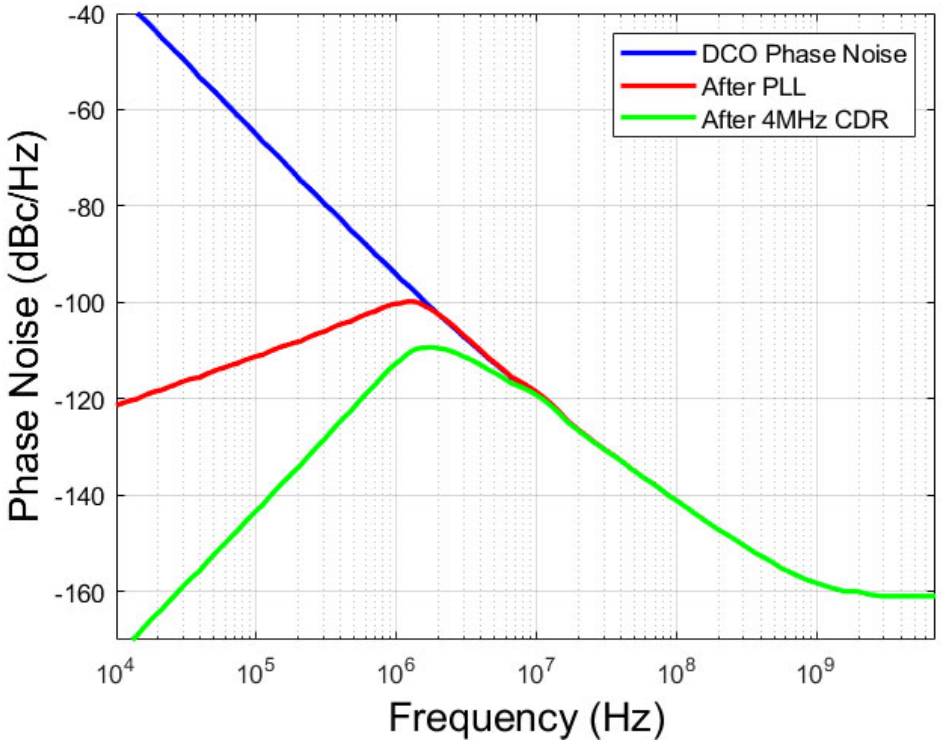


- After PLL: $\sigma_{j,DACq}$ = 332fs$_{rms}$ (10kHz – 10MHz)
- Including CDR: $\sigma_{j,DACq}$ = 211fs$_{rms}$ (100Hz – 7GHz)
- This is too high! Will need to increase DAC resolution.

DCO Noise

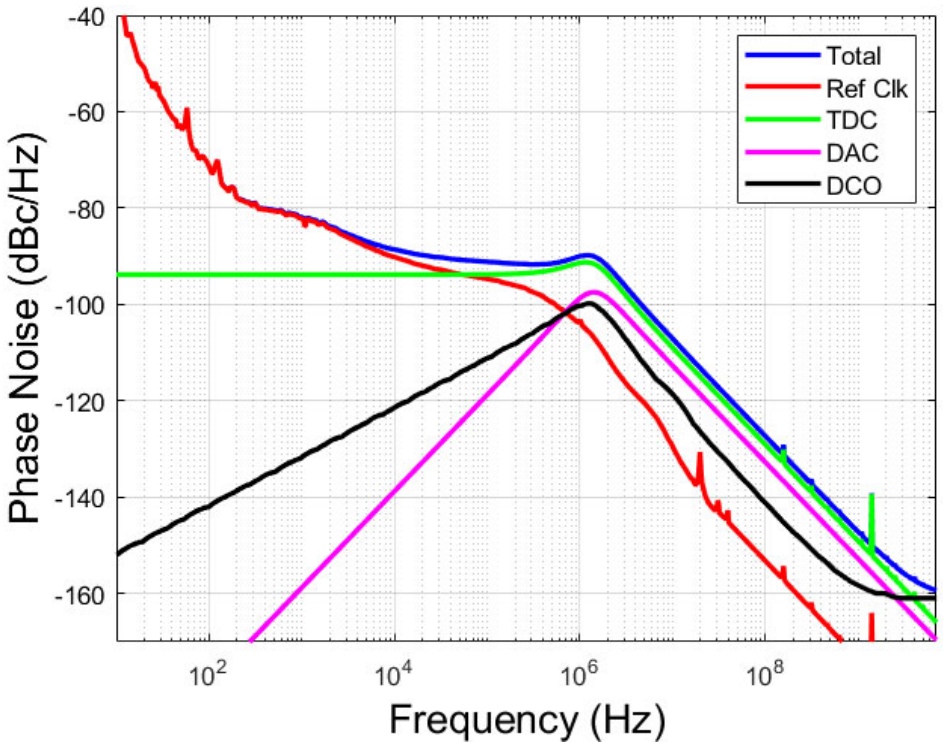
$$S_{\phi_{out}}^{\phi_{DCO}}(f) = S_{\phi_{DCO}}(f)|NTF_{VCO}(f)|^2 = S_{\phi_{DCO}}(f)\left|\frac{1}{1+LG(f)}\right|^2$$

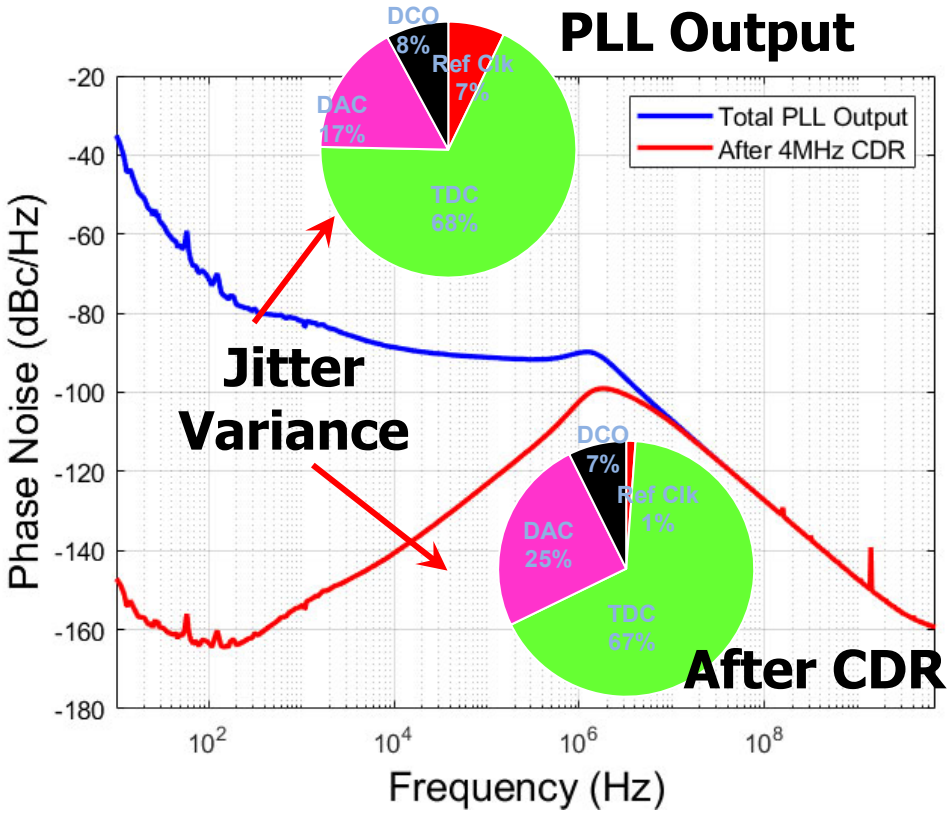




- After PLL: $\sigma_{j,in}$ = 228fs$_{rms}$ (10kHz – 10MHz)
- Including CDR: $\sigma_{j,in}$ = 115fs$_{rms}$ (100Hz – 7GHz)

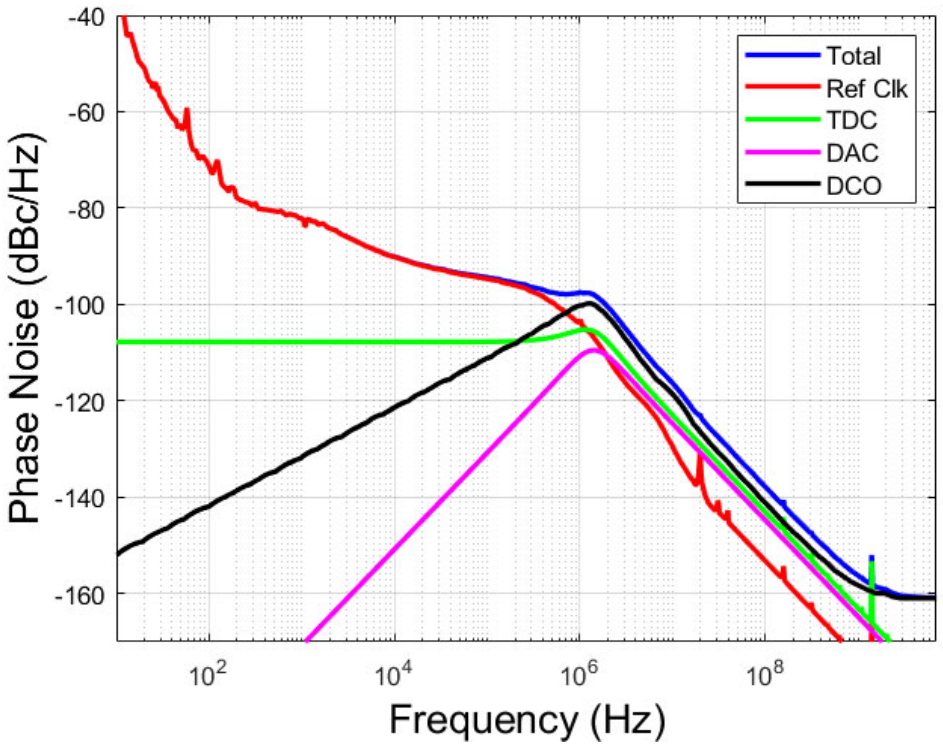
Total Noise

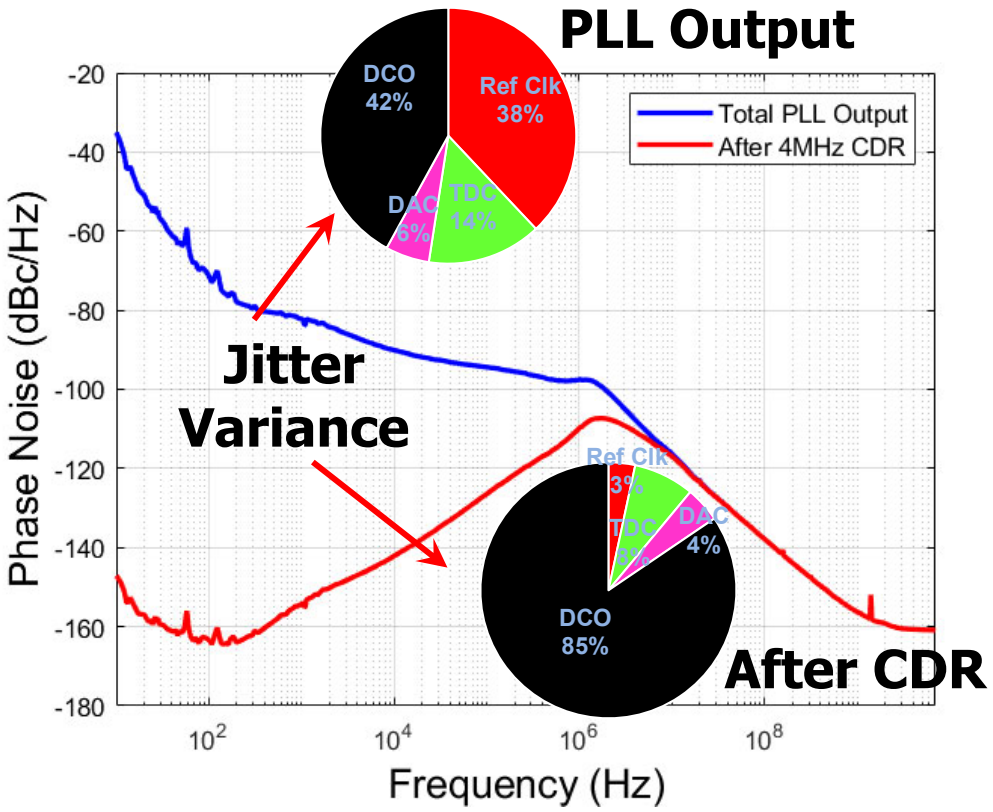




- After PLL: $\sigma_{j,Total} = 842fs_{rms}$ (10kHz – 10MHz)
- Including CDR: $\sigma_{j,Total} = 423fs_{rms}$ (100Hz – 7GHz)
  - TDC quantization noise dominates over much of the spectrum
  - Loop filter DAC quantization noise is also significant
  - Higher effective resolution TDC & DAC is necessary!

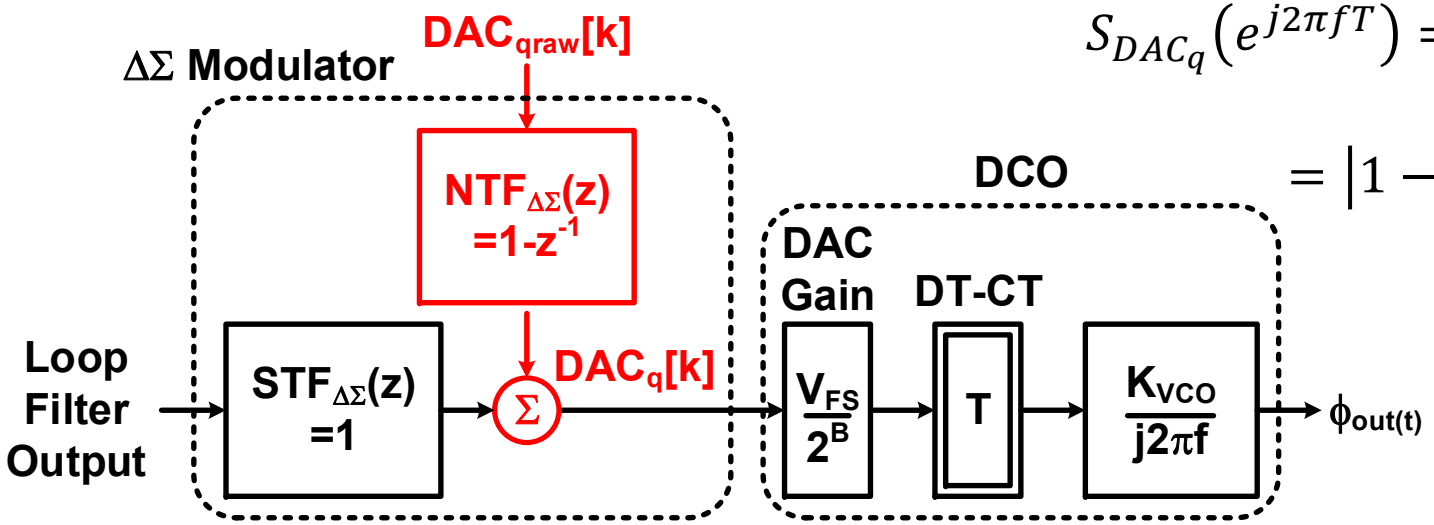
Increase TDC & DAC Resolution





- Increase resolution: TDC Δ_t=2ps & $(V_{FS}/2^B)K_{VCO}$=250kHz (12b)
- After PLL: $\sigma_{j,Total}$ = 353fs$_{rms}$ (10kHz – 10MHz)
  - Reference clock noise dominates at low frequency
  - DCO dominates near loop bandwidth and higher
- Including CDR: $\sigma_{j,Total}$ = 151fs$_{rms}$ (100Hz – 7GHz)
  - Now DCO noise clearly dominates total

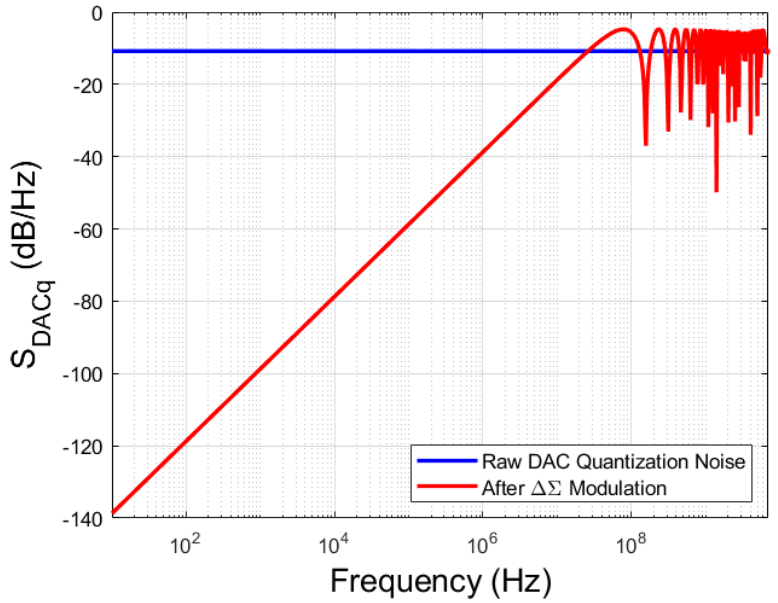
Delta Sigma Modulation



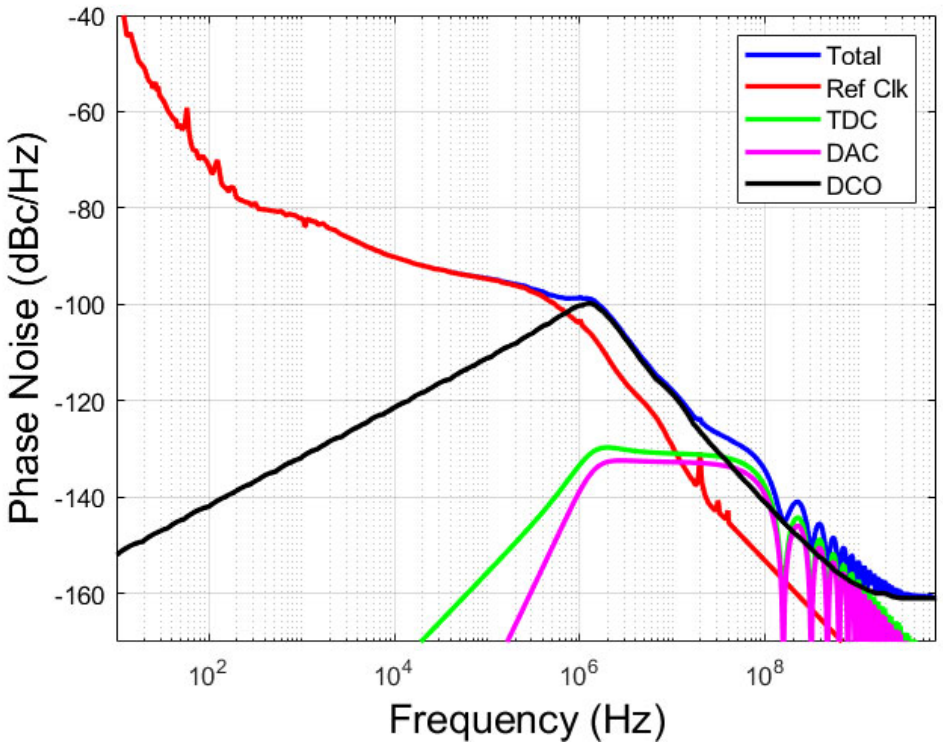
$$S_{DAC_q}\left(e^{j2\pi fT}\right) = \left|NTF_{\Delta\Sigma}\left(e^{j2\pi fT}\right)\right|^2 \left(\frac{1}{12}\right)$$

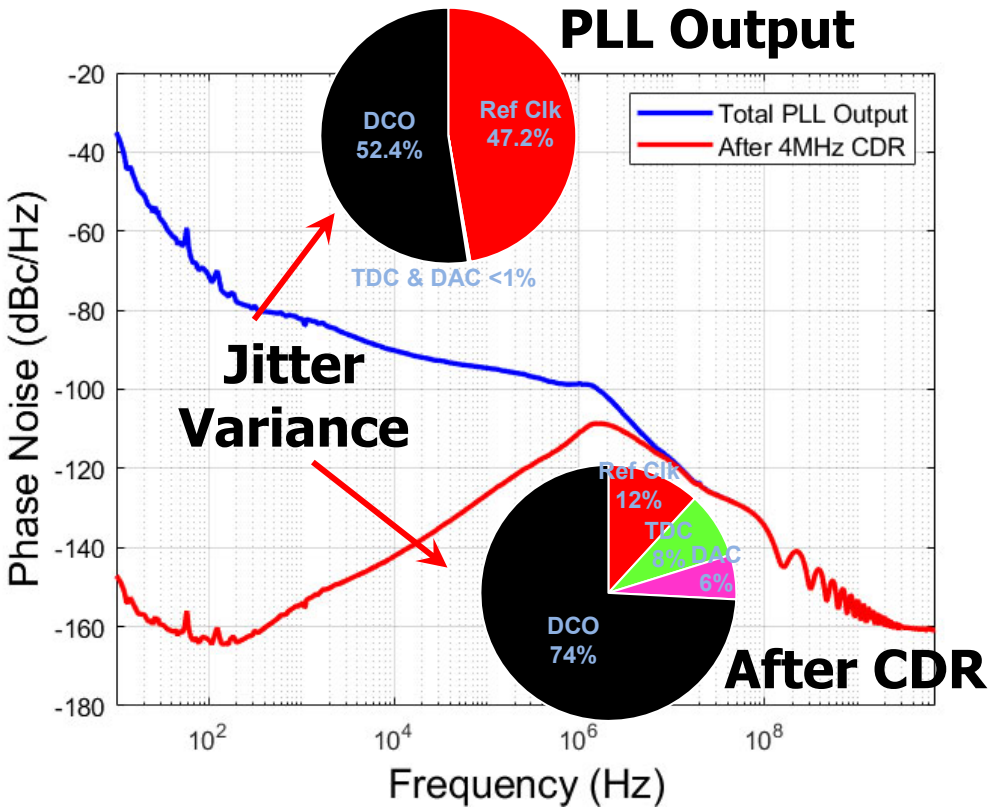
$$= \left|1 - e^{-j2\pi fT}\right|^2 \left(\frac{1}{12}\right)$$

- DS modulation provides high-pass quantization noise shaping to dramatically reduce low-frequency content



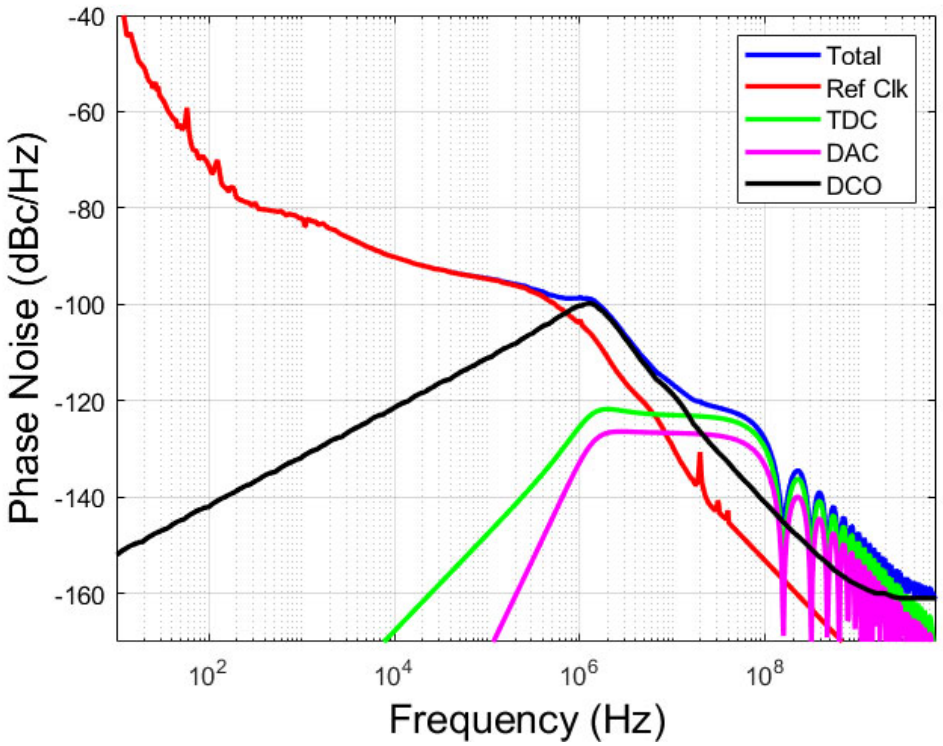
With Delta-Sigma Modulation

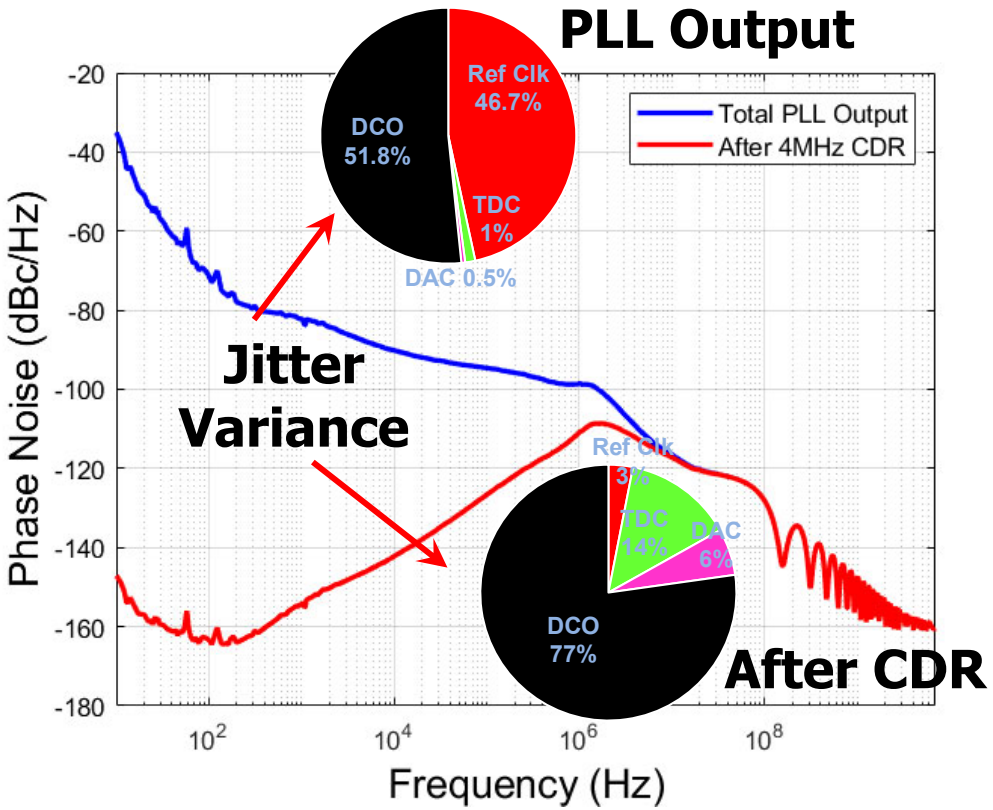




- Add $\Delta\Sigma$ modulation to TDC Δ_t=2ps & $(V_{FS}/2^B)K_{VCO}$=250kHz (12b)
- After PLL: $\sigma_{j,Total}$ = 316fs$_{rms}$ (10kHz – 10MHz)
  - Reference clock noise dominates at low frequency
  - DCO dominates near loop bandwidth and higher
- Including CDR: $\sigma_{j,Total}$ = 133fs$_{rms}$ (100Hz – 7GHz)
  - Now DCO noise clearly dominates total
  - Some contribution from TDC & DAC at high frequency

With Delta-Sigma Modulation & Relaxed TDC & DAC



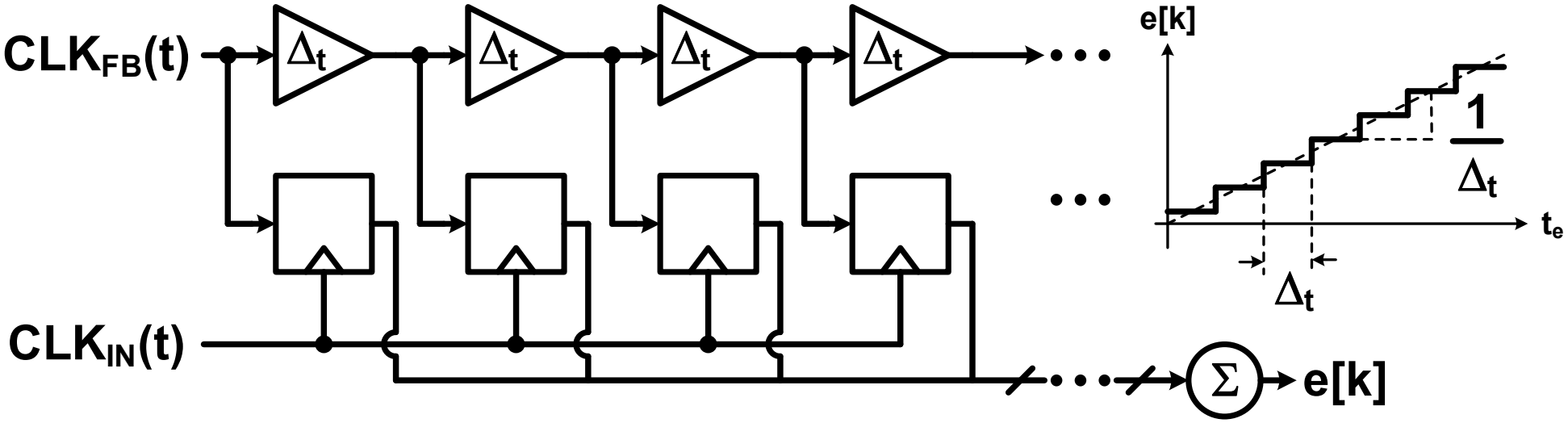


- Include $\Delta\Sigma$ modulation with relaxed TDC Δ_t=5ps & $(V_{FS}/2^B)K_{VCO}$=500kHz (11b)
- After PLL: $\sigma_{j,Total}$ = 318fs$_{rms}$ (10kHz – 10MHz)
  - Reference clock noise dominates at low frequency
  - DCO dominates near loop bandwidth and higher
- Including CDR: $\sigma_{j,Total}$ = 169fs$_{rms}$ (100Hz – 7GHz)
  - Now DCO noise clearly dominates total
  - Increased contribution from TDC & DAC at high frequency could be reduced with additional passive filter after DAC and/or operating $\Delta\Sigma$ with higher frequency clock

Agenda

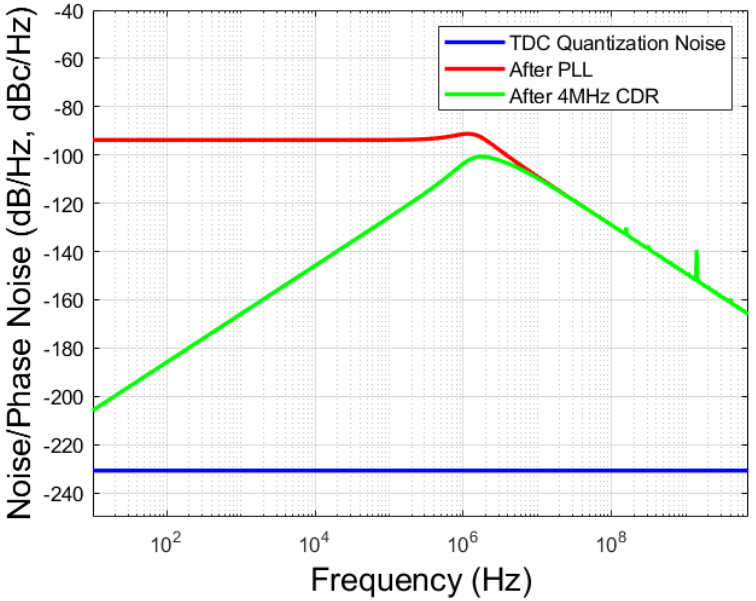
- Digital PLL Overview
- Linear Model
- Design Procedure
- Noise Analysis
- Time-to-Digital Converters
- Conclusion

Flash TDC

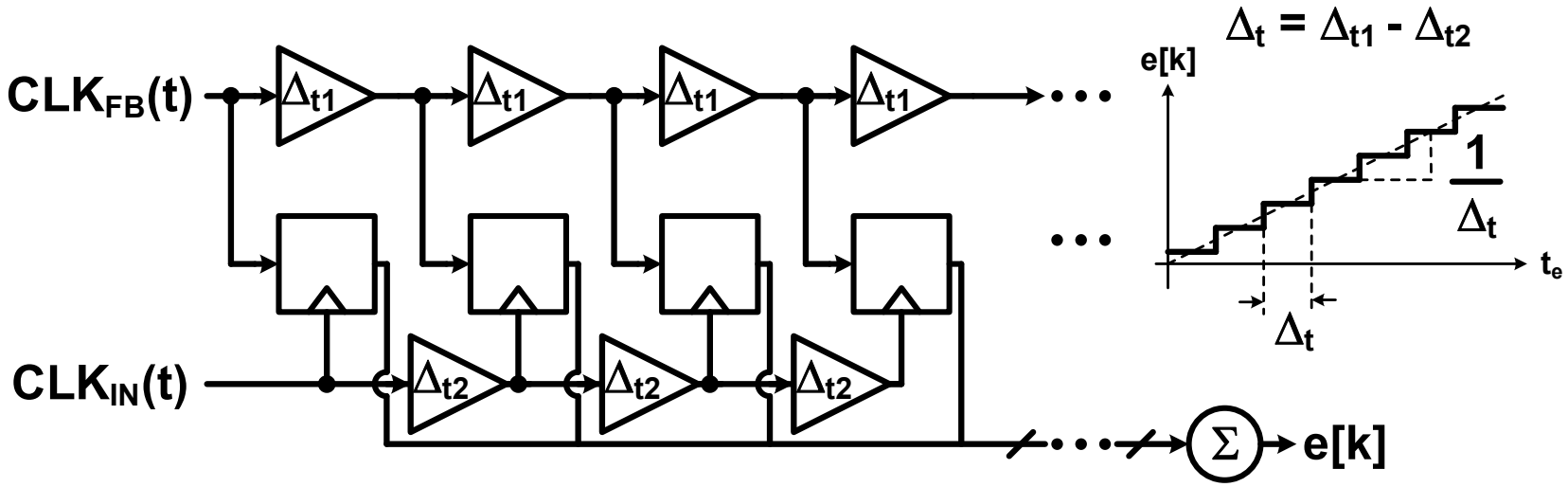


- Flash TDC converts the time difference between the input and feedback clocks to a digital code at a resolution Δ_t with a single delay chain

- Unit cell delay limits TDC resolution and can introduce significant quantization noise



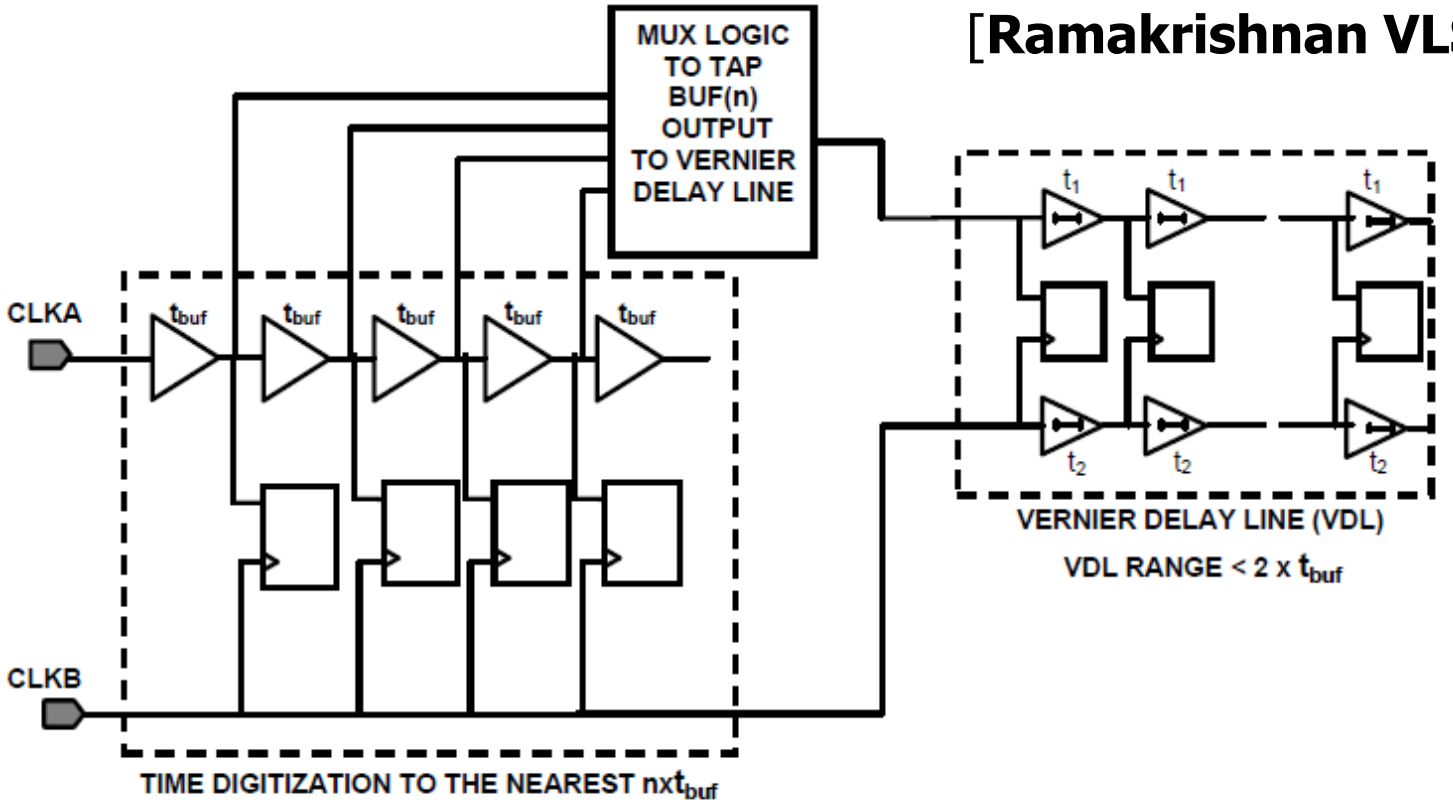
Vernier TDC



- Both inputs pass through different delay lines
- Increases TDC resolution to Δ_{t1}-Δ_{t2}
- Sensitive to mismatch between the two delay lines
- Delay stage count scales with increased resolution to cover a given full scale range

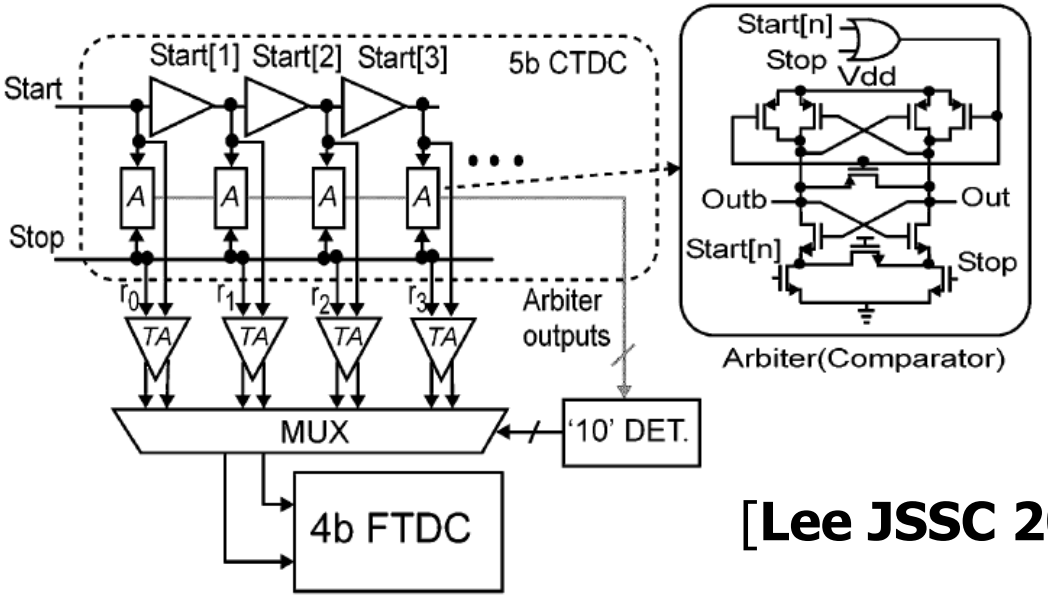
Two-Step TDC

[**Ramakrishnan VLSID 2006**]

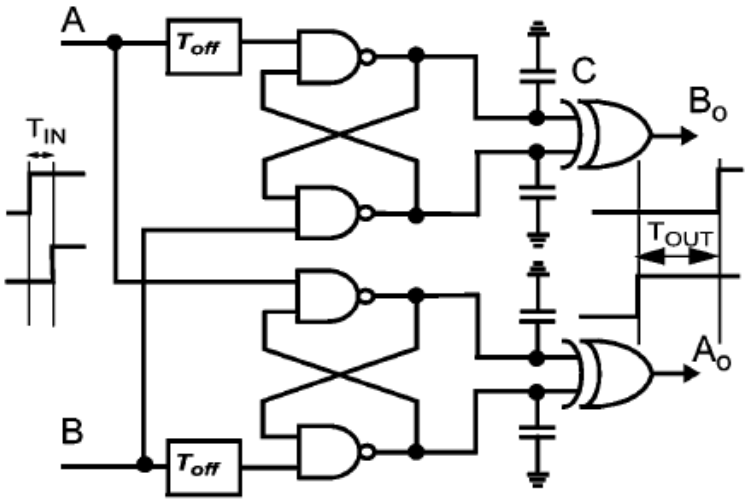


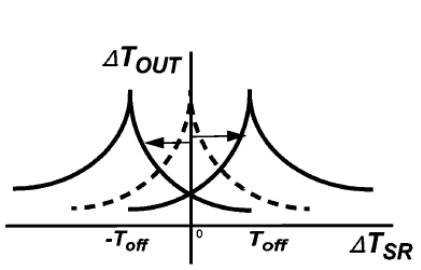
- Coarse conversion with input flash TDC
- Time residue transferred to Vernier TDC for fine conversion
- Allows for Vernier resolution with reduced area for a given full scale range

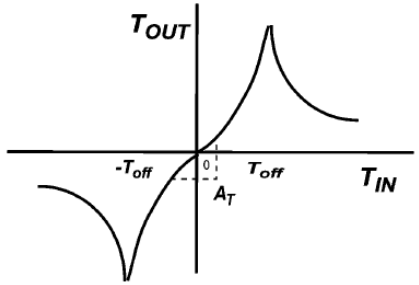
Two-Step TDC w/ Time Amplification



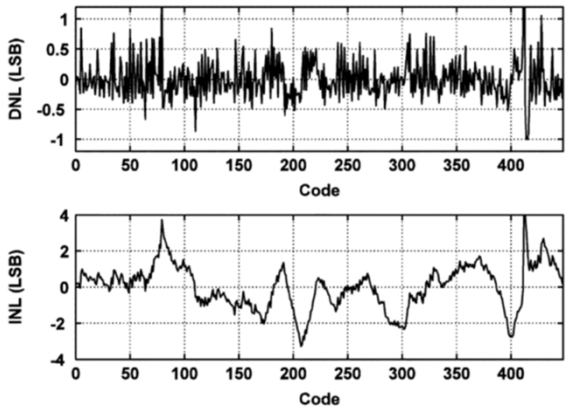
[**Lee JSSC 2008**]







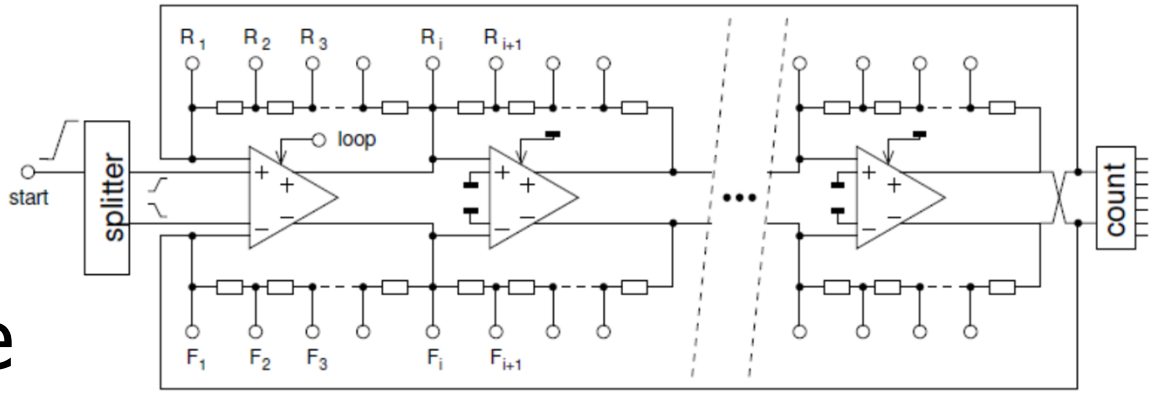
- Utilizes two single delay chain TDCs with a time amplifier between stages to improve resolution
- Time amplifier is based on unbalanced SR latches
- Achieves 1.25ps LSB in 90nm

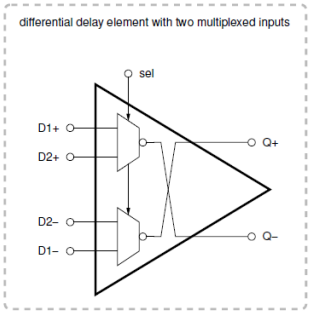


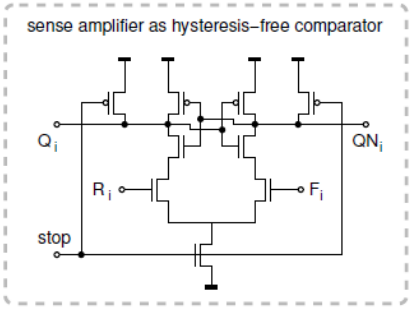
Interpolating TDC

- Interpolation with passive resistors provides a simple technique to increase TDC resolution
- Delay line output is cycled through the loop to increase conversion range

[**Henzler ISSCC 2008**]





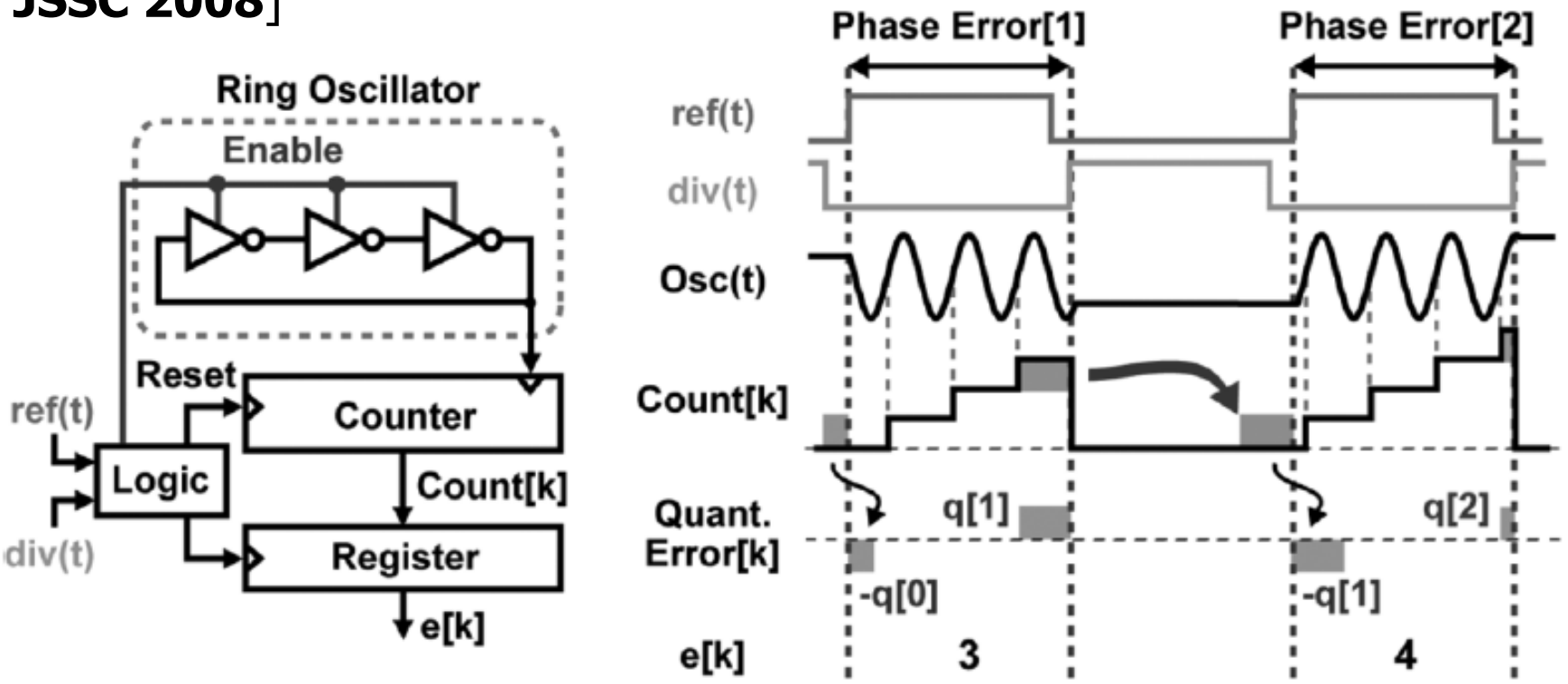


ref.	technique	tech. [nm]	resol. [ps]	single shot precision	INL [LSB]	INL [ps]	DNL [LSB]	DNL [ps]	power [1]	area [mm²]	variation robustness
[1]	delay line	90	20.0		0.7	14.0	0.6	12.0	157	0.01	++
[2]	vernier	700	30.0	0.7 LSB	1.3	39.0				10	+
[3]	pulse shrinking	350	68.0	0.8 LSB					1102	0.03	–
[4]	parallel del. elements	350	12.2		1.6	19.5			735	7.5	—
[5]	delay amplification	90	1.25		3.0	3.7	0.8	1.0	300	0.6	––
[6]	scrambling	130								0.02	
this	loc. passive interpol.	90	4.7	0.7 LSB	1.2	5.6	0.6	2.8	14	0.02	++

[1] normalized power defined by (1MHz x P)/(V_{DD}^2 x f)

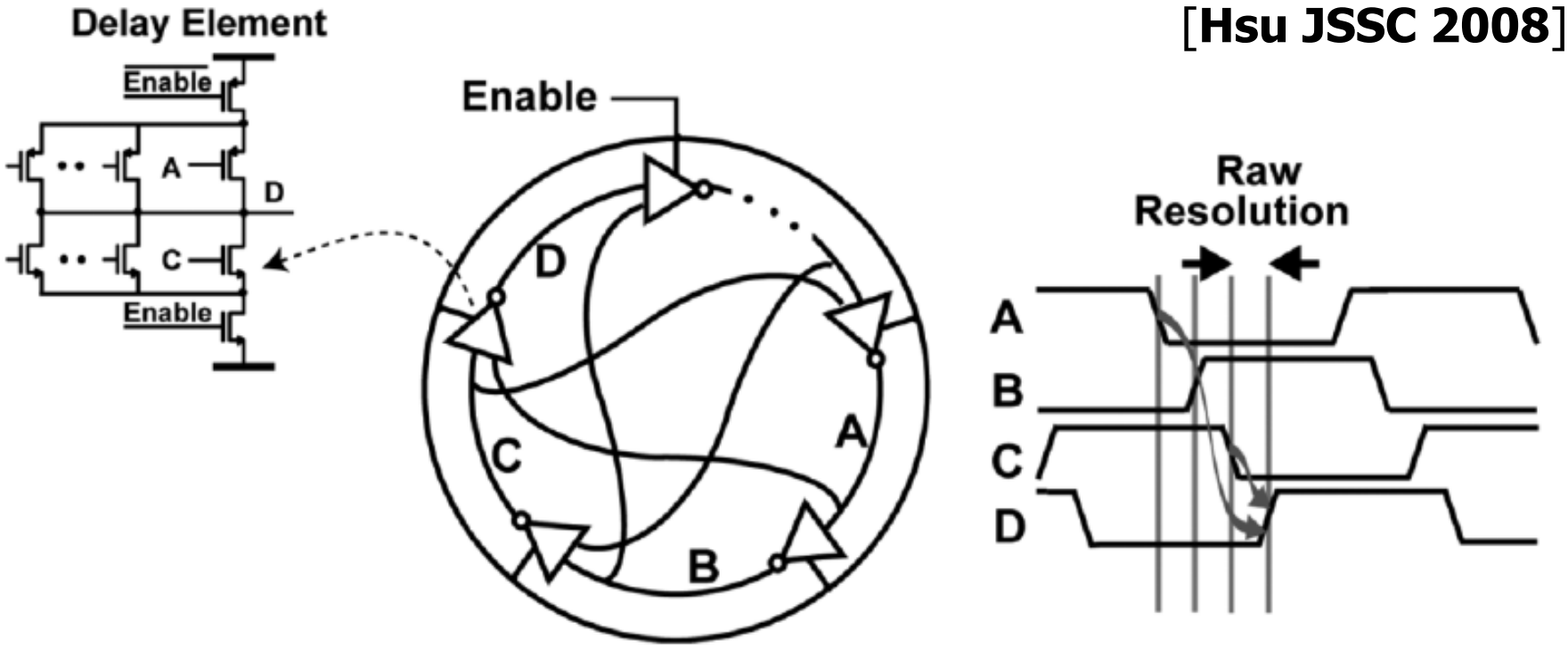
Oscillator-Based TDC

[**Hsu JSSC 2008**]



- Gated ring oscillator (GRO) is enabled between rising edges of the two input clocks
- Counting the oscillator transitions performs the conversion
- The GRO retains internal state between measurements, providing first-order quantization noise shaping

Oscillator-Based TDC



[**Hsu JSSC 2008**]

- All transitions of the oscillator's multiple phases can be counted to increase resolution
- Resolution is further increased with a multipath ring oscillator
- Achieves 6ps resolution in 0.13um

Conclusion

- Digital PLLs can eliminate analog charge pump non-idealities and allow for lower-area loop filters
- Key blocks are the input TDC, digital PI loop filter, and DCO
- Quantization noise is introduced by the TDC and loop filter DAC/DCO
- Advanced TDC architectures can achieve sub-inverter delay resolution

Next Time

- Fractional-N Frequency Synthesizers