ECEN620: Network Theory Broadband Circuit Design Fall 2023

Lecture 5: Charge Pump Circuits

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Announcements

- HW2 due Oct 3
  - Requires transistor-level design
  - For 90nm CMOS device models, see https://people.engr.tamu.edu/spalermo/ecen689/cadence_90nm_2023.pdf
  - Can use other technology models if they are a 90nm or more advanced CMOS node

Agenda

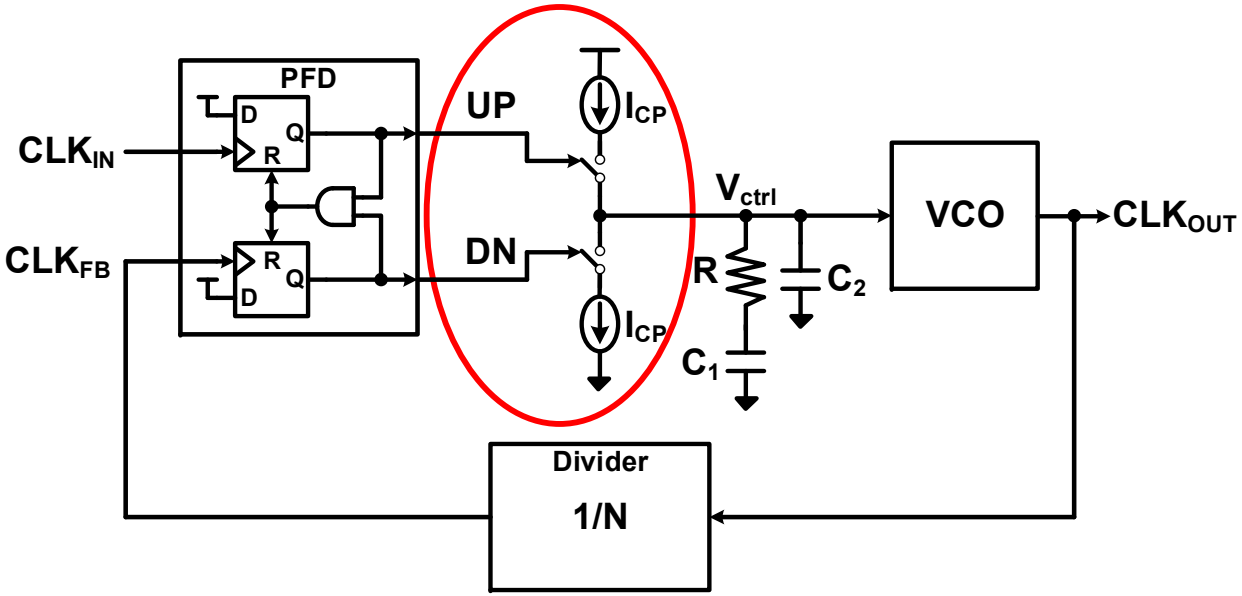
- Charge pump circuits
  - Basic operation
  - Techniques to improve static and dynamic current source matching

References

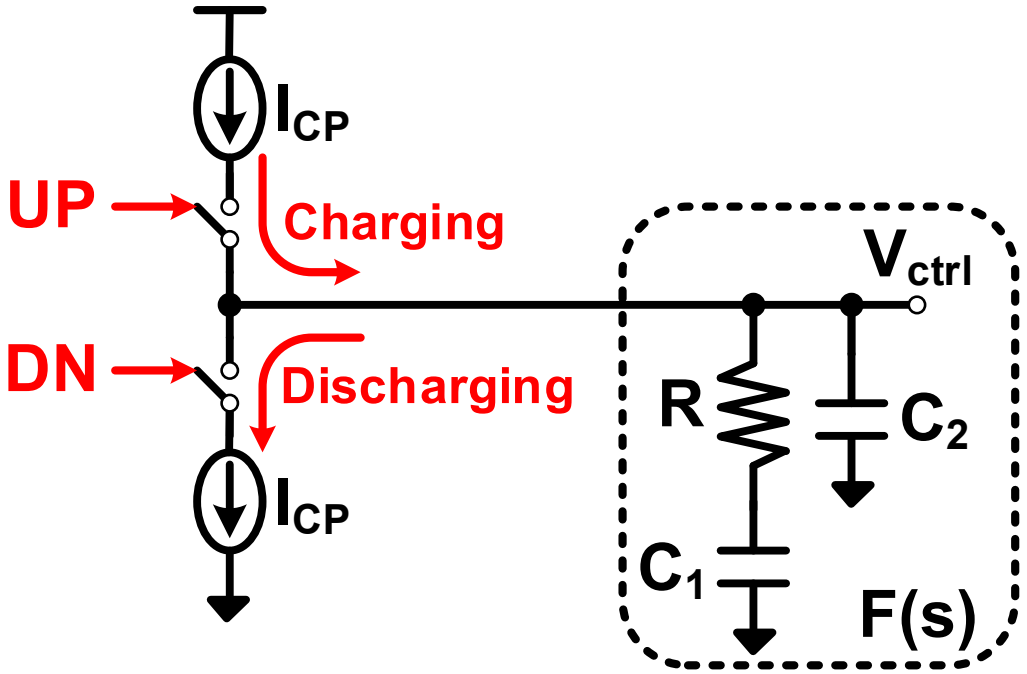
- *Design of Integrated Circuits for Optical Communications,* B. Razavi, McGraw-Hill, 2003.
- *First Time, Every Time – Practical Tips for Phase-Locked Loop Design,* D. Fischette, IEEE Tutorial, 2009.
- PLL/charge-pump papers posted on the website

Analog Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider



Charge Pump



- Converts PFD output signals to charge
- Charge is proportional to PFD pulse widths

$$\text{Un - Averaged Charge - Pump Gain} = I_{CP} \ \left(\text{Amps}\right)$$

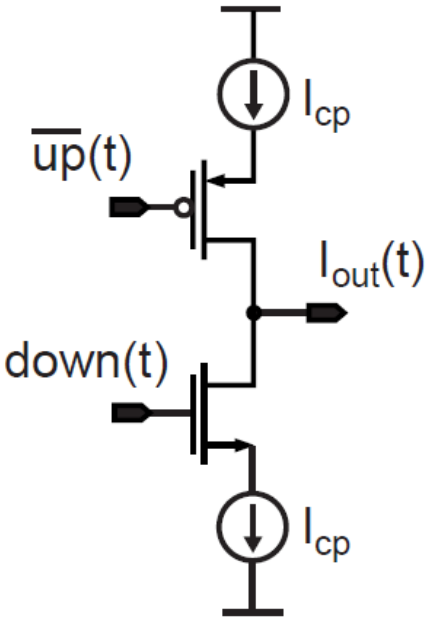
$$\text{Averaged Charge - Pump Gain} = \frac{I_{CP}}{2\pi} \left(\frac{\text{Amps}}{\text{rad}}\right)$$

$$\text{Total PFD \& Charge - Pump Gain} = \frac{I_{CP}}{2\pi} \left(\frac{\text{Amps}}{\text{rad}}\right)$$

This gain can vary if a different phase detector is used

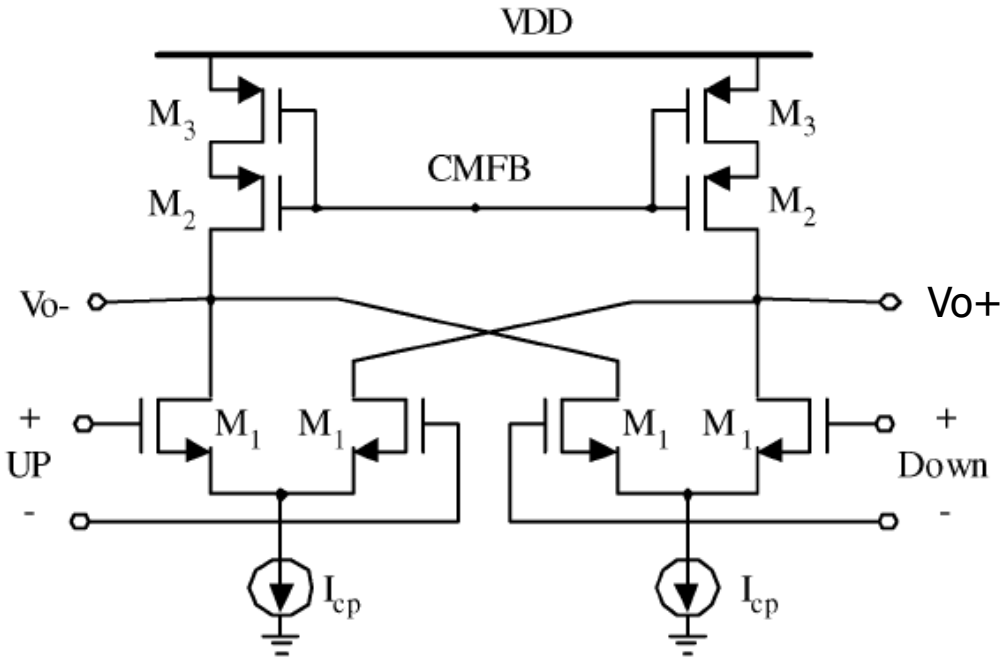
Charge Pump Implementations

Single-Ended



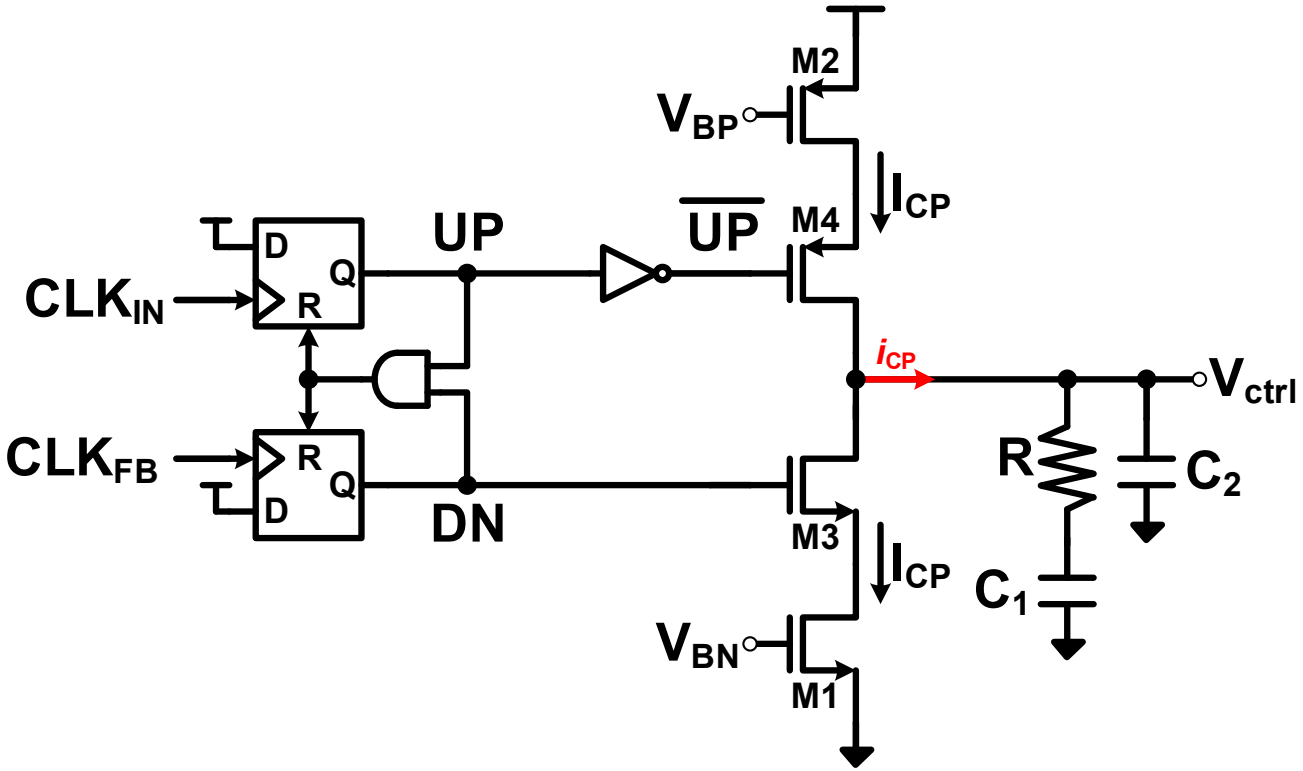
[**Perrott**]

Fully Differential



[**Li TCAS1 2008**]

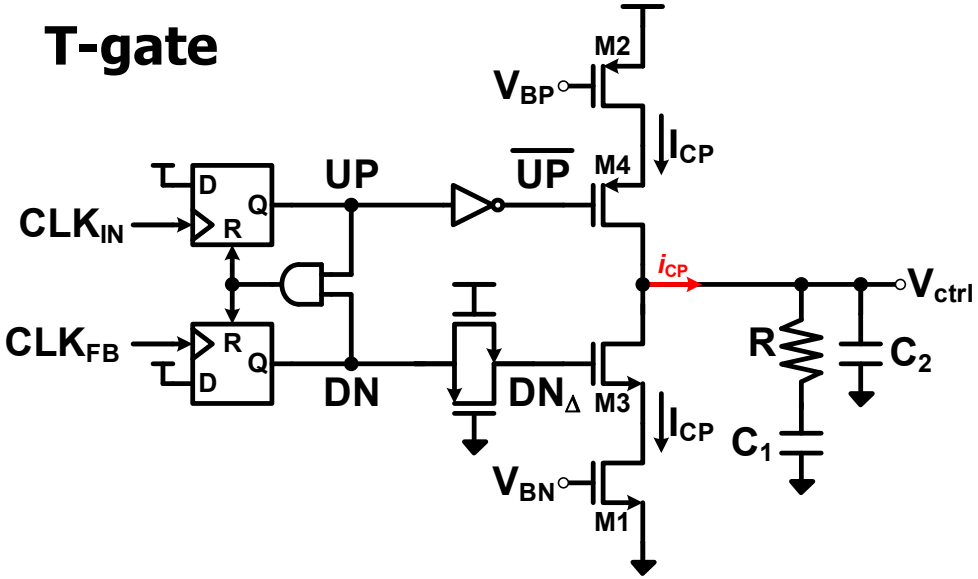
Simple Charge Pump



- Issues
  - Skew between UPB and DN control signals
  - Matching of UP/DN current sources
  - Clock feedthrough and charge injection from switches onto V_{ctrl}
  - Charge sharing between current source drain nodes' capacitance and V_{ctrl}

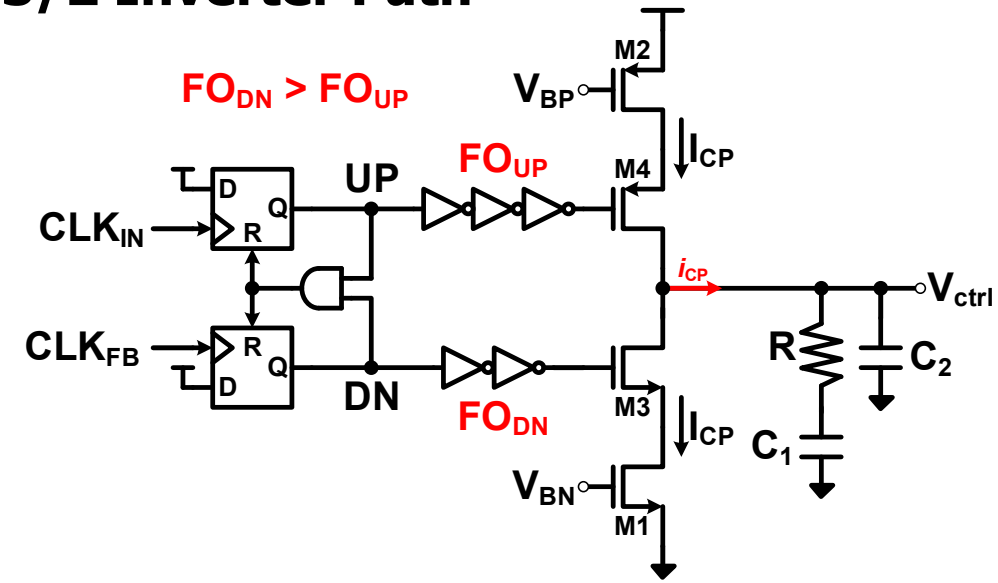
Simple Charge Pump Skew Compensation

T-gate



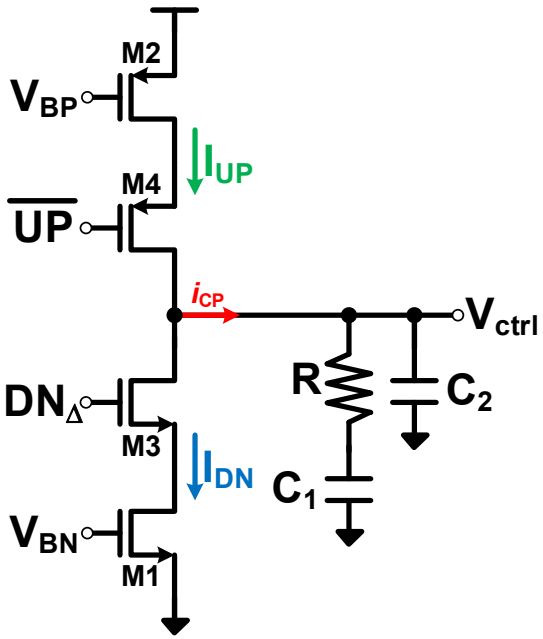
- Adding a transmission gate in the DN signal path helps to equalize the delay with the UPB signal for better overlap between the UP and DN current sources
- Poor matching of UPB and DN_Δ edge rates

3/2 Inverter Path

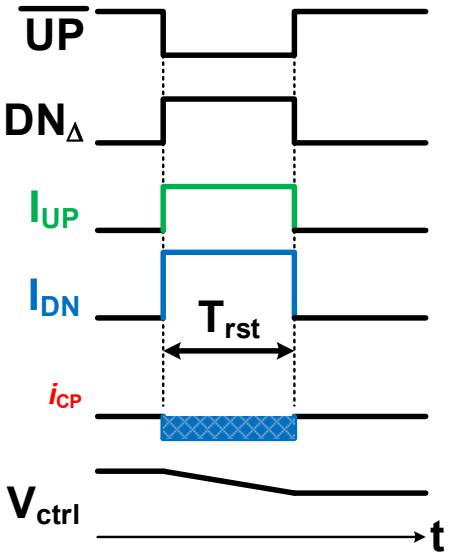


- Utilizing a 3-inverter UP path and a 2-inverter DN path with a higher fanout provides good matching of both delay and edge rates

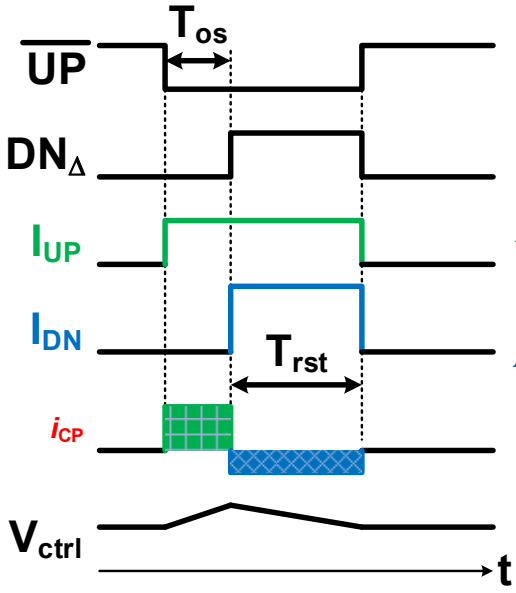
Charge Pump Mismatch



Ideal locked condition, but CP mismatch



Actual locked condition w/ CP mismatch



$$I_{UP} = I_{CP} - \frac{\Delta I}{2}$$

$$I_{DN} = I_{CP} + \frac{\Delta I}{2}$$

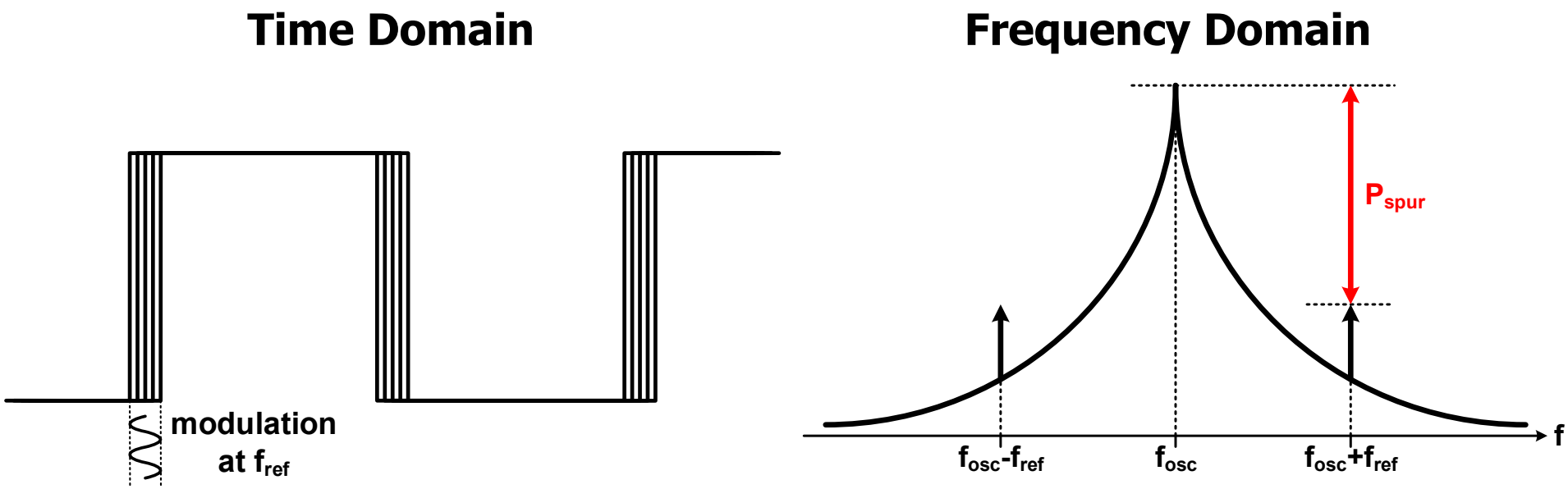
- PLL will lock with static phase error if there is a charge pump mismatch
- Extra "ripple" on V_{ctrl}
  - Results in frequency domain spurs at the reference clock frequency offset from the carrier

$$I_{UP}(T_{os}) = \Delta I(T_{rst})$$

$$T_{os} = \frac{\Delta I(T_{rst})}{I_{CP} - \frac{\Delta I}{2}}$$

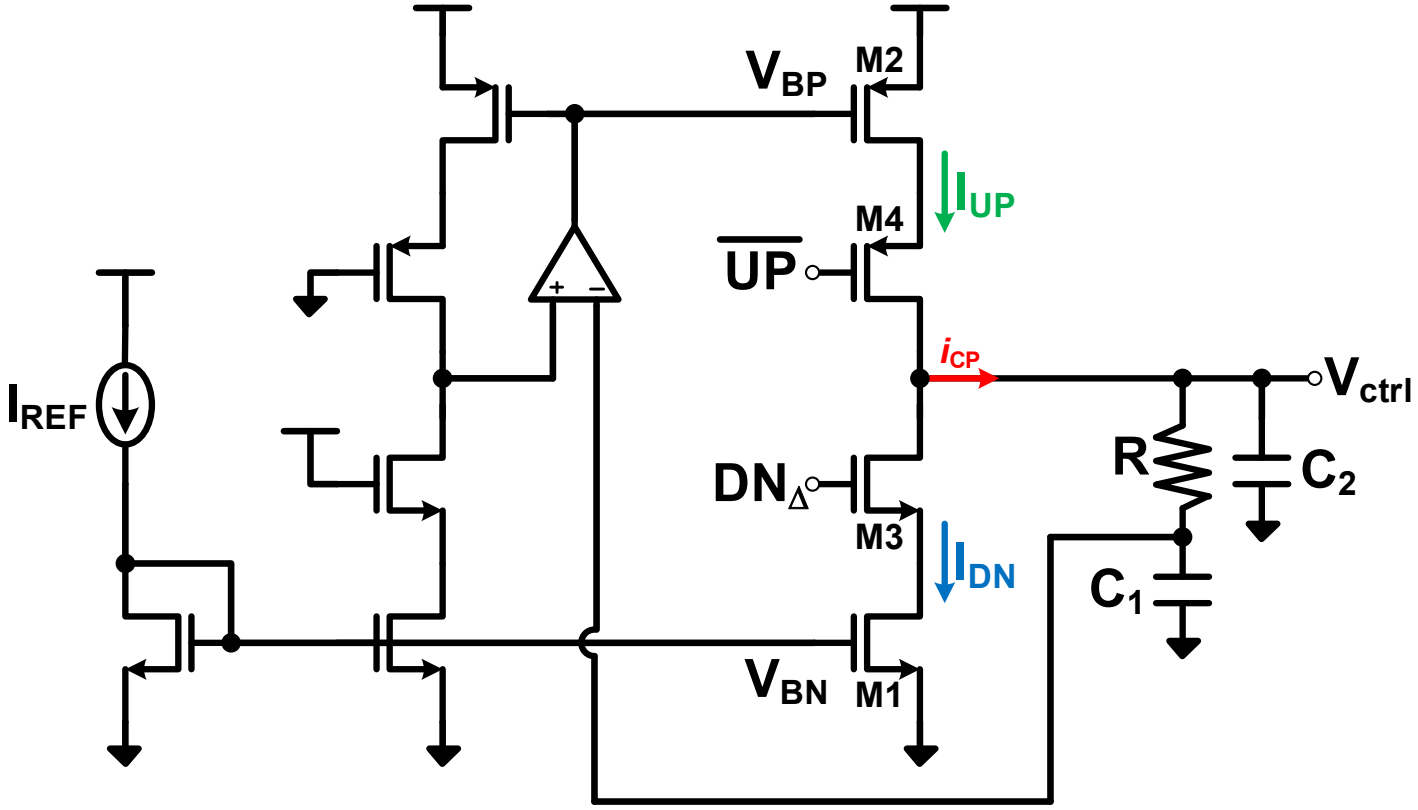
$$\phi_{os} = 2\pi \left(\frac{\Delta I}{I_{CP} - \frac{\Delta I}{2}} \right) \left(\frac{T_{rst}}{T_{ref}} \right)$$

PLL Output Spectrum w/ Spurs



- Control voltage ripple results in periodic modulation of clock frequency
- Spurs appear at $\pm f_{ref}$ relative to the carrier frequency
- In order to minimize this, it is not only important to match the DC value of $I_{UP}=I_{DN}$, but also address dynamic current mismatches
  - Charge sharing
  - Charge injection and clock feedthrough

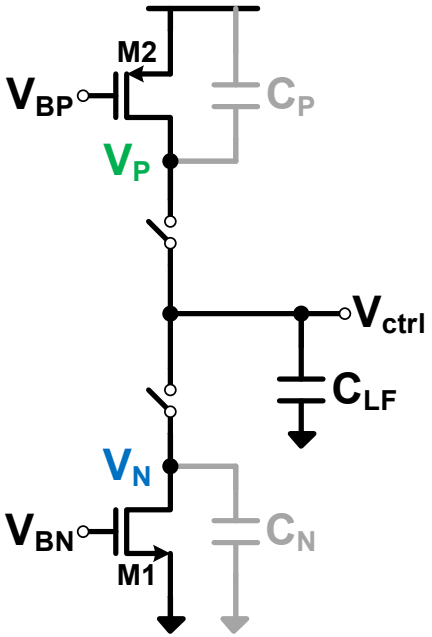
Charge Pump Feedback Biasing



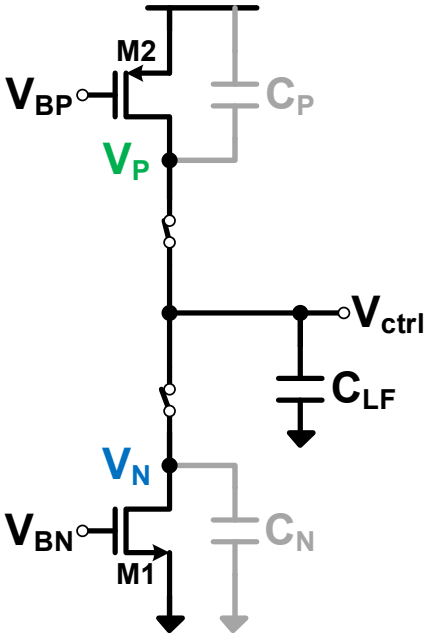
- PMOS I_{UP} current source is feedback biased to match NMOS I_{DN} current at the V_{ctrl} output level

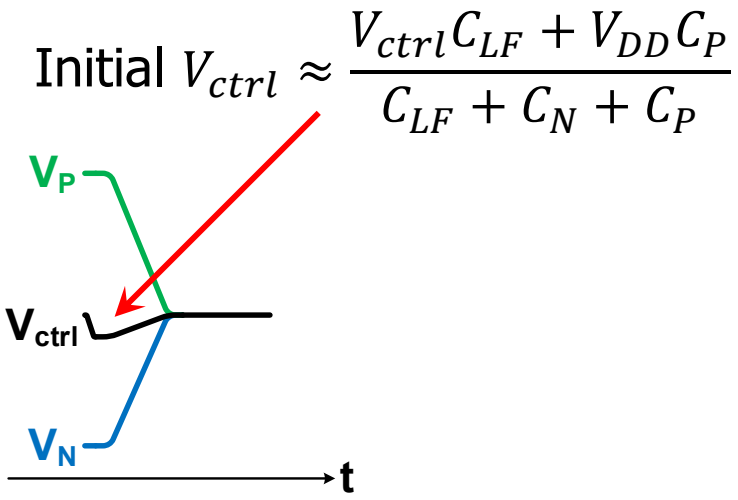
Charge Sharing on V_{ctrl}

Switches Off



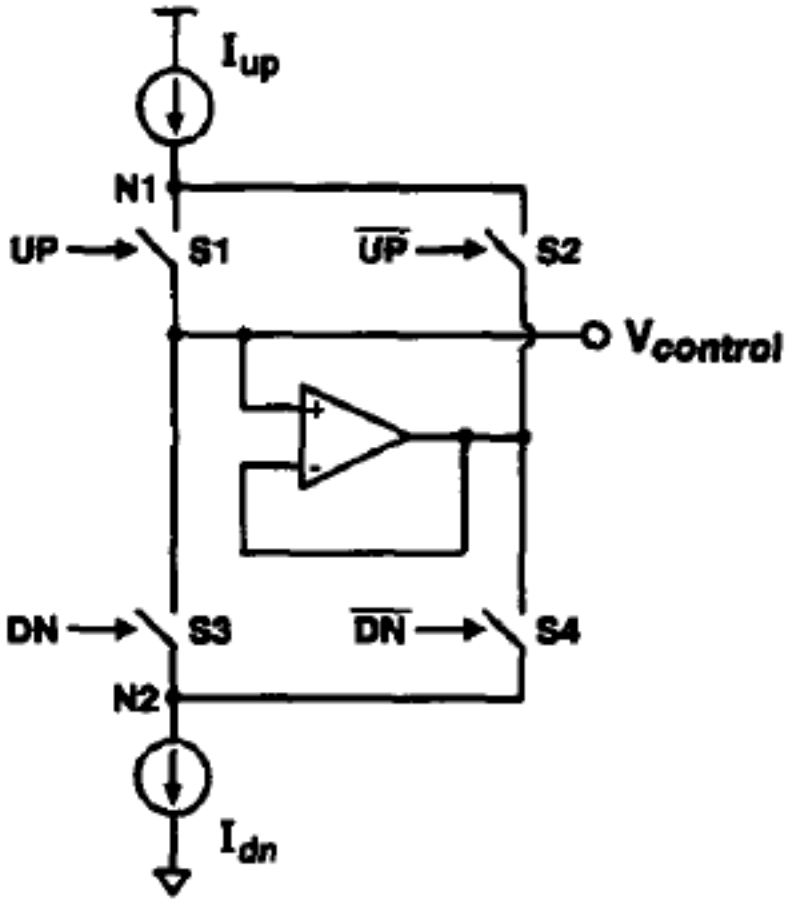
Switches On





- When switches are off, the PMOS current source drain discharges to VDD and the NMOS current source drain discharges to GND
- When switches are on, charge sharing occurs between the loop filter capacitance and these current source drain nodes, causing a level-dependent disturbance on V_{ctrl}

Charge Pump w/ Improved Matching



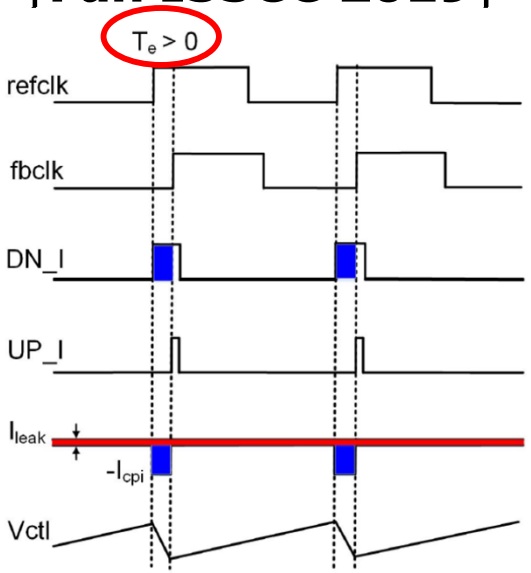
[**Young JSSC 1992**]

- Parallel path keeps current sources always on
- Amplifier keeps current source V_{DS} voltages constant resulting in reduced transient current mismatch (charge sharing)

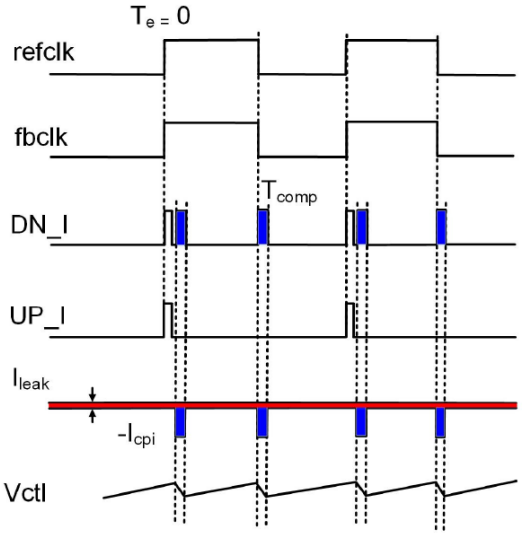
Digital Leakage Compensation

- Charge pump **off-state leakage** causes PLL to lock with static phase error
- Compensated by additional digitally-controlled charge pump current pulses
- TDC detects phase error between input reference clock and feedback clock

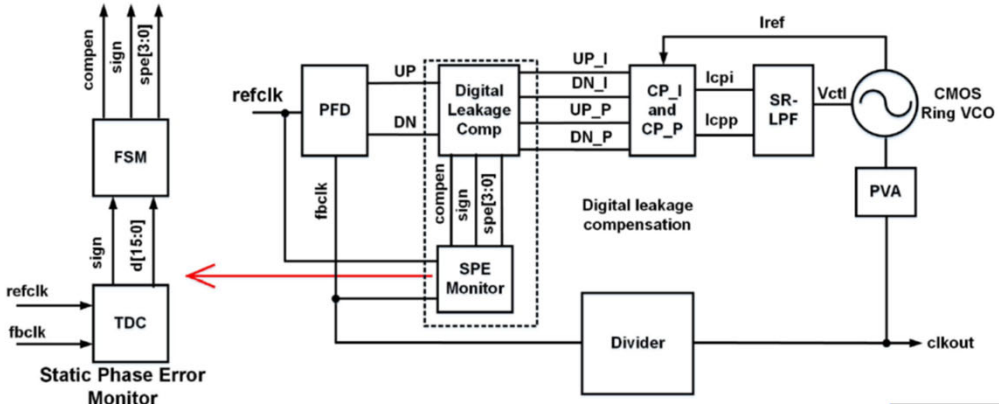
[**Fan ISSCC 2019**]

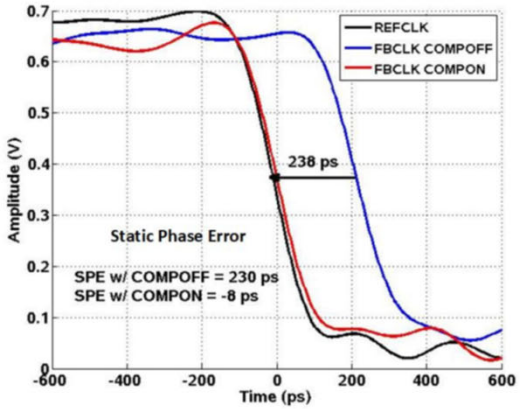


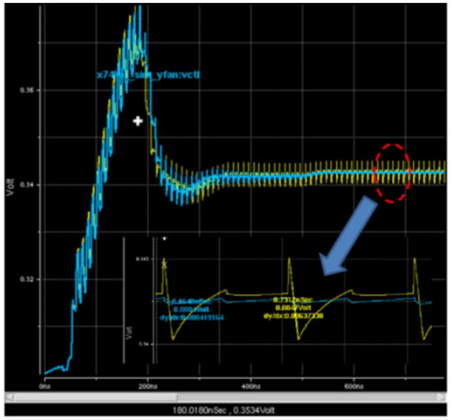
Static Phase Error due to leakage from supply

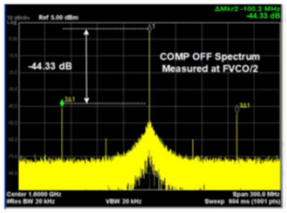


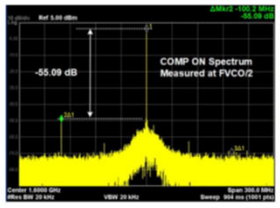
Two pulse digital leakage compensation for leakage from supply





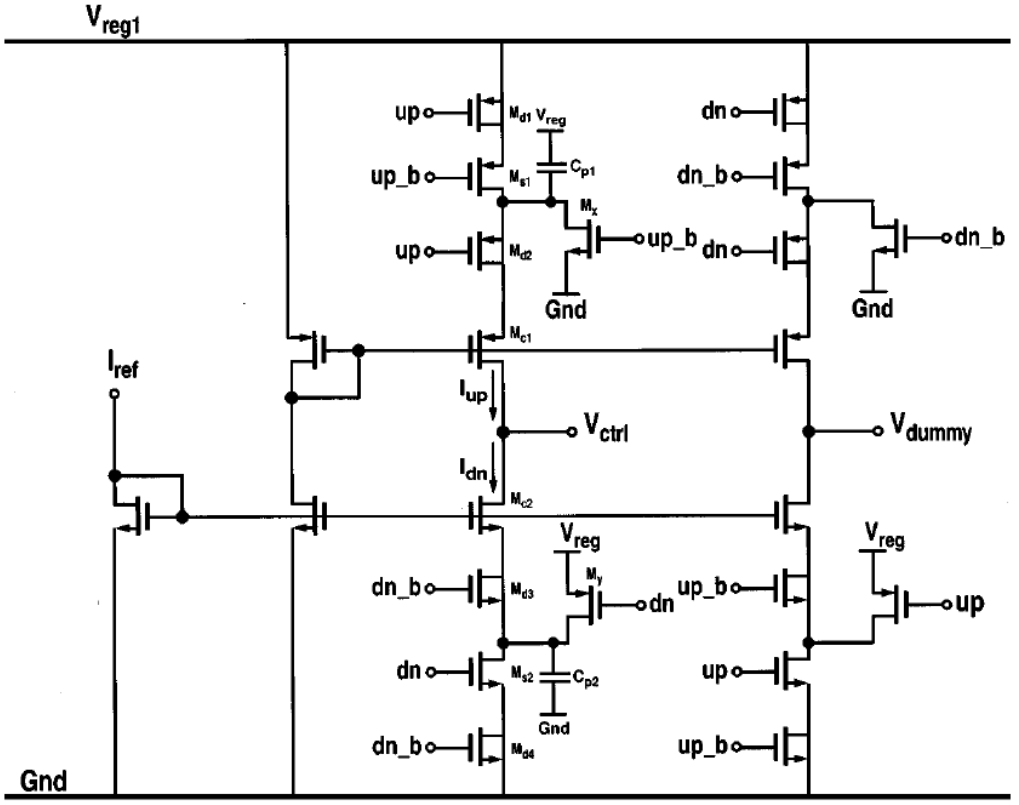






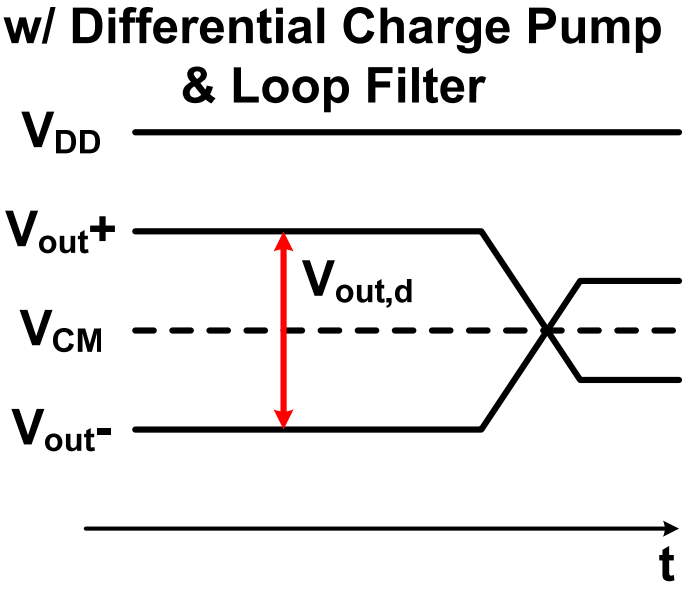
Charge Pump w/ Reversed Switches

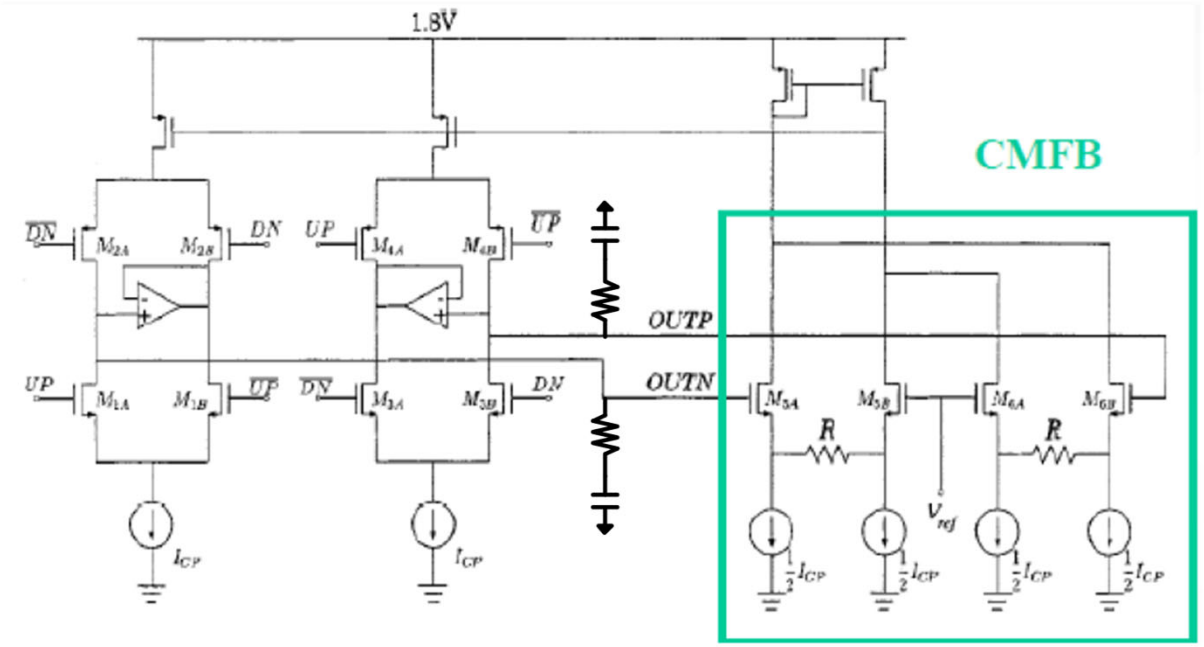
- Swapping switches reduces **charge injection**
  - MOS caps (Md1-4) provide extra **clock feedthrough** cancellation
- Helper transistors Mx and My quickly turn-off current sources
- Dummy branch helps to match PFD loading
- Helps with charge injection, but charge sharing is still an issue



[**Ingino JSSC 2001**]

Fully-Differential Charge Pump

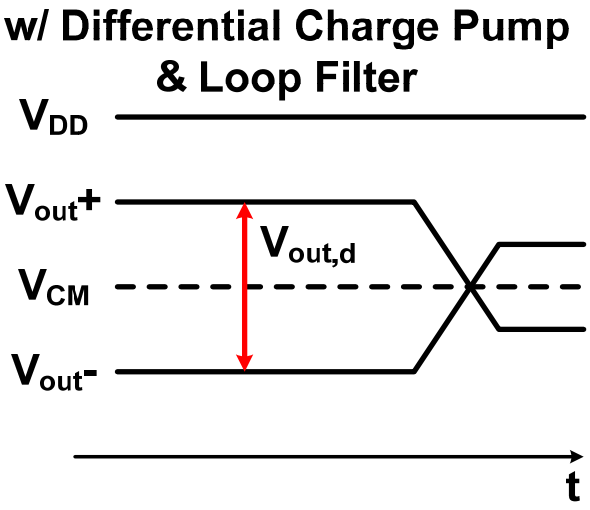


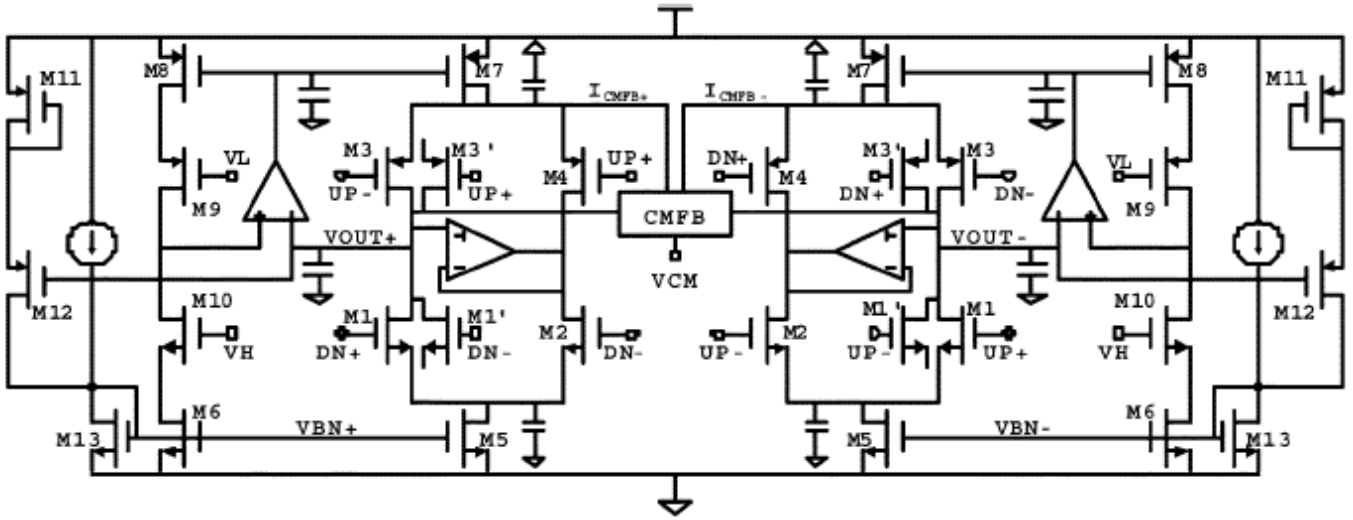


- CMFB loop adjusts the top current sources to match I_{CP} at the differential loop filter common-mode level

Everything But The Kitchen Sink

[**Cheng TCAS2 2006**]

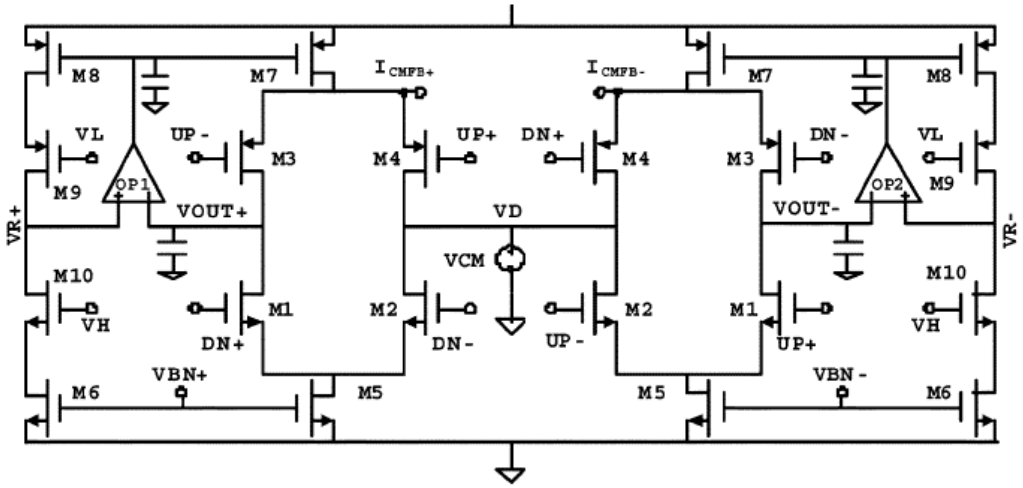




- This fully-differential charge pump uses many techniques to match the UP/DN current sources and mitigate charge injection and charge sharing
  - Dummy path M2 and M4 w/ feedback amps to match current source V_{DS}
  - Dummy switches M1’ and M3’ provide charge injection cancellation
  - CMFB circuit matches UP/DN current at the filter common-mode output
  - Left and right-most feedback loop improve matching considering the differential loop filter control voltage
  - Additional PMOS current sources M11 & M12 extend matching over a wide voltage range

Improved Matching w/ Differential Output

[**Cheng TCAS2 2006**]



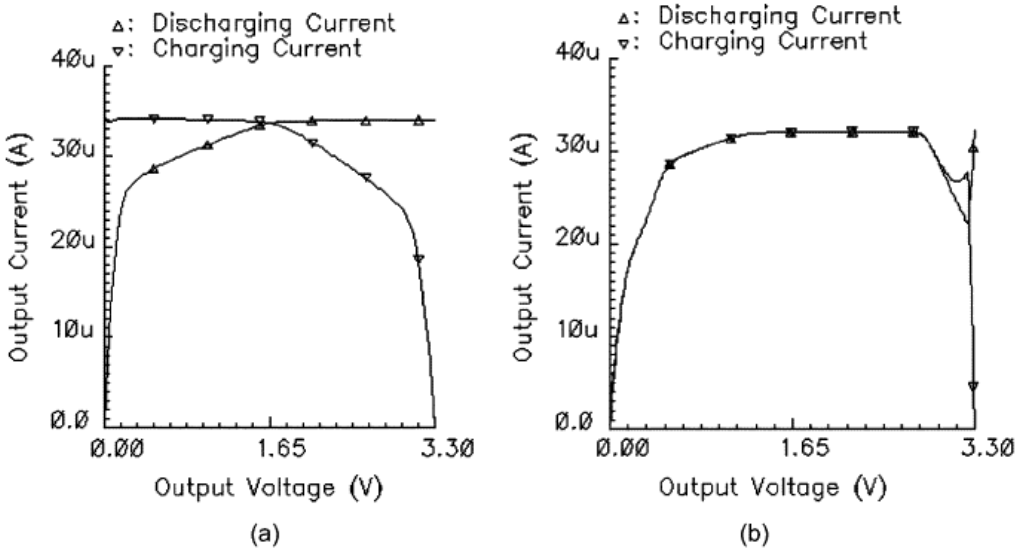
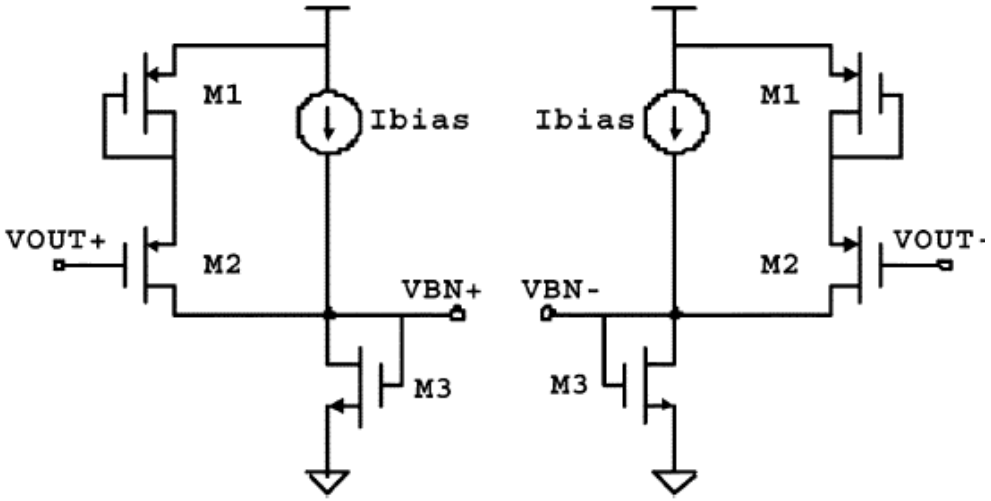


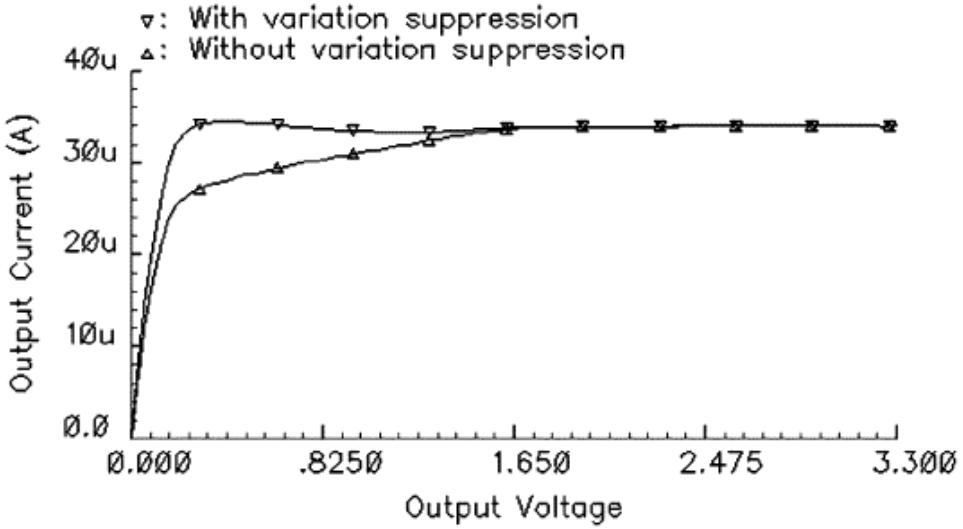
Fig. 4. Output currents with and without mismatch suppression.

- The CMFB loop compensates for current source mismatch at the common-mode level
- However, it cannot compensate for current source mismatch due to the differential control output voltage, as this voltage is symmetric with the common-mode
- Additional feedback networks (OP1 & OP2) provide for improved matching with the differential control output voltage

Additional Current Variation Suppression

[**Cheng TCAS2 2006**]

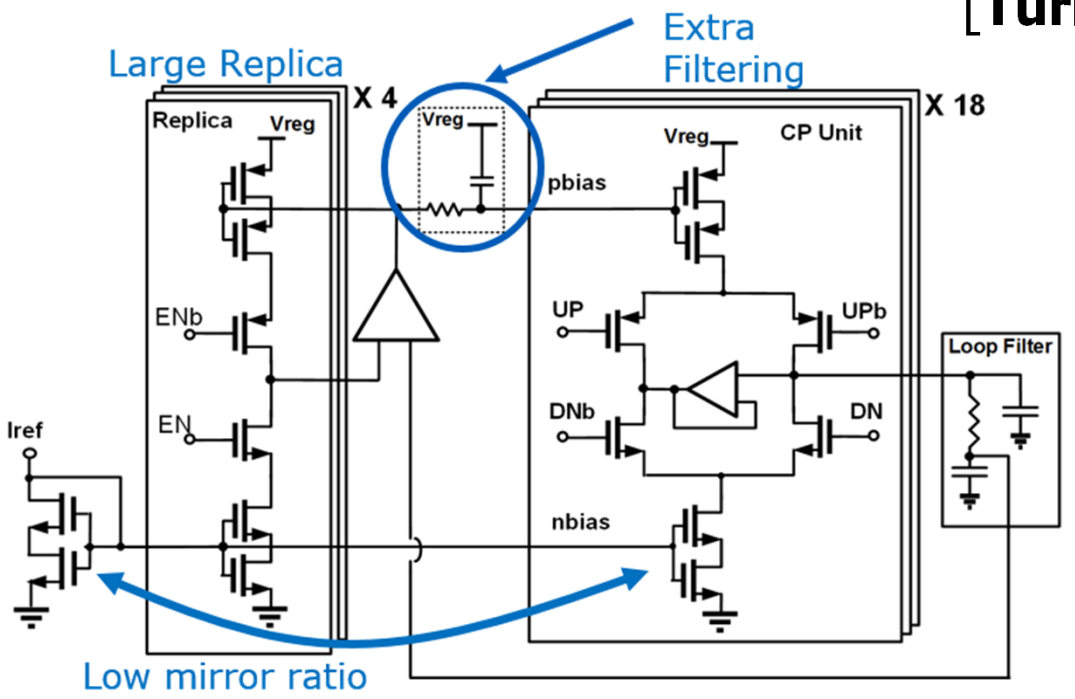




- While matching is good at the control voltage extremes, the absolute current value falls due to finite current source output resistance
- Additional PMOS current sources M1 and M2 provide additional NMOS current when the single-ended control voltage is low, which the main PMOS current source then tracks via feedback
- This extends the voltage range over which the absolute charge pump current matches its nominal value

Low-Noise Charge Pump

[**Turker ISSCC 2018**]



- Low mirroring ratio between input diode-connected transistor and charge pump current source
- Large replica bias transistors to set PMOS current
- Extra filtering in PMOS bias
- Stacked transistors utilized

Next Time

- Loop Filter Circuits