Why Broadband Circuits?

• Broadband circuits are used in many wireline and wireless communication systems

• Trends in processor design and the growing demand for digital connectivity are pushing data rates and bandwidth requirements in these systems

• In this class, we will study key clocking, amplifier, and logic circuits that enable these communication systems to scale in performance
Class Topics

- Broadband circuit design methodologies
- Clocking circuits
  - Phase-Locked Loops (PLLs)
  - Clock-and-Data Recovery systems (CDRs)
- Broadband amplifiers
  - Transimpedance, limiting, and variable-gain amplifiers
- High-Speed Logic
  - Design techniques for high-speed CMOS and CML logic
Analog Circuit Sequence

Pre/Co-Requisite

Electronics I 325
Electronics II 326

Operational Amplifiers 457
Solid-State Devices 671
Data Converters 610

VLSI Circuit Design 474
Advanced Analog Circuit Design 607
Integrated CMOS RF Circuits and Systems 665

Active Filter Analysis and Design 458
Broadband Circuits 620
Active Network Synthesis 622

Advanced Mixed-Signal Interfaces 669
MM-Wave Integrated Circuits 689
High-Speed Links Circuits & Systems 720

High Frequency GaAs/SiGe Analog IC Design 650
Administrative

• Instructor:
  • Sam Palermo
  • 315E WERC Bldg., 845-4114, spalermo@ece.tamu.edu
  • Office hours: MW 1:00pm-2:30pm

• Lectures: MWF 10:20am-11:10am, ZACH 223A

• Class web page
  • http://www.ece.tamu.edu/~spalermo/ecen620.html
Class Material

• Textbook: Class Notes and Technical Papers

• Key References

• Class notes
  • Will hand out hard copies in class
Grading

• Exams (60%)
  • Three midterm exams (20% each)

• Homework (20%)
  • Collaboration is allowed, but independent simulations and write-ups
  • Need to setup CADENCE simulation environment
  • No late homework will be graded

• Final Project (20%)
  • Groups of 1-2 students
  • Report and PowerPoint presentation required
Prerequisites

• Circuits
  • ECEN474 or approval of instructor
  • Basic knowledge of CMOS gates, flops, etc…
  • Circuit simulation experience (HSPICE, Spectre)

• Systems
  • Basic knowledge of s- and z-transforms
  • MATLAB experience
Simulation Tools

• Matlab

• Cadence

• 90nm CMOS device models
  • Can use other technology models if they are a 130nm or more advanced CMOS node

• Other tools, schematic, layout, etc… are optional
Preliminary Schedule

<table>
<thead>
<tr>
<th>Topic</th>
<th>Week</th>
</tr>
</thead>
<tbody>
<tr>
<td>I. Introduction and Linear Systems</td>
<td>Week 1-4</td>
</tr>
<tr>
<td>II. PLL System Analysis</td>
<td></td>
</tr>
<tr>
<td>1st Exam</td>
<td>Oct. 3</td>
</tr>
<tr>
<td>III. PLL Building Blocks</td>
<td></td>
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<tr>
<td>IV. CDRs</td>
<td>Week 5-9</td>
</tr>
<tr>
<td>2nd Exam</td>
<td>Nov. 7</td>
</tr>
<tr>
<td>V. Broadband Amplifiers</td>
<td></td>
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<tr>
<td>VI. Other Topics</td>
<td>Week 10-14</td>
</tr>
<tr>
<td>3rd Exam</td>
<td>Dec. 5</td>
</tr>
<tr>
<td>Project Report Due</td>
<td>Dec. 9</td>
</tr>
<tr>
<td>Project Presentation</td>
<td>Dec. 16</td>
</tr>
</tbody>
</table>

- Dates may change with reasonable notice
High-Speed Electrical Link System

 Serializer -> TX -> Channel -> RX ->Deserializer

 TX data -> TX clk

 PLL ref clk -> TX clk

 RX clk -> RX clk

 TX data: D[n] D[n+1] D[n+2] D[n+3]

 TX clk

 RX clk
10GHz PLL Example

<table>
<thead>
<tr>
<th>PLL Performance</th>
<th>TxPLL</th>
<th>RxPLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min freq (GHz)</td>
<td>8.98</td>
<td>8.96</td>
</tr>
<tr>
<td>Max freq (GHz)</td>
<td>13.54</td>
<td>13.47</td>
</tr>
<tr>
<td>Mean freq (GHz)</td>
<td>11.26</td>
<td>11.22</td>
</tr>
<tr>
<td>Lock range (GHz)</td>
<td>4.56</td>
<td>4.52</td>
</tr>
<tr>
<td>+/−20.2%</td>
<td>+/-20.1%</td>
<td></td>
</tr>
<tr>
<td>Fine tune hold range</td>
<td>5.8%</td>
<td>5.8%</td>
</tr>
<tr>
<td>Quarter rate clock phase noise @ 10MHz offset (dBc/Hz)</td>
<td>-117.8</td>
<td>-117.7</td>
</tr>
<tr>
<td>Jitter, 1MHz-100MHz (ps rms)</td>
<td>1.5</td>
<td>1.4</td>
</tr>
<tr>
<td>Jitter, fc/1667-100MHz (ps rms)</td>
<td>0.64</td>
<td>0.64</td>
</tr>
</tbody>
</table>

100mW Power consumption (with clock distribution)

[Meghelli (IBM) ISSCC 2006]
High-Speed Logic Example: Divide-by-2 with CML FF

- High-speed logic blocks are required in numerous high-speed circuits, such as PLLs, CDRs, and equalizers.
- Relative to CMOS logic, current-mode logic (CML) circuits can achieve higher bandwidth due to lower self-loading.
- Additional bandwidth extension can be achieved with the addition of passives (inductors) and feedback.

[Diagram of Divide-by-2 circuit with CML FF]  

[Razavi]
Detailed Serial-Link Receiver Architecture

Key Features:
- Half-rate design
- 5-tap continuously adaptive DFE
- Variable gain amplifier
- Digital CDR
- ESD protection (HBM & CDM)
- 130mW (with DFE and CDR logic)

[Meghelli (IBM) ISSCC 2006]
**Key Features:**
- Fully digital loop
- Can handle up to +/- 4000ppm frequency offset
- Independent I,Q control

![Receiver Jitter tolerance curve ( BER<1e-9)](image)

Tracking bandwidth ~9MHz

[Meghelli (IBM) ISSCC 2006]
Variable-Gain Amplifier (VGA) Example

Key Features:
- Dual Diff Amps
  - Half/Full Amplitude
- Switched R Degen
- 7 Bit Thermometer
  - Multi-bit Slewrate
- Glitchless Operation
- Continuous Adjustment
- Optimized with GA

[Sorna (IBM) ISSCC 2005]
Optical Receiver Front-End

- Transimpedance amplifiers (TIAs) convert an input current signal into an output voltage with a transimpedance gain.
- Limiting amplifier amplifies the TIA output to a reliable level to achieve a given BER with a certain decision element (comparator).
Next Time

• Linear circuit analysis review