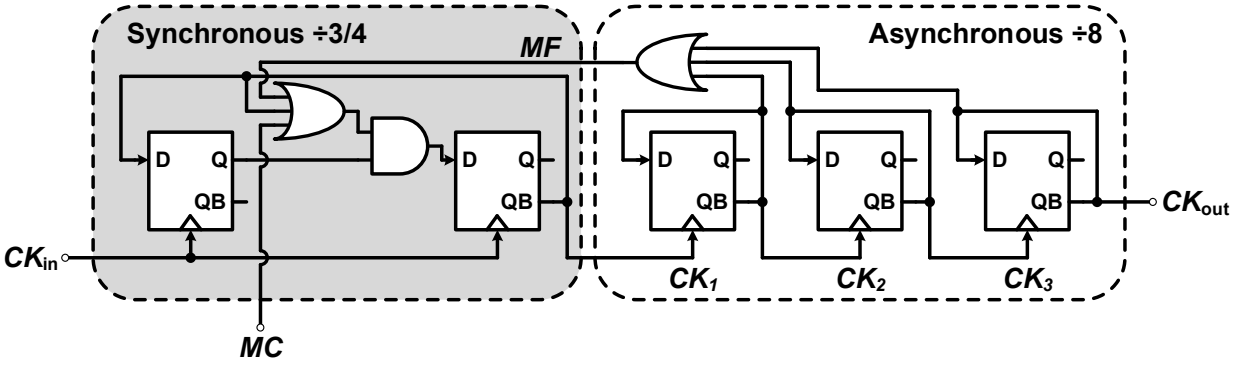
Homework #3 Problem 2 Solution

Divide-by-31/32



MC=1 → ÷32
The circuit is not sensitive to the *MF* signal and the first synchronous divider always divides by 4.

MC=0 → ÷31
The circuit is now sensitive to the MF signal, which will go low 1 out of every 8 cycles due to the asynchronous divide-by-8 second stage. This causes the first synchronous stage to divide by 4 seven times and 3 once, resulting in an overall divide-by-31 operation.