ECEN 620

Homework #3

Due: 10-31-2023, 11:59PM Homeworks will not be received after due. Instructor: Sam Palermo

- 1. VCO Design and Comparison. This problem compares the design of a ring and LC-oscillator. Refer to the 665 lab notes posted on the website for help in the simulations.
 - **a. Ring Oscillator Design.** Shown below is a 3-stage ring oscillator that employs a replica-bias scheme to ensure a constant swing over frequency tuning. Design this circuit at the transistor-level to meet the following specifications:
 - i. 3.125GHz nominal operating frequency
 - ii. Phase Noise < -90dBc/Hz @1MHz offset
 - **iii.** Minimum Tuning Range = 1.5GHz to 3.5GHz

You are free to use whatever voltage swing you would like for the ring oscillator. Reasonable swing values are 0.3-0.5*VDD single-ended peak-to-peak (differential amplitude). Note, there is only one replica bias delay cell that is shared to provide the tail current gate bias voltage for all the 3 VCO delay cells.



3-stage differential ring oscillator.

- **b.** LC Oscillator Design. Design an LC-oscillator at the transistor-level to meet the following specifications:
 - i. 3.125GHz nominal operating frequency
 - ii. Phase Noise < -90dBc/Hz @1MHz offset. Note, this should be easier for this design, relative to the previous ring oscillator.
 - iii. Minimum Tuning Range = 2.8GHz to 3.5GHz

You are free to use whatever topology you would like. If you do not have a design kit inductor model, then use a maximum Q=5 and model this with a series resistor. If you do have access to a design kit inductor, then using a Q>5 is fine.

- c. **ISF Simulations.** Obtain the impulse sensitivity function for both the designed ring and LC oscillators by following the procedure outlined in the "VCO ISF Simulation" notes on the website. Place a single noise current source on one of the oscillators' output (single-ended) nodes to obtain the ISF.
 - i. Use a minimum of 100 phase points to construct the ISF function.
 - ii. Normalize the LC oscillator ISF for an absolute peak of 1, as the notes describe.
 - iii. Use the same LC oscillator normalization factor to scale the ring oscillator ISF.
 - iv. Plot both of the normalized LC and ring oscillator ISFs on a single plot and comment on the differences.

d. **Oscillator Comparison.** Make a summary table that compares the two oscillators. One row of the table should be the following figure-of-merit (FOM) which normalizes phase noise performance with oscillator power

FOM =
$$\left(\frac{f_0}{f_m}\right)^2 \frac{1}{L(f_m)P_{avg}}$$
,

where f_0 is the 3.125GHz oscillation frequency, f_m is the 1MHz offset, $L(f_m)$ is the phase noise, and P_{avg} is the oscillator average power consumption.

2. **Divider Design.** Design a dual-modulus divider which realizes a divide-by-31/32 function and can operate at a maximum 3.5GHz input frequency. Simulate the divider with both the designed ring and LC-oscillators from Problem 1.