# Design and Analysis of an Ultrahigh-Speed Glitch-Free Fully Differential Charge Pump With Minimum Output Current Variation and Accurate Matching

Shanfeng Cheng, *Student Member, IEEE*, Haitao Tong, *Student Member, IEEE*, Jose Silva-Martinez, *Senior Member, IEEE*, and Aydin Ilker Karsilayan, *Member, IEEE*

***Abstract*—An ultrahigh-speed fully differential charge pump with minimum current mismatch and variation is proposed in this brief. A mismatch suppression circuit is employed to minimize the mismatch between the charging and discharging currents, which minimizes the steady-state phase error in a phase-locked loop (PLL). A variation suppression circuit is proposed to minimize output current variation with the change of output voltage, which reduces the variation of the bandwidth in a PLL. Techniques are proposed to suppress both low-speed glitches and high-speed glitches in the output current to allow glitch-free operation of the charge pump with ultrafast input pulses. The differential charge pump is designed and simulated under the power supply of 3.3 V in TSMC 0.35-$\mu$m CMOS technology to verify the effectiveness of the proposed techniques.**

***Index Terms*—Charge pump, current variation, differential charge pump, glitch, mismatch, phase-locked loop (PLL).**

## I. Introduction

PHASE-LOCKED loops (PLLs) are widely used in modern communication systems. A PLL based on a charge pump is preferred over other types because it has a wide capture range and no systematic phase offset. In practice, nonidealities of the charge pump degrade the performance of the entire loop. The mismatch between the charging and discharging current introduces steady-state phase offset and increases reference spurs in a PLL. The variation of the output current amplitude of the charge pump due to the change of the output voltage will result in variation of the loop bandwidth. Glitches in the output current will increase the level of reference spurs in frequency synthesizers. It will also increase the level of jitter generation in clock and data recovery (CDR) systems, which are widely used in multigigahertz serial data links.

Several single-ended charge pump structures were proposed in the literature [1]–[6]. A single-ended charge pump with positive feedback was proposed in [2] to boost the operational frequency of the charge pump. An obvious disadvantage of that technique is that the positive feedback will result in an undesirable hysteresis effect which swallows narrow input pulses. A technique was proposed in [3] to eliminate the high-frequency glitches, which is done at the price of decreasing the operational frequency of the charge pump. The charge pump proposed in [4] uses wide-swing current mirrors which still suffer from heavy mismatch when the output voltage comes close to the rails. The charge pump proposed in [5] uses source-switching, but it is slow to turn off the output current. In high-performance applications with stringent noise suppression requirements, a fully differential charge pump is preferred over a single-ended charge pump because of the immunity to common-mode noise and power supply variation [1]. Some recent works [7]–[9] proposed differential charge pump structures which have only common-mode feedback (CMFB) but do not suppress the differential mismatch errors.

A novel fully differential charge pump for applications in high-speed high-performance PLLs is proposed in this brief. Section II covers the charge pump design with mismatch and variation suppression. Section III discusses the techniques to suppress the transient glitches. Section IV shows the complete schematic of the charge pump with system-level performance verification. Section V draws conclusions from this work.

## II. Fully Differential Charge Pump With Accurate Matching and Minimum Current Variation

### A. Differential Charge Pump With Mismatch Suppression

Fully differential charge pumps are preferred in high-performance PLLs with stringent requirements on noise suppression [1]. The conceptual diagram of a fully differential charge pump is shown in Fig. 1. Several differential charge pump structures with proper CMFB have been reported [7]–[9]. The CMFB, however, cannot eliminate the differential error caused by the mismatch between charging and discharging current when the differential output voltage is not zero. To illustrate this, let us define the output voltages as

$$\begin{aligned} V_{\mathrm{OUT}+} &= V_{\mathrm{CM}} + \Delta V \\ V_{\mathrm{OUT}-} &= V_{\mathrm{CM}} - \Delta V \end{aligned} \tag{1}$$

where $V_{\mathrm{CM}}$ is the desired common-mode voltage and $\Delta V > 0$. We also assume that those voltages are the exact values required by the voltage-controlled oscillator (VCO) to operate at the desired frequency. However, due to the channel-length modulation effect, the charging current will be smaller than the discharging

Manuscript received May 21, 2005; revised November 8, 2005. This paper was recommended by Associate Editor F. Maloberti.

The authors are with Analog and Mixed-Signal Center, Department of Electrical Engineering, Texas A&M University, College Station, TX 77840 USA (e-mail: sfcheng@ee.tamu.edu).

Digital Object Identifier 10.1109/TCSII.2006.879100

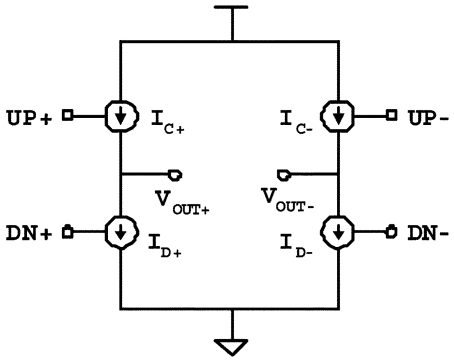


Fig. 1. Conceptual diagram of a differential charge pump.

current on the positive output terminal while the charging current will be larger than the discharging current on the other side. We can assume for simplicity that

$$I_{C+} = I_{D-} = I_0 - \Delta I$$
$$I_{C-} = I_{D+} = I_0 + \Delta I \quad (2)$$

where $\Delta I > 0$ and $\mathbf{I}_0$ is the current when the output voltage is equal to $V_{\rm CM}$. Let us consider the case of a classic phase-frequency detector [10]. The up (UP) and down (DN) pulses have the same width when the input phase difference is zero. Thus, we can define the overall differential output current as

$$I_{\rm diff} = (I_{C+} - I_{D+}) - (I_{C-} - I_{D-}) = -4\Delta I. \quad (3)$$

Instead of staying at the desired voltages, the positive output voltage will decrease while the negative output voltage will increase, due to the nonzero differential current. This error cannot be corrected by the CMFB circuit since the two output voltages are symmetric around the common mode level. Thus, the PLL has to settle to a nonzero phase error. Also, the UP and DN pulses will have different widths, which increases the level of reference spurs.

To overcome this drawback, we propose a differential charge pump with excellent mismatch suppression, which is shown in Fig. 2. The charging and discharging current are turned on when UP and DN are high, respectively. The mismatch suppression technique is derived from the one proposed in [11]. The terminals $\mathbf{I}_{\rm CMFB+}$ and $I_{\rm CMFB-}$ are reserved for injection of CMFB current. Two opamps are used to ensure that $V_{R+} \cong V_{\rm out+}$ and $V_{R-} \cong V_{\rm out-}$. VH and VL are the logic low level and logic high level of the differential input signal. When the charge pump is providing discharging current, the discharging current flowing through M1 will be equal to the current flowing through M10 because the transistor pairs (M1, M5) and (M10, M6) are matched. On the other hand, when the charge pump is providing charging current, the current flowing through M3 will be equal to the current flowing through M9 since the transistor pairs (M3, M7) and (M9, M8) are matched. Thus, the amplifiers force the charging current to closely follow the discharging current. A simplified version of the rail-to-rail opamp proposed in [12] with 54-dB dc gain is used to implement the amplifiers. A large capacitor must be added at the gate of M7/M8 to properly compensate for the feedback loop.

The CMFB circuit is shown in Fig. 3. It amplifies the common-mode error signal and converts it into two output currents. Source degeneration is used at the input stage to maximize the linear input swing so that the CMFB circuit

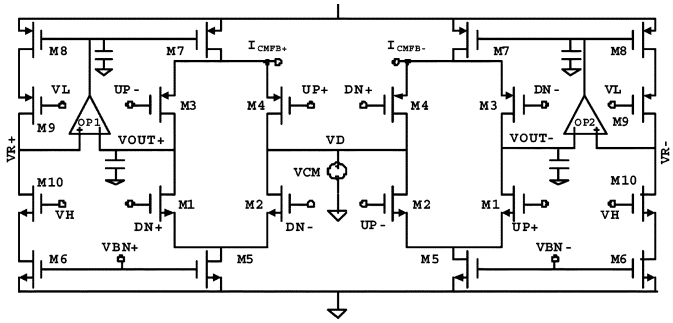


Fig. 2. Proposed fully differential charge pump with mismatch suppression.

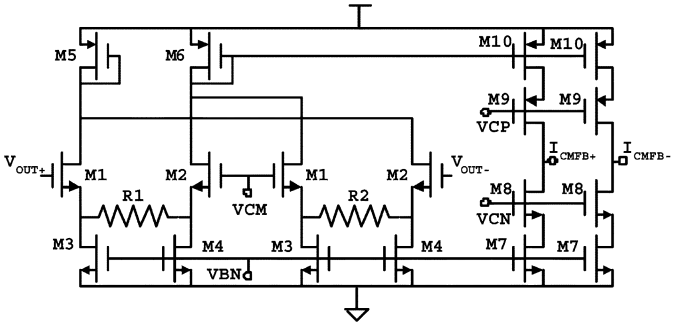


Fig. 3. CMFB circuit for the differential charge pump. (a) Without mismatch suppression. (b) With mismatch suppression.

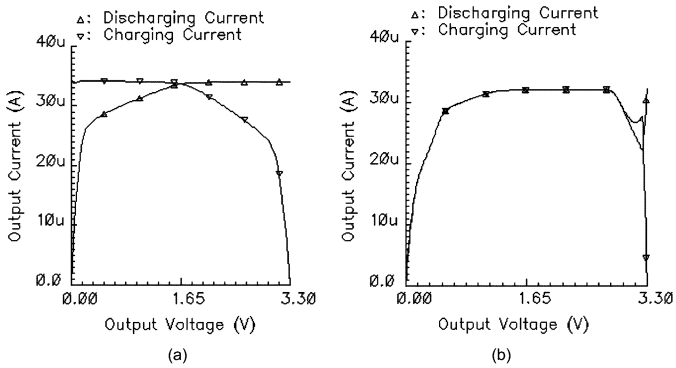


Fig. 4. Output currents with and without mismatch suppression.

can work properly over a large swing. The output currents are injected into the nodes $\mathbf{I}_{\rm CMFB\pm}$ in the charge pump shown in Fig. 2 without interfering with the operation of the mismatch suppression circuit previously discussed.

The differential charge pump is designed at transistor level in TSMC 0.35-$\mu$m CMOS technology with a 3.3-V supply. The charge pump is simulated to verify the effectiveness of the proposed techniques. Fig. 4 shows the output currents versus the output voltage with and without mismatch suppression. Without mismatch suppression, the charging current and discharging current are close to each other only when the output voltage is near the common-mode voltage (1.65 V). When the output voltage goes farther away from the common-mode level, the difference between the charging and discharging current becomes larger. If the desired output swing is $\pm 1$ V around 1.65 V, the current mismatch can be as high as 15%, which will cause unacceptable phase offset in many applications. After the introduction of a mismatch suppression circuit, the charging current and discharging current match very well for a large swing from 0.1 to 3 V.

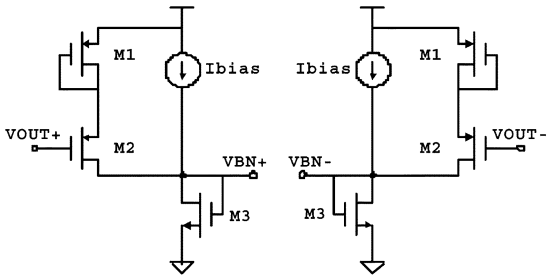


Fig. 5. Variation suppression circuit.

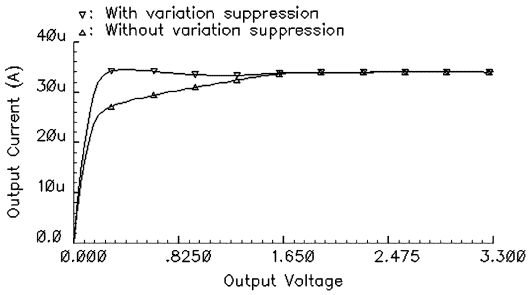


Fig. 6. Comparison of charge pump output current with and without variation suppression.

### *B. Suppression of Output Current Variation*

It is evident in Fig. 4(b) that both output currents decrease when the output voltage goes towards zero. At 0.3-V output voltage, the current amplitude decreases by 30% from the nominal value at the common-mode level. Unfortunately, the variation of charge pump output current will result in variation of the PLL loop bandwidth. Such a big variation may bring the PLL from a stable region to an unstable region.

To suppress the current variation dependent on the output voltage, we propose the variation suppression circuit shown in Fig. 5 to dynamically adjust the bias voltages $V_{\mathrm{BN}\pm}$ (also marked in Fig. 2) and, hence, the charge pump bias current. When the output voltage is higher than the common-mode level, M1–M2 from the compensation circuit stay off and have no effect on the tail current source bias voltages $(V_{\mathrm{BN}\pm})$. When the output voltage goes low enough to push the NMOS output transistor into the triode region, M1–M2 from the compensation circuit starts to conduct and injects current into M3. This results in an increase of the bias current for the charge pump as an effective compensation. As a rule of thumb, M2 can be designed to conduct when the output transistor starts to enter the triode region, i.e., $V_{\mathrm{OUT}} = 2V_{\mathrm{dsat,NMOS}}$. DC sweep simulation can be done to achieve optimum compensation in actual design.

Fig. 6 shows the discharging output current of the charge pump with and without the variation suppression circuit. It can be seen that the variation suppression technique extends significantly the range of the output voltage for a given variation tolerance. The output current variation is controlled within 3% when the output voltage is higher than 0.2 V.

## III. Glitch Suppression

For an ideal charge pump, if a square-wave control signal with a particular rising time and falling time is applied, the output current should be a square wave without any glitches. However, in the actual implementation of a differential charge pump, the output current pulse has glitches whose magnitude increases with the speed of the input signal. The current glitches are generated mainly via two mechanisms discussed in the following subsections.

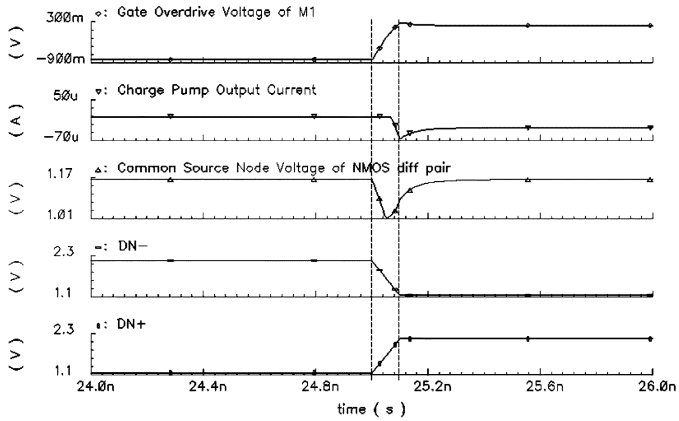


Fig. 7. Transient waveforms of the NMOS differential pair with fast input signal.

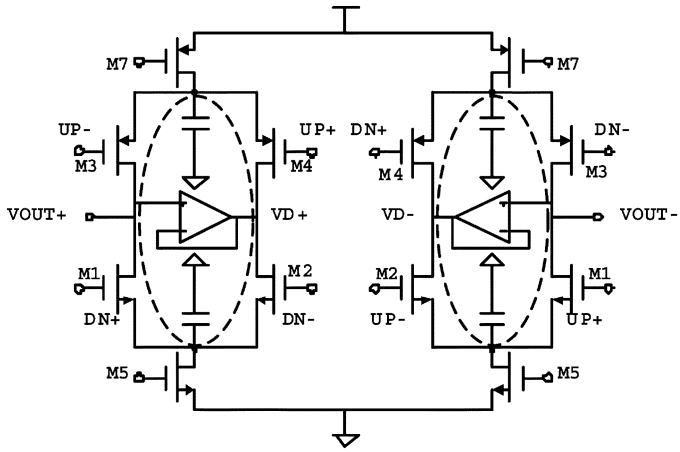


Fig. 8. Proposed low-speed glitch suppression circuit (enclosed in ellipses).

### *A. Low-Speed Glitch*

The first type of glitch is caused by the speed limitation of the common source node of the differential pairs. Let us consider the NMOS differential pair in the charge pump in Fig. 2 with a very slow input pulse. When the input is balanced, the common node voltage $V_S$ is equal to $V_{S1} = V_{\mathrm{CM}} - V_{\mathrm{TH}} - V_{\mathrm{dsat,M1}}$. When the differential pair is fully switched to one side, $V_S$ is equal to $V_{S2} = V_H - V_{\mathrm{TH}} - \sqrt{2}V_{\mathrm{dsat,M1}}$, which is smaller than the value when the input is balanced under the condition that the input signal swing is much larger than $V_{\mathrm{dsat,M1}}$. Thus, with a slow input pulse, $V_S$ goes down to $V_{S1}$ when the input is balanced and goes back to $V_{S2}$ when the input is fully switched to the other side. However, when the input signal is very fast, $V_S$ is not able to settle to the value of $V_{S2}$ as soon as the input finishes switching, due to heavy parasitics at the common source node. Thus, there is a temporary overshoot of $V_{\mathrm{gs}}$ for the transistor being turned on, which leads to overshoot of the output current. Fig. 7 shows the transient waveforms of the NMOS differential pair in the charge pump during the switching. This overshoot current is referred to as low-speed glitch in this study.

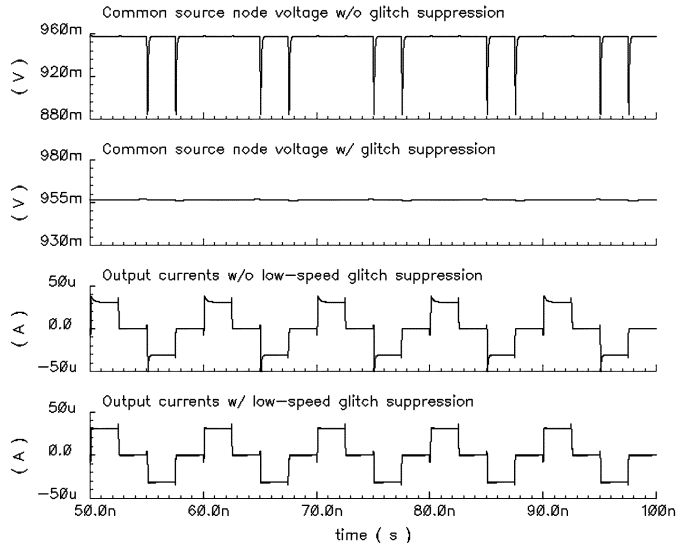


Fig. 9. Common source node voltage (NMOS differential pair) and output current of the charge pump with and without low-speed glitch suppression circuit.

The circuit shown in Fig. 8 is proposed to minimize the low-speed glitch. Two relatively large capacitors are added at the common source nodes of the differential pairs. They are used to minimize the voltage variation on the common source nodes during the transition of the input signal by pulling the common source node down to a much lower speed compared with the input signal. Also, instead of using a fixed bias for $V_D$ as shown in Fig. 2, an amplifier in the unity-gain feedback configuration is added to ensure that $V_{\rm out}$ and $V_D$ have very close voltages [13]. As a result, the common source node will have the same voltage before and after the switching. The amplifier used here has the same structure as the one used for the mismatch suppression.

The charge pump was simulated with and without low-speed glitch suppression. The output currents are shown in Fig. 9. The input signal has a pulsewidth of 2.5 ns with a transition time of 0.1 ns. Without the glitch suppression circuit, the voltage at the common source node of the NMOS differential pair experiences a slow variation with a peak around 60 mV, which causes large and wide glitches in the output current. After the introduction of the low-speed glitch suppression circuit, the variation of the common source node voltage is much smaller (about 1 mV). As a result, the low-speed glitch on the output current is almost completely eliminated. On the other hand, we can see that there still remain fast and sharp glitches in the output current even with the low-speed glitch suppression circuit. This is called high-speed glitch, which will be discussed in Section III-B.

### *B. High-Speed Glitch*

The high-speed glitch is generated by charging or discharging the gate-to-drain capacitance $(C_{\rm gd})$ of the output transistors, which directly injects current into the output node. Let us assume that the input voltage has a transition time of $\Delta T$ to switch from $V_L$ to $V_H$. The generated glitch current is expressed as

$$I_{\rm glitch} = C_{\rm gd}(V_H - V_L)/\Delta T = C_{\rm gd}K \tag{4}$$

where $K$ represents the slew rate of the input voltage during transition. The glitch magnitude is proportional to the input voltage slew rate and the gate-to-drain capacitance. The amplitude of the high-speed glitch can be larger than the output

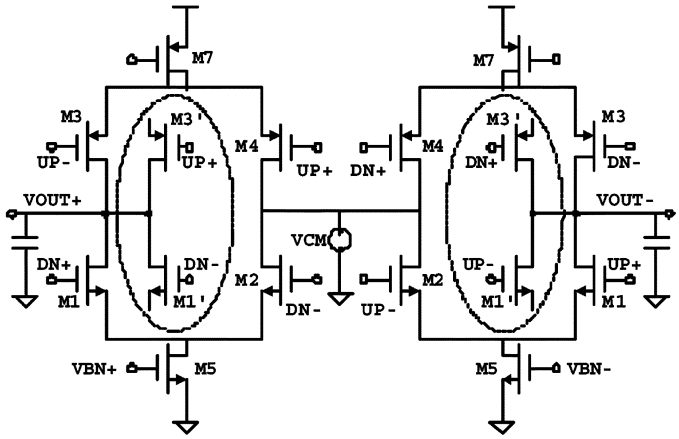


Fig. 10. Proposed high-speed glitch suppression circuit (enclosed in ellipses).

current itself when the input signal is switching extremely fast. This kind of glitch is very narrow and has approximately the same width as the input transition time. If somehow the output transistor goes into deep triode region (e.g., the NMOS output transistor will go into triode region when the output voltage is very low), $C_{\rm gd}$ will be close to half the MOS gate capacitance, i.e.,

$$C_{\rm gd} = C_{\rm gs} = C_{\rm gg}/2 = WLC_{\rm ox}/2. \tag{5}$$

When this happens, the gate-to-drain capacitance will be several times larger and so is the induced glitch current. To minimize the glitch, it is always desirable to keep the output transistors in saturation region. In addition, it maximizes the switching speed of the charge pump if the output transistors work in the saturation region instead of the triode reğion.

The circuit shown in Fig. 10 is proposed to suppress the high-speed glitches. The source terminals of M1′ and M3′ are left floating to avoid extra dc current. The transistors M1′ and M3′ match the size of the transistors M1 and M3. When both M1 and M1′ stay in the saturation region, they have the same gate-to-drain overlap capacitance. Thus, the glitches on the discharging current induced by the switching of DN+ and DN− cancel each other. The same thing happens for the glitches produced on the charging current provided by PMOS devices.

The output current glitches are simulated for the charge pump with and without the high-speed glitch suppression circuit (the low-speed glitch suppression technique is applied in both cases). The output current waveform is shown in Fig. 11. The input signal has 50-ps pulsewidth with 5-ps transition time. The output current has extremely large glitches due to the fast switching of the input signal. With such a high-speed input signal, the desired output current level (about 30 $\mu$A) is totally drowned by the glitches (about 150 $\mu$A). After adding the proposed circuit, the high-speed glitches are almost completely eliminated from the output current since the output transistors and the dummy transistors are matched. It was verified by simulations that the charge pump can have glitch-free operation for 10-ps input pulsewidth and 1-ps transition time with pure large capacitance as load. In practical implementation, however, this performance will be limited by the resistance in the loop filter and any other parasitic resistance like routing resistance and gate resistance.

It should be pointed out that the high-speed glitches generated by the output transistor and dummy transistor fully cancel each

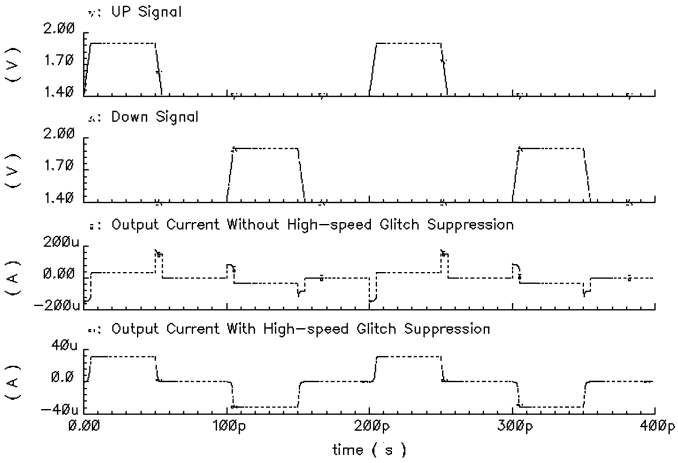


Fig. 11. Output current with and without suppression of high-speed glitch.

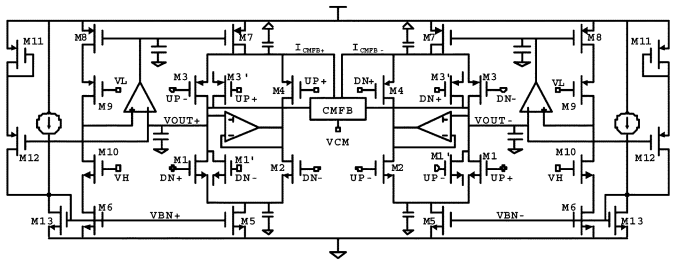


Fig. 12. Complete schematic of the proposed fully differential charge pump.

other only when both of them stay in the saturation region. The output voltage ranges for the NMOS and PMOS transistors to stay saturated are given below, respectively, as

$$\begin{aligned} 0 &< V_{R-\mathrm{PMOS}} \\ &< V_{\mathrm{CM}} - V_A/2 + |V_{\mathrm{TH-PMOS}}| V_{\mathrm{CM}} \\ &\quad + V_A/2 - V_{\mathrm{TH-NMOS}} \\ &< V_{R-\mathrm{NMOS}} \\ &< V_{\mathrm{dd}} \end{aligned} \tag{6}$$

where $V_A$ is the input signal swing. The range for the glitches generated by NMOS and PMOS transistors to be fully cancelled is the cross-set of the two ranges as given as

$$\begin{aligned} V_{\mathrm{CM}} + V_A/2 - V_{\mathrm{TH-NMOS}} &< V_R \\ &< V_{\mathrm{CM}} - V_A/2 + |V_{TH-PMOS}|. \end{aligned} \tag{7}$$

The length of this range is given by

$$\begin{aligned} V_{R-L} &= V_{\max} - V_{\min} \\ &= |V_{\mathrm{TH-PMOS}}| + V_{\mathrm{TH-NMOS}} - V_A \end{aligned} \tag{8}$$

The simulated range of full cancellation in this design is from 1.2 to 2 V with $V_A = 0.6$ V. That's very close to the result estimated by (7).

## IV. Complete Implementation of the Charge Pump

The complete schematic of the fully differential charge pump employing all of the techniques discussed above is shown in Fig. 12. The overall power consumption is around 1 mW with a 3.3-V supply voltage. Simulation results indicate that these techniques can be combined to achieve optimum performance without interfering with each other.

A 10-GHz PLL with 312.5-MHz reference (modeled in Cadence VerilogAMS) using the proposed charge pump was simulated to verify system-level performance improvement. After introducing the proposed techniques, the reference spur is reduced from $-65$ to $-74$ dB for small differential output voltage of 0.4 V. Also, the spur decreases from $-39$ to $-58$ dB for a large differential output voltage of 2 V.

## V. Conclusion

A glitch-free fully differential charge pump with excellent suppression of output current mismatch and variation is introduced in this study. Techniques are proposed to eliminate the low-speed glitches caused by the speed limitation of the common source nodes and the high-speed glitches induced by capacitive coupling. Especially, the technique to suppress the high-speed glitch enables the charge pump to have glitch-free operation with very narrow input pulses. Mismatch suppression circuit is incorporated into the proposed charge pump so that the output currents have very good matching over a large output swing. Variation suppression circuit is employed to effectively minimize the variation of the output current amplitude with the change of the output voltage, which results in more stable loop bandwidth of the PLL.

Detailed analysis and simulation results indicate that the proposed fully differential charge pump is very suitable to be used in high-performance PLLs and CDRs working at the frequency of multigigahertz or even higher.

## References

[1] W. Rhee, "Design of high-performance CMOS charge pumps in phase-locked loops," in *Proc. Int. Symp. Circuits Syst.*, May–Jun. 1999, vol. 2, pp. 545–548.

[2] E. Juarez-Hernandez and A. Diaz-Sanchez, "A novel CMOS charge-pump circuit with positive feedback for PLL applications," in *Proc. Int. Conf. Electron., Circuits Syst.*, Sep. 2001, vol. 1, pp. 349–352.

[3] B. Bahreyni and I. M. Filanovsky, "A novel design for deadzone-less fast charge pump with low harmonic content at the output," in *Proc. Midwest Symp. Circuits Syst.*, Aug. 2002, vol. 3 , pp. III-397–III-400.

[4] R. C. H. Beek and C. S. Vaucher, "A 2.5–10-GHz clock multiplier unit with 0.22-ps RMS jitter in standard 0.18-$\mu$m CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1862–1872, Nov. 2004.

[5] J. F. Parker and D. Weinlader, "A 15 mW 3.125 GHz PLL for serial backplane transceivers in 0.13 $\mu$m CMOS," in *Proc. Int. Solid-State Circuits Conf.*, 2005, pp. 412–413.

[6] D. M. W. Leenaerts and J. v. der Tang, *Circuit Design for RF Transceivers*. Boston, MA: Kluwer, 2001, ch. 7.

[7] T. S. Cheung and B. C. Lee, "A 1.8–3.2-GHz fully differential GaAs MESFET PLL," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 605–601, Apr. 2001.

[8] N. D. Dalt and C. Sandner, "A Subpicosecond Jitter PLL for Clock Generation in 0.12 $\mu$m Digital CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1275–1278, Jul. 2003.

[9] B. Terlemez and J. P. Uyemura, "The design of a differential CMOS charge pump for high performance phase-locked loops," in *Proc. Int. Symp. Circuits Syst.*, May 2004, vol. 4, pp. IV–561-4.

[10] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001, ch. 15, pp. 550–556.

[11] J.-S. Lee and M.-S. Keel, "Charge pump with perfect current matching characteristics in phase-locked loops," *Electron. Lett.*, vol. 36, pp. 1907–1908, Nov. 2000.

[12] J. N. Babanezhad, "A rail-to-rail CMOS op amp," *IEEE J. Solid-State Circuits*, vol. 23, no. 12, pp. 1414–1417, Dec. 1988.

[13] I. A. Young and J. K. Greason, "A PLL clock generator with 5 to 10 MHz of lock range for microprocessors," *IEEE J. Solid-State Circuits*, vol. 27, no. 11, pp. 1599–1607, Nov. 1992.