Texas A&M University
Department of Electrical and Computer Engineering

ECEN 620 – Network Theory (Broadband Circuit Design)

Fall 2022

Exam #2

Instructor: Sam Palermo

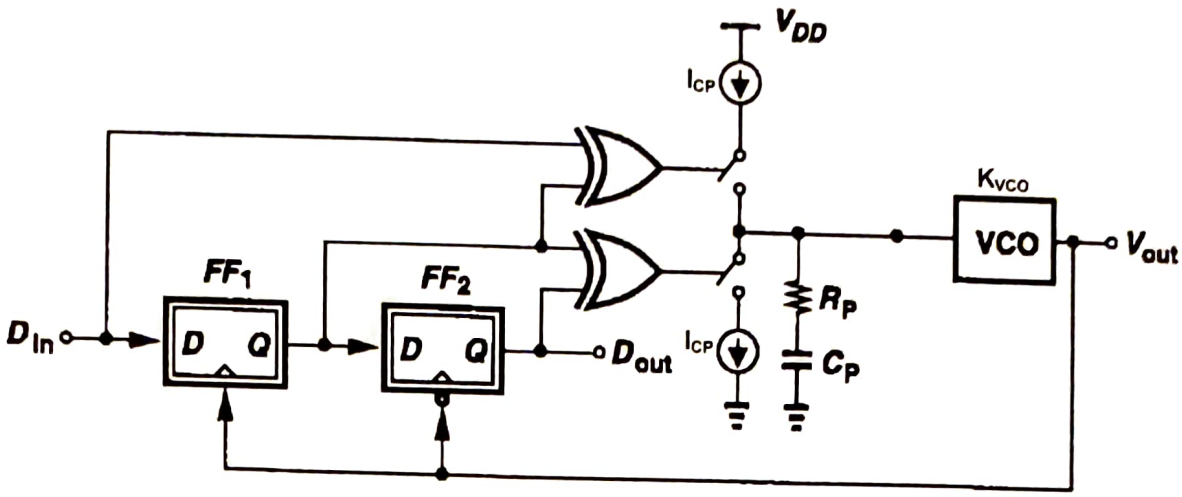
- Please write your name in the space provided below
- Please verify that there are **5** pages in your exam
- You may use <u>one</u> double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		60
2		40
Total		**100**

Name: SAM PALERMO

UIN:

Problem 1 (60 points)
For the CDR shown below, assume that the incoming data has a transition density *TD*.



a) Give the expression for the closed-loop CDR transfer function $H(s)=\phi_{out}(s)/\phi_{in}(s)$ as a function of ω_n and ζ. Also give the expressions for ω_n, ζ, and K_{PD} as a function of the loop parameters.

$$H(s) = \frac{2\zeta\omega_n\left(s + \frac{\omega_n}{2\zeta}\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\frac{K_{PD} I_{CP} K_{VCO}}{C}}$$

$$\zeta = \frac{\omega_n}{2} RC$$

Hogge PD $\Rightarrow$ $K_{PD} = \frac{1}{\pi}(TD) = \frac{TD}{\pi}$

H(s) =

ω_n =

ζ =

K_{PD} =

b) Assume that the maximum input peak-to-peak phase error that the system can tolerate is $1UI_{pp}$. Give an expression for the CDR jitter tolerance, JTOL(s). Also give expressions for the poles and zeros of the system JTOL(s).

$$JTOL(s) = \frac{TM}{1-H(s)} \quad \text{where} \quad TM = 1UI_{pp}$$

$$= \frac{TM}{1 - \frac{2\zeta\omega_n(s+\frac{\omega_n}{2\zeta})}{s^2+2\zeta\omega_n s+\omega_n^2}} = TM\left(\frac{s^2+2\zeta\omega_n s+\omega_n^2}{s^2}\right)$$

To find 2 zeros $s^2+2\zeta\omega_n s+\omega_n^2=0$

$$z_{1,2} = \frac{-2\zeta\omega_n \pm \sqrt{4\zeta^2\omega_n^2 - 4\omega_n^2}}{2}$$

$$= -\zeta\omega_n\left(1 \pm \sqrt{1-\frac{1}{\zeta^2}}\right)$$

JTOL(s) =

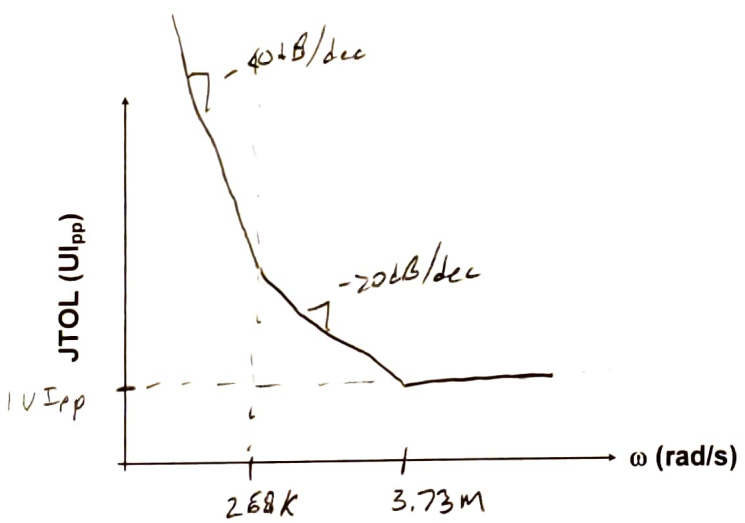
JTOL(s) poles = 2 poles at ϕ

JTOL(s) zeros = $-\zeta\omega_n\left(1 \pm \sqrt{1-\frac{1}{\zeta^2}}\right)$

c) Assume that ω_n=1Mrad/s and ζ=2. Sketch the system JTOL(s) magnitude versus frequency. Label the high frequency value and the key frequencies and slopes in the plot. **Use a log scale for both the x and y-axis.**

$$z_1 = -2(1M)\left(1-\sqrt{1-\frac{1}{4}}\right) = -268K\,rad/s$$

$$z_2 = -2(1M)\left(1+\sqrt{1-\frac{1}{4}}\right) = -3.73M\,rad/s$$

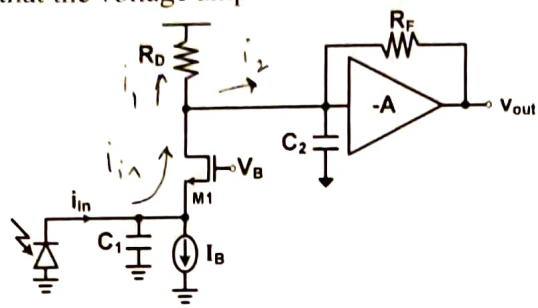


d) If we wish to increase the minimum frequency at which the CDR can tolerate >$1UI_{pp}$ jitter, should ζ be increased or decreased? Justify your answer.

ζ should be increased. We need to increase $|\omega_{z2}| = \zeta\omega_n\left(1+\sqrt{1-\frac{1}{\zeta^2}}\right)$ which for large ζ is $|\omega_{z2}| \approx 2\zeta\omega_n$.

Problem 2 (40 points)

For the TIA shown below, assume that all transistors are operating in saturation with $r_o=\infty$. Also assume that the voltage amplifier has infinite bandwidth, but finite open-loop gain A.



$$V_{OUT} = -\frac{i_2 R_F A}{1+A}$$

$$i_2 = \frac{R_D}{R_D + \frac{R_F}{1+A}} \cdot i_{in}$$

Obtain expressions for the following:

a) Low-Frequency Transimpedance (v_{out}/i_{in}). Note, don't neglect the impact of R_D.

b) The TIA's two poles. Note, it's OK to neglect the transistor capacitors here.

$$V_{OUT} = -i_{in}\left(\frac{R_D R_F A}{R_D(1+A) + R_F}\right)$$

$$\boxed{R_T = \left(\frac{-R_D R_F}{R_D + \frac{R_F}{1+A}}\right)\left(\frac{A}{1+A}\right)}$$

Input pole: $\omega_1 = \frac{g_{m1}}{C_1}$

Output pole: $\omega_2 = \frac{1}{\left(R_D \parallel \frac{R_F}{1+A}\right) C_2}$

c) Now assume that R_D is relatively large. What does the low-frequency transimpedance expression simplify to? What benefit does this topology offer over just using an input feedback TIA?

w/ large R_D: $R_T = \left(\frac{-R_D R_F}{R_D + \frac{R_F}{1+A}}\right)\left(\frac{A}{1+A}\right) \Rightarrow \boxed{-R_F\left(\frac{A}{1+A}\right)}$

This is the same gain as a standard feedback TIA.

However, now we have the ability to set the input pole w/ g_{m1} without impacting the TIA stability.