Texas A&M University Department of Electrical and Computer Engineering

ECEN 620 - Network Theory (Broadband Circuit Design)

Fall 2023

Exam #2

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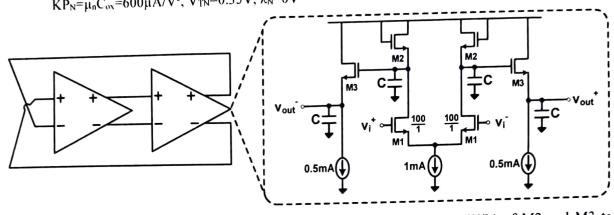
- Please write your name in the space provided below
- Please verify that there are 4 pages in your exam
- You may use one double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		50
2		50
Total		100

Name:	SAM	PALEKMO		
UIN:				

A differential ring oscillator is shown below. Assume that all transistors are operating in saturation with $r_o = \infty$ and you can ignore any transistor device capacitors. Assume that C=100fF and use the following NMOS parameters

 $KP_{N}{=}\mu_{n}C_{ox}{=}600\mu A/V^{2},\,V_{TN}{=}0.35V,\,\lambda_{N}{=}0V^{-1}$



- a) Assume that for M2 and M3 that $W_2/L_2 = W_3/L_3$. Determine the sizes (W/L) of M2 and M3 to achieve oscillation. b. Wose = 7
- What is the oscillation frequency?

a. Each oscillator cell:
$$\frac{g_{m2}}{1 + \frac{sc}{g_{m2}}} = \frac{\sqrt{K^{\rho}(\frac{y}{L})_{2}^{2}}}{1 + \frac{sc}{g_{m3}}} = \frac{\sqrt{K^{\rho}(\frac{y}{L})_{2}^{2}}}{100\rho F}$$

$$100\rho F$$

=38.76 rad/s = 6.176H=

$$H(S) = \begin{bmatrix} \frac{9m_1}{g_{n2}} \\ \frac{1}{1 + \frac{SC}{g_{n2}}} \end{bmatrix}^2 \begin{bmatrix} \frac{1}{1 + \frac{SC}{g_{n3}}} \\ \frac{1}{1 + \frac{SC}{g_{n3}}} \end{bmatrix}^2$$

To oscillate each cell should contribute a phase shift of

$$\frac{360^{\circ}-180^{\circ}}{2}=90^{\circ}$$

Since $\left(\frac{\omega}{L}\right)_2 = \left(\frac{\omega}{L}\right)_3$ and $I_2 = I_3 \Rightarrow g_{m2} = g_{m3}$. Thus, each cell has

2 poles that are both at - 9m2

=> (!realt will oscillate when each pole gives 45, which is W2/L2=W3/L3=

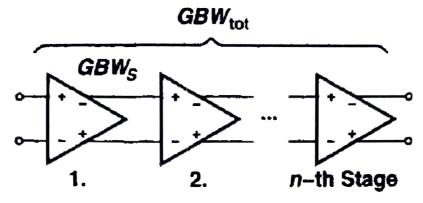
$$Wos_{L} = Wp = \frac{9m_{Z}}{c}$$

$$A_{r} Wos_{L} + he gain is \frac{gn_{I}}{gm_{Z}} \left(\frac{1}{\sqrt{2}}\right) \left(\frac{1}{\sqrt{2}}\right) = \frac{9m_{I}}{29m_{Z}} \quad \text{which reads to equal } I,$$

$$\frac{9m_{I}}{27m_{L}} = \frac{1}{27KP(4D_{L}2I_{D})} = \frac{1}{2}\sqrt{\frac{W_{I}}{W_{I}}} = 1 \Rightarrow \left(\frac{W}{L}\right)_{Z} = \frac{25}{4}$$

Problem 2 (50 points)

Assume that the limiting amplifier below consists of cascaded identical single-pole amplifier stages, with gain A_{vs} and bandwidth ω_{3dBs} .



a) Design the limiting amplifier to achieve a 34dB total gain and 20GHz total bandwidth with the minimum per-stage gain-bandwidth product. Give the stage number and the per-stage gain and bandwidth. Also compute the per-stage gain-bandwidth product.

$$N_{0}pt = 2\ln(6+0+) = 2\ln(50.1) = 7.83 \Rightarrow v_{se} 8 \text{ stages}$$

$$W_{0} = 8 \quad A_{vs} = \sqrt[8]{50.1} = 1.63$$

$$W_{3}18_{1} + W_{3}28_{1} = \sqrt{2^{1/8} - 1} \Rightarrow W_{3}28_{5} = \frac{W_{3}28_{1}}{12^{1/5} - 1} = \frac{2\pi(206Hz)}{\sqrt{2^{1/8} - 1}} = 4176ra^{1/5}$$

$$G_{0}BU_{5} = (1, 63)(4176ra^{1/5}) = 6806rad/5 = 108GHz$$

$$n = 8$$

$$A_{vs} = 1.63$$

$$\omega_{3dBs} = 4176rad/5$$

$$(66,56t)$$

b) Assume that the simple differential amplifier stage shown below can only achieve a maximum GBW_s=70GHz. Propose a change to the stage design below to achieve the required GBW_s from part (a).

