Texas A&M University
Department of Electrical and Computer Engineering

ECEN 620 – Network Theory (Broadband Circuit Design)

Fall 2022

Exam #1

Instructor: Sam Palermo

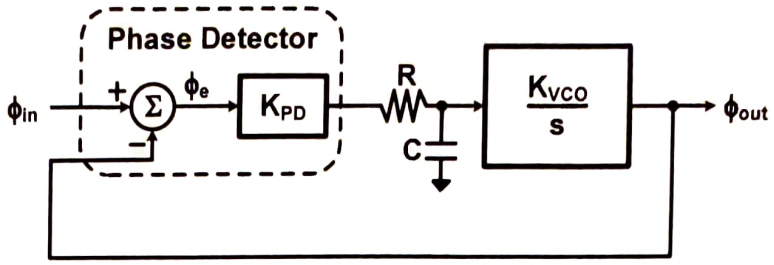
- Please write your name in the space provided below
- Please verify that there are **6** pages in your exam
- You may use <u>one</u> double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		50
2		50
Total		**100**

Name: SAM PALERMO

UIN: _____

Problem 1 (50 points)
For the PLL block diagram shown below, assume that the phase detector gain is K_{PD} and the VCO gain is K_{VCO}.



a) Find the expressions for the open loop gain, LG(s), the closed-loop transfer function $H(s)=\phi_{out}(s)/\phi_{in}(s)$, and the phase error transfer function, $E(s)=\phi_e(s)/\phi_{in}(s)$. (30 points)

$$LG(s) = \frac{K_{PD}K_{VCO}F(s)}{s} \quad \text{where} \quad F(s) = \frac{1}{1+sRC}$$

$$LG(s) = \frac{K_{PD}K_{VCO}/(RC)}{s(s+\frac{1}{RC})}$$

$$H(s) = \frac{LG(s)}{1+LG(s)} = \frac{K_{PD}K_{VCO}/(RC)}{s^2+\frac{s}{RC}+\frac{K_{PD}K_{VCO}}{RC}}$$

$$E(s) = \frac{1}{1+LG(s)} = \frac{s(s+1/RC)}{s^2+\frac{s}{RC}+\frac{K_{PD}K_{VCO}}{RC}}$$

LG(s) =

$H(s)=\phi_{out}(s)/\phi_{in}(s)=$

$E(s)=\phi_e(s)/\phi_{in}(s)=$

b) Assume that $K_{PD}=2/\pi$ and R=1kΩ. Give the values of K_{VCO} and the loop filter capacitor C for a ζ=1 and steady-state phase error of (π/10) rad. with a 1Mrad/s frequency step. (10 points)

For steady-state phase error w/ freq step

$$\phi_{e,ss} = \lim_{s\to 0}\left(\frac{\Delta\omega}{s^2}\right)\left(sE(s)\right) = \frac{\Delta\omega}{s^2}\,\frac{s^2\left(s+\frac{1}{RC}\right)}{s^2+\frac{s}{RC}+\frac{K_{PD}K_{VCO}}{RC}} = \frac{\Delta\omega}{K_{PD}K_{VCO}}$$

$$K_{VCO} = \frac{\Delta\omega}{K_{PD}\phi_{e,ss}} = \frac{1M\ rad/s}{\left(\frac{2}{\pi}\right)\left(\frac{\pi}{10}\right)} = 5M\ rad/s$$

For $\zeta=1 \Rightarrow$ From H(s) denominator $2\zeta\omega_n = \frac{1}{RC}$ and $\omega_n^2 = \frac{K_{PD}K_{VCO}}{RC}$

$$2\zeta\sqrt{\frac{K_{PD}K_{VCO}}{RC}} = \frac{1}{RC} \Rightarrow C = \frac{1}{(2\zeta)^2 K_{PD}K_{VCO}R} = \frac{1}{(2\cdot1)^2\left(\frac{2}{\pi}\right)(5M)(1K)} = 78.5pF$$

$K_{VCO} = 5M\ rad/s\ V$

$C = 78.5pF$

c) Now assume that K_{VCO} is modified to improve the steady-state phase error to (π/100) rad. with a 1Mrad/s frequency step. Using the same R and C numerical values from part(b), what is the new ζ? (5 points)

For $\frac{\pi}{100}$ phase error $\Rightarrow K_{VCO,new} = 10\cdot K_{VCO,old}$

$$\zeta_{,NEW} = \left(\frac{1}{2}\right)\left(\frac{1}{\sqrt{K_{PD}K_{VCO}RC}}\right) = \frac{\zeta_{,OLD}}{\sqrt{10}} = \frac{1}{\sqrt{10}} = 0.316$$

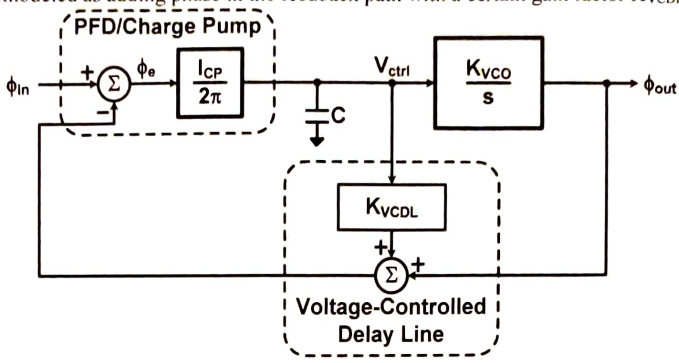
$\zeta = 0.316$

d) Qualitatively comment on how the accuracy of the steady-state phase error with a frequency step impacts the PLL stability. (5 points)

If the PLL is designed with a smaller steady-state phase error the stability will be worse (lower ζ) if the loop filter is not adjusted by increasing its bandwidth.

Problem 2 (50 points)

This problem analyzes a PLL with a voltage-controlled delay line (VCDL) in the feedback path. The VCDL can be modeled as adding phase in the feedback path with a certain gain factor K_{VCDL} (rad/V).



a) Find the expressions for the open loop gain, LG(s), the phase error transfer function, $E(s)=\phi_e(s)/\phi_{in}(s)$, and the closed-loop transfer function $H(s)=\phi_{out}(s)/\phi_{in}(s)$. (25 points)

$$LG(s) = \frac{I_{CP}}{2\pi}\left(\frac{1}{sC}\right)\left[\frac{K_{VCO}}{s} + K_{VCDL}\right] = \frac{\frac{I_{CP}K_{VCDL}}{2\pi C}\left[s + \frac{K_{VCO}}{K_{VCDL}}\right]}{s^2}$$

$$E(s) = \frac{1}{1+LG(s)} = \frac{s^2}{s^2 + \frac{I_{CP}K_{VCDL}}{2\pi C}s + \frac{I_{CP}K_{VCO}}{2\pi C}}$$

$$H(s) = \frac{\frac{I_{CP}}{2\pi}\left(\frac{1}{sC}\right)\left(\frac{K_{VCO}}{s}\right)}{1+LG(s)} = \frac{\frac{I_{CP}K_{VCO}}{2\pi C}}{s^2 + \frac{I_{CP}K_{VCDL}}{2\pi C}s + \frac{I_{CP}K_{VCO}}{2\pi C}}$$

LG(s) =

$E(s)=\phi_e(s)/\phi_{in}(s)=$

$H(s)=\phi_{out}(s)/\phi_{in}(s)=$

b) Assume that K_{PD}=10μA/(2π), K_{VCO}=100Mrad/(sV), and K_{VCDL}=10rad/V. Find the value of the loop filter capacitor C for a 45° phase margin. (20 points)

$$PM = \angle LG(j\omega_u) - (-180^\circ) = 45^\circ$$

$$\tan^{-1}\left(\frac{\omega_u K_{VCDL}}{K_{VCO}}\right) - 180^\circ + 180^\circ = 45^\circ$$

$$\omega_u = \frac{K_{VCO}}{K_{VCDL}} \tan(45^\circ) = \frac{100M\,rad/sV}{10\,rad/V} = 10^7\,rad/s$$

$$|LG(j\omega_u)|^2 = 1$$

$$\frac{\frac{I_{CP} K_{VCDL}}{2\pi C}\sqrt{\omega_u^2 + \left(\frac{K_{VCO}}{K_{VCDL}}\right)^2}}{\omega_u^2} = \frac{\frac{10\mu A\,(10^7\,rad/s)}{2\pi C}\left(\sqrt{2}\cdot 10^7\right)}{(10^7)^2} = 1$$

$$C = \frac{(10\mu A)(10^7\,rad/s)(\sqrt{2})}{2\pi(10^7)} = 2.25pF$$

C= 2.25pF

c) Qualitatively comment on the main differences between this PLL with a VCDL in the feedback path and the conventional charge-pump PLL with a series RC loop filter. Which architecture provides more filtering to high-frequency input phase noise? (5 points)

For the design with the VCDL in the feedback, the proportional term appears in the feedback. Thus, the open-loop gain and phase error are similar, but the closed-loop output transfer function doesn't have a zero. Thus, the VCDL design will filter high-frequency input phase noise by -40dB/dec, while the conventional design will filter by -20dB/dec.