# Texas A&M University Department of Electrical and Computer Engineering

# ECEN 620 - Network Theory (Broadband Circuit Design)

## Fall 2023

## Exam #1

Instructor: Sam Palermo

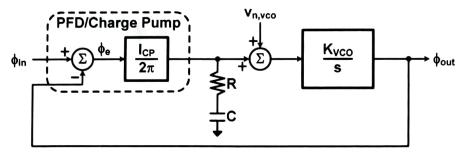
- Please write your name in the space provided below
- Please verify that there are 6 pages in your exam
- You may use one double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		50
2		50
Total		100

Name:	SAM	PALERMO	
UIN:			

#### Problem 1 (50 points)

This problem investigates how voltage noise on the VCO control voltage impacts the output phase noise. Assume that the VCO input noise is modeled as an additive voltage noise term, as shown in the model below.



a) Find the expression for the input VCO voltage noise induced phase noise transfer function,  $T(s) = \phi_{out}(s)/v_{n,vco}(s)$ .

b) Assume that the PLL has been designed for  $\omega_n$ =1Mrad/s and  $\zeta$ =0.7. Also, assume that  $\omega_{VCO}$ =10Grad/s and  $K_{VCO}$ =2 $\pi$ \*1GHz/V. If the VCO input voltage noise has sinusoidal modulation  $v_{n,vco}(t) = V_{amp} \sin(10^8 t)$  (V)

What is the maximum voltage amplitude, V<sub>amp</sub>, for an output jitter amplitude of 0.5ps?

$$\frac{P_{\text{out}}}{V_{1/V_{10}}} \left(\frac{10^8}{10^8}\right) = \frac{\left(2\pi \cdot 16Hz/V\right) \left(\frac{10^8 \text{ ray}}{10^8 \text{ ray}}\right)}{-10^{16/104/5}^2 + 2(0.7) \left(10^6 \text{ ray}\right)^2 + 10^{12/(104/5)^2}}$$

$$\frac{P_{\text{out}}}{V_{1/V_{10}}} \left(\frac{10^8 \text{ ray}}{V_{10}}\right) = 62.8 \text{ ray}/V$$

$$\frac{P_{\text{out}}}{V_{1/V_{10}}} \left(\frac{10^8 \text{ ray}}{V_{10}}\right) \left(\frac{2\pi \cdot 100ps}{V_{10}}\right) = 6.5ps$$

$$V_{\text{amp}} = 79.6 \text{ ps}$$

Vamp = 79.6 mV

c) Assuming 10<sup>4</sup> rad/s sinusoidal noise with a 10mV amplitude, what is the output jitter amplitude in ps?

$$\left| \frac{\varphi_{0J} + (10^4)}{V_{N_1} V CO} \right| = \frac{(2\pi \cdot 16^{42} V)(10^4 \cdot 10^4)}{10^{12} (rad/s)^2} = 62.8 \, vad/v$$

$$(62.8^{r=2} V)(10^{m} V) = 0.628 \, rad$$

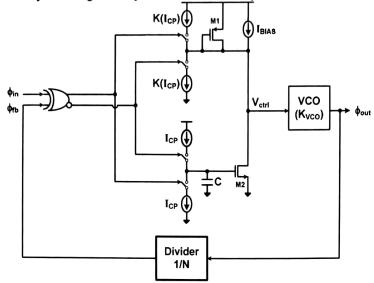
$$(62.8^{r=2} V)(10^{m} V) = 0.628 \, rad$$

$$(63.628 \, rad) \left( \frac{2\pi (roops)}{2\pi rad} \right) = 62.8 \, ps$$

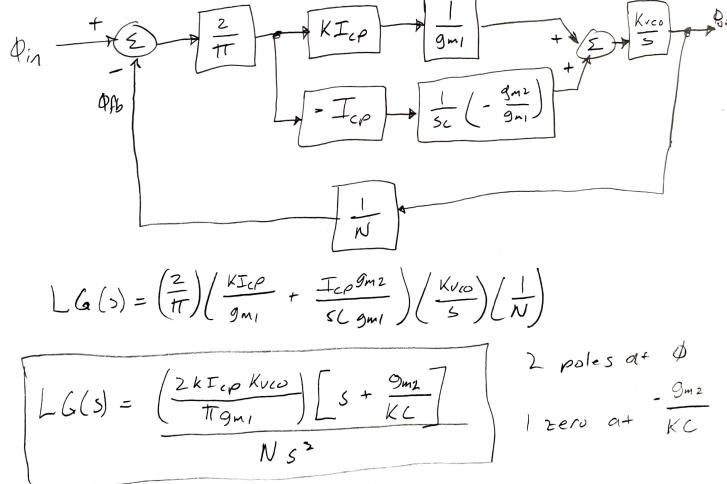
Output Jitter Amplitude (ps) = 62,8ps

#### Problem 2 (50 points)

For the PLL shown below, assume that the VCO gain is  $K_{VCO}$  is positive, all transistors are operating in saturation with  $r_0=\infty$  and you can ignore any transistor device capacitors.



- a) Draw the phase domain small signal model of the loop.
- b) Find the expressions for the loop gain, LG(s), and determine the pole-zero locations of LG(s).



c) Assume that K=5, C=200pF, g<sub>m1</sub>=gm<sub>2</sub>=2mA/V, K<sub>VCO</sub>=2π\*(1GHz/V), N=64. Calculate the unit charge pump current, I<sub>CP</sub>, for a phase margin of 45°.

$$LG(s) = \left(\frac{2k L_0 k_0}{T lg_{Ml}}\right) \left[s + \frac{9m^2}{kC}\right]$$

$$Ns^2$$

$$0 = 180^\circ + 4m^* \left(\frac{10 k_0}{g_{M2}}\right) - 10^\circ = 4m^* \left(\frac{10 k_0}{g_{M2}}\right)$$

$$= 180^\circ + 4m^* \left(\frac{10 k_0}{g_{M2}}\right) - 10^\circ = 4m^* \left(\frac{10 k_0}{g_{M2}}\right)$$

$$\frac{1}{2k^2} \left(\frac{10 k_0}{g_{M2}}\right) = 45^\circ$$

$$1 = 180^\circ + 4m^* \left(\frac{10 k_0}{g_{M2}}\right) = 45^\circ$$

$$\frac{1}{2k^2} \left(\frac{10 k_0}{g_{M2}}\right) = \frac{2m^2 k_0}{5} = 2 \times 10^{\frac{5}{2}} \cdot \frac{10 k_0}{5}$$

$$\frac{1}{2k^2} \left(\frac{10 k_0}{g_{M2}}\right) = \frac{2m^2 k_0}{5} = \frac{2 \times 10^{\frac{5}{2}} \cdot \frac{10 k_0}{5}}{5}$$

$$\frac{1}{2k^2} \left(\frac{10 k_0}{g_{M2}}\right) = \frac{2 \times 10^{\frac{5}{2}} \cdot \frac{10 k_0}{5}}{5} = \frac{2$$

$$I_{cp} = \frac{64(2\times10^6)(2-)}{2(5)(2^4/6)\sqrt{2}} = 9.05 \text{ nA}$$

 $I_{CP}$  for 45° Phase Margin = 9.0 Ju A

d) What is the phase relationship between  $\phi_m$  and  $\phi_m$  when is PLL locked?

$$\phi_{in} - \phi_{fb} = Q_i O^{ij}$$