A 1.8V, Sub-mW, Over 100% Locking Range, Divide-by-3 and 7 Complementary-Injection-Locked 4 GHz Frequency Divider

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Abstract- **A low-power wideband divide-by-odd-ratio ring-oscillator-based complementary-injection-locked frequency divider (CILFD) is proposed. The multiple-input complementary-injection scheme widens its locking range over 100% to sufficiently cover the PVT variations. The CILFD consumes dynamic power only with no additional power penalty for larger division ratios. The differential input and output are realized employing auxiliary cross-connected inverters. The CILFDs with division ratios of 3 and 7 are implemented in a 0.18 µm CMOS technology. The measurement results show a locking range from 1.4 to 4.4 GHz with an input incident power of -4 dBm. The power consumption while locked at 4.7 GHz is 0.9 mW from a single 1.8-V power supply.**

I. Introduction

Frequency dividers (FDs) are a basic but critical building block for phase-locked loops (PLLs) in various high-speed wireline and wireless communication systems. In addition to frequency transition, FDs may have to provide various division moduli and multiple phases. Conventional flip-flop-based FDs are robust and broadband but their power budget is excessive especially for high-speed operations. Injection-locked frequency dividers (ILFDs) [1], [2] are a low-power alternative for applications in the range of several tens of gigahertz. LC-based ILFDs (LC-ILFDs) can operate at very high speed [3], [4] and they have optimal noise performance due to their bandpass LC filtering characteristic. However, the area penalty is significant due to the inductor used; furthermore, the division ratio cannot be large within one LC tank load. Small division ratio implies that several LC-ILFDs are needed for converting very high frequency down to the desired frequency. Also, the low quality factor Q of the LC tank to widen the locking range costs additional power consumption. Even if a low-Q LC tank can be used, the locking range usually cannot cover the PVT variations, thus some additional control or feedback circuits are required to adjust the free running frequency to ensure the LC-ILFDs locked. These expensive and complicated controls make the LC-ILFDs unfavorable for practical applications.

Ring-oscillator-based ILFDs (Ring-ILFDs) feature wider locking ranges, smaller silicon area and larger division moduli [5]-[8]. Ring-ILFDs' operation frequencies are mainly determined by the dimension of the devices and the power consumption. Although the phase noise of the conventional ring-oscillator is poor, the noise performance of ring-ILFDs can be further improved by injecting a clean signal [9]. In order to widen the locking range, to overcome PVT variations, the multiple-input injection technique for Ring-ILFDs with even division ratios has been proposed [6], [7]. However, the locking range of Ring-ILFDs with odd division ratios can rarely overcome the PVT variations. Usually when the number of ring-oscillator stages increases, the locking range shrinks drastically [10]. Since large division ratios can relax the speed and power in the following building blocks, to widen the locking range of large odd-division-moduli Ring-ILFDs is still desired.

In this paper, a new ring-oscillator-based complementary-injection-locked frequency divider (CILFD) is presented. The multiple-input complementary-injection achieves large odd division ratios and wide enough locking range to overcome the process variations without tuning the free running frequency. The power consumption overhead is negligible for larger division modulus. The CILFDs provide differential outputs due to the cross-connected inverters.

II. Circuit Architecture And Analysis

A. Circuit Architecture and Model

Fig. 1 shows the proposed divide-by 3 complementary-injection-locked frequency divider. The divide-by-(2n+1) CILFD can be realized by using (2n+1) ring-oscillator stages (n is a prime number). Every ring-oscillator stage (delay cell) has an upper tail-injection transistor, $M_{TP,n}$, and a bottom-injection transistor, $M_{TN,n}$. The inverter, $M_{P,n}$ and $M_{N,n}$, is placed between the upper and bottom tail transistors. The free-running frequency of the ring-oscillator is controlled through the DC bias voltage at the gate terminals of tail transistors. Increasing the |Vgs| of tail transistors draws more tail current and hence reduces the delay of each ring-oscillator stage to increase the oscillating frequency. The injection signal is coupled by the capacitors connected to the gate terminals of the tail transistors.

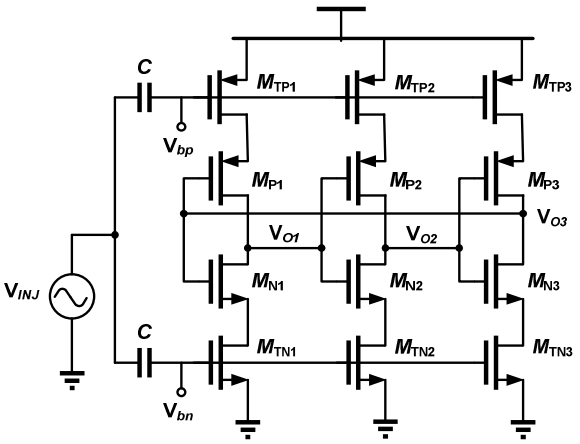


Fig. 1. Divide-by-3 complementary injection-locked frequency divider

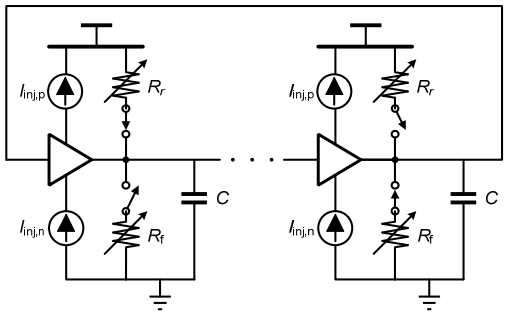


Fig. 2. Simplified circuit model of a CILFD

The conceptual circuit model of a divide-by-(2n+1) CILFD is shown in Fig. 2. Each ring-oscillator stage consists of a transconductor, an effective current-controlled resistor R_f that discharges the load capacitor C and an effective R_r that charges the load capacitor. In order to simplify the analysis, the time-variant characteristic of R_r and R_f is ignored. Instead, R_r and R_f stand for the effective time-average resistance values during the rising and falling transitions; this approximation allows us to obtain simpler expression for propagation delay computations. $I_{inj,n}$ and $I_{inj,p}$ represent the injection currents from a bottom NMOS tail transistor and an upper PMOS tail transistor, respectively. The injection through NMOS and PMOS is named complementary injection. Notice that the equivalent values of R_r and R_f vary with the tail currents. If the loop gain satisfies the Barkhausen criteria, the free-running frequency of the (2n+1)-stages ring-oscillator can be approximated as

$$f_{osc} \cong 1/[(2n+1)(t_{pdr}+t_{pdf})], \qquad (1)$$

where t_{pdr} and t_{pdf} are the rising and falling propagation delays and can be modeled as R_rC and R_fC, respectively.

While the signal is injected, it produces both amplitude and phase variations at the outputs of CILFD and alters the load impedance of each stage. If the negative-feedback loop is able to reach steady state, the CILFD will be locked to a sub-harmonic of the injection signal. Since the division ratio is usually the same as the number of ring-oscillator stages, an equal phase shift Φ exists between each inverter and its tail transistor. If I_T is defined as the tail current in free-running state, I_{INJ} as the current drawn by the injection signal and I_{OSC} as the effective tail current while the system is locked. The phase shift Φ can increase or decrease the effective upper or bottom tail currents as shown in the Fig. 3. The variation of the effective tail currents changes the effective R_r and R_f, or equivalently the rising and falling propagation delay to meet the injection frequency. Intuitively, the boundaries of locking range can be obtained from the geometrical interpretation. The existing smallest and largest phase shifts determine the maximum and minimum locking oscillation frequencies, respectively. Fig. 3 also illustrates how increasing the ratio of I_{INJ} to I_T widens the percentage of locking range. Since the amplitude of injection signal is limited, a proper selection of I_T optimizes the tradeoff between the locking range and operating frequency. Due to the characteristic of ultra-wide

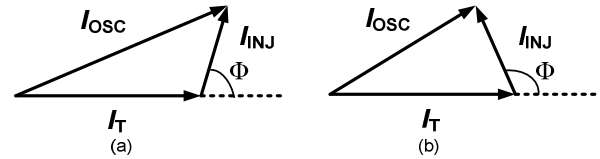


Fig. 3. Geometrical interpretation of complementary injection. A phase shift (a) to increase oscillation frequency (b) to decrease oscillation frequency.

locking range, the CILFD is able to cover PVT variations with a small I_{INJ} to save power on the buffer stages.

In order to realize a differential-input and output CILFD structure and to take full advantage of the differential nature of LC VCOs, auxiliary cross-connected inverter pairs are used to couple two CILFDs as shown in the Fig. 4. The cross-connected inverters provide current injection to each other to vary the phases and force the two CILFD outputs to stay out of phase during steady state conditions.

B. Complementary and Multiple-input Injection

The CILFDs' wide locking range is a result of the use of complementary and multiple-input signal injection. The N-and-P complementary-injection scheme not only increases the effect of the injected signal into the ring-oscillator but also simultaneously drives both the rising and falling propagation delays, unlike the conventional injection mechanisms that vary the falling propagation delays only [10]-[11]. Therefore, the complementary injection offers the advantages of more control on the ring-oscillator oscillation frequency and wider locking range. Simulations results for a divide-by-7 CILFD are shown in Fig. 5; notice that the injection currents complement each other and occur only during rising and falling transitions.

The combination of the complementary injection and multiple-input injection points avoids the interference from stage to stage, attenuates the injection signal at the unwanted timings, blocks the crosstalk between upper and bottom tail transistors, and allows us to control both transition times t_{pdr} and t_{pdf}. As a result, wider locking range is achieved even in the case of large-division-ratios CILFDs.

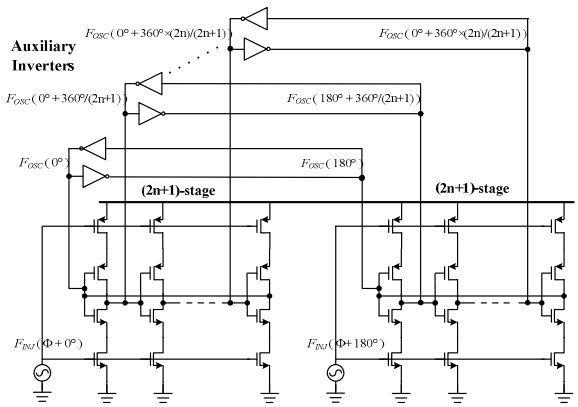


Fig. 4. A divide-by-(2n+1) differential complementary-injection-locked frequency divider

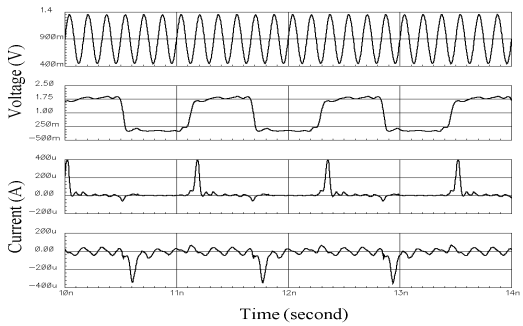


Fig. 5. Simulated waveforms from top to bottom (a) injection signal, (b) voltage in one of the nodes of the ring-oscillator, (c) NMOS tail transistor current, (d) PMOS tail transistor current.

C. Power Consumption and Phase Noise Performance

The CILFD consumes dynamic power only due to the nature of the complementary injection locking scheme. The power consumption of a single ring-oscillator stage under locking with a divide-by-(2n+1) ratio can be approximated as

$$P_{stage} \cong 2CV_{DD}^2 f_{inj} / (2n+1) . \quad (2)$$

Equation (2) multiplied by the number of ring-oscillator stages gives the total power consumption of the CILFD:

$$P_{total} \cong 2CV_{DD}^2 f_{inj} . \quad (3)$$

Expression (3) shows that the power consumption of the CILFD is independent of its division ratio (the number of ring-oscillator stages) but proportional to the frequency of the injected signal. The CILFDs are then favorable for the use of large division ratios.

It is well known that the ring-oscillators present poor phase noise due to their inherent low-Q of each stage. However, Ring-ILFDs' internal stages phase noise is high-pass filtered by the loop dynamics. When locked, the phase noise of Ring-ILFDs is mainly determined by the phase noise of the injection signal [9]. The phase noise of a CILFD can then be approximated as

$$PN(ILFD) \cong PN(Injection) - 10\log(2n+1)^2 . \quad (4)$$

This equation fits well with the simulated phase noise of a modulus-7 CILFD shown in Fig. 5. The phase noise under free running condition is -97 dBc/Hz at 1MHz frequency offset. Locked by an injection signal generated from a 6-GHz LC VCO with a phase noise of -112 dBc/Hz at 1MHz offset frequency, the modulus-7 CILFD shows a phase noise of -130 dBc/Hz at 1MHz offset.

III. Test Chip and Mesurement Results

Two differential CILFDs with division moduli of three and seven were implemented in a standard TSMC 0.18-µm technology. Two-stage buffers are used for driving the 50-Ω external loads. Fig. 7 shows the microphotogragh of the CILFDs and their buffer stages. The chip area is 1×1 mm^2 including all testing pads; the core of the divide-by-3 and divide-by-7 CILFDs occupies 40×120 µm^2 and 90×120 µm^2, respectively.

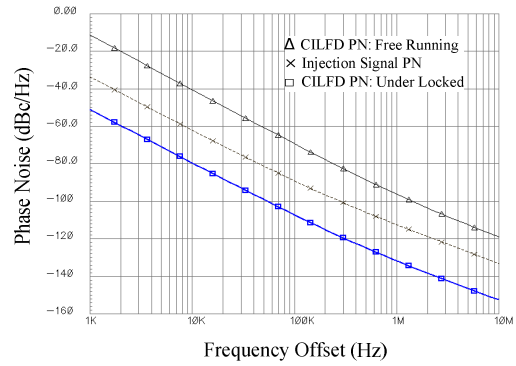


Fig. 6. Simulated phase noise. From top to bottom (a) free running CILFD, (b) injection signal, and (c) locked CILFD

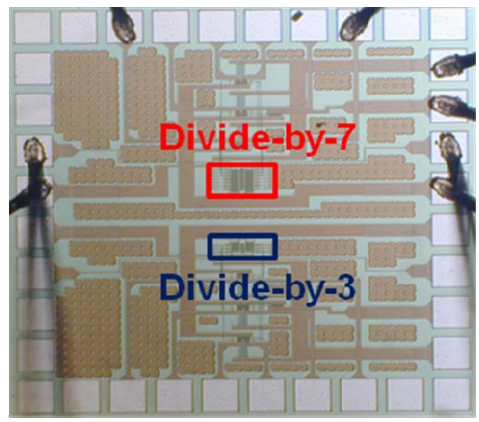


Fig. 7. Micorphotograph of the fabricated CILFDs

The measured average free-running frequency of the divide-by-3 and divide-by-7 CILFDs is 1.15 GHz and 540 MHz, around 10% below the simulated values. The injection signal is generated from a HP 8673C synthesized signal generator. Fig. 8 shows the output spectrum of the divide-by-7 CILFD locked by an input frequency of 1.4 GHz. The output frequency of the CILFD is center at 200MHz. When the CILFD is locked, the output signal tone is much sharper and the skirt of the output signal tone in free-running oscillation state is eliminated.

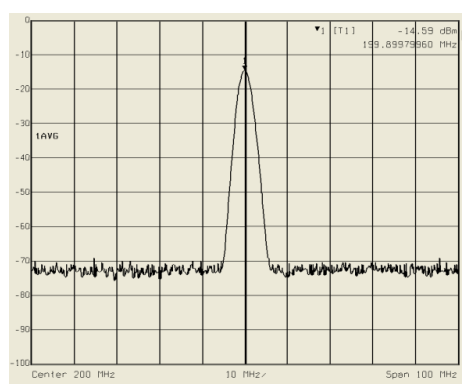
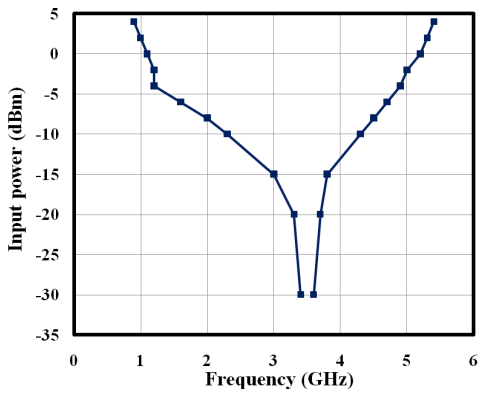
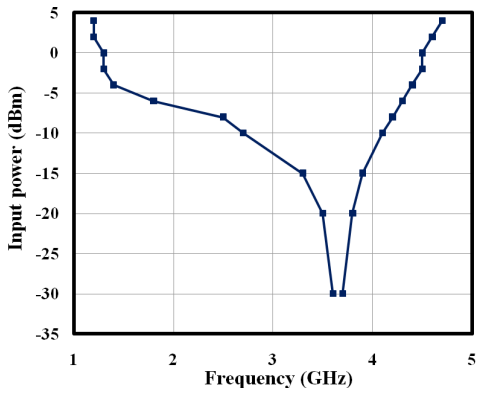


Fig. 8. Measured output spectrum of a divide-by-7 CILFD locked by a 1.4 GHz input frequency



(a)



(b)

Fig. 9. Measured input sensitivity curves of (a) divide-by-7 and (b) divide-by-3 CILFDs

The measured input sensitivity curves of divide-by-3 and divide-by-7 CILFDs are shown in Fig. 9. With an input injection power of -4 dBm, the measured locking range of the divide-by-3 CILFD spans approximately from 1.2 to 4.9 GHz, while the frequency locking range of the divide-by-7 CILFD spans from 1.4 to 4.4 GHz. The measured locking ranges are around 20 % smaller than the ones predicted by schematic simulations. The power consumption of the divide-by-3 and divide-by-7 CILFDs locked by an input frequency of 4.5 GHz is 0.74 and 0.88 mW, respectively. The performance of the measured CILFDs is summarized in Table 1. Table 2 presents a comparison of this work with previously published Ring-ILFDs.

TABLE 1
SUMMARY OF MEASURED PERFORMANCE

	Divide-by-3	Divide-by-7
Free Running Frequency	1.15 GHz	540 MHz
Locking Range @ -4 dBm Input Power	1.2 ~ 4.9 GHz	1.4 ~ 4.4 GHz
Power Consumption @4.5 GHz Input Frequency	0.74 mW	0.88 mW
Power Consumption @1.5 GHz Input Frequency	0.31 mW	0.36 mW
Core Area	40 × 120 μm^2	90 × 120 μm^2

TABLE 2
PERFORMANCE COMPARISON WITH EXISTING WORKS

Ref	Techno -logy	Div. Ratio	Input Power (dBm)	Locking Range (GHz)	Power (mW)
This Work	0.18µm CMOS	3 7	-4	1.2 ~ 4.9 1.4 ~ 4.4	0.74 0.88
[6]	0.18µm CMOS	2 4	0	15 ~ 22 37.4 ~ 38.6	24
[7]	0.13µm CMOS	2 6	NA	0.05 ~ 1.65 0.25 ~ 1.22	0.9 2.7
[8]	0.18µm CMOS	8	3	9.2 ~ 12.3	3.6

IV. CONCLUSION

A robust wideband odd-division-ratio complementary-injection-locked frequency divider has been described. The complementary injection scheme widens the locking range for large division-modulus operations. A 120% locking range from 1.1 to 4.7 GHz has been experimentally demonstrated in a 0.18µm CMOS technology divide-by-7 CILFD while dissipating a maximum power of 0.9mW. The proposed CILFD can be used for various applications such as PLLs, CDRs, and time-to-digital converter circuits.

ACKNOWLEDGMENTS

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