A Low-Noise Wide-BW 3.6-GHz Digital $\Delta\Sigma$ Fractional-N Frequency Synthesizer With a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation

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***Abstract*—A 3.6-GHz digital fractional-N frequency synthesizer achieving low noise and 500-kHz bandwidth is presented. This architecture uses a gated-ring-oscillator time-to-digital converter (TDC) with 6-ps raw resolution and first-order shaping of its quantization noise along with digital quantization noise cancellation to achieve integrated phase noise of less than 300 fs (1 kHz to 40 MHz). The synthesizer includes two 10-bit 50-MHz passive digital-to-analog converters for digital control of the oscillator and an asynchronous frequency divider that avoids divide-value delay variation at its output. Implemented in a 0.13-μm CMOS process, the prototype occupies 0.95-mm^2 active area and dissipates 39 mW for the core parts with another 8 mW for the oscillator output buffer. Measured phase noise at 3.67 GHz carrier frequency is -108 and -150 dBc/Hz at 400 kHz and 20 MHz offset, respectively.**

***Index Terms*—Digital-to-analog converter (DAC), divider, fractional-N, frequency synthesizer, gated ring oscillator (GRO), noise shaping, phase-locked loop (PLL), time-to-digital converter (TDC), $\Delta\Sigma$.**

I. Introduction

DIGITAL phase-locked loops (PLL) have recently emerged as an attractive alternative to the more traditional analog PLL, with recent results demonstrating that digital frequency synthesizers with GSM level noise performance can be achieved [1]. As shown in Fig. 1, one of the key advantages of digital PLLs over their analog counterparts is that they remove the need for large capacitors within the loop filter by utilizing digital circuits to achieve the desired filtering function. The resulting area savings are critical for achieving a low-cost solution, and the overall PLL implementation is more readily scaled down in size as new fabrication processes are utilized. Also, by avoiding analog-intensive components such as charge pumps, a much more attractive "mostly" digital design flow is achieved.

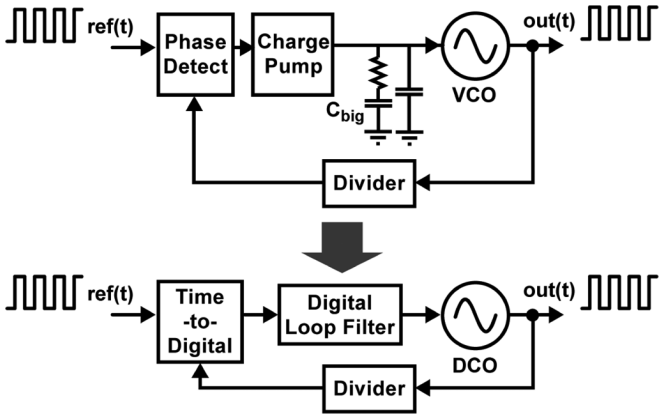

Fig. 1. Progression from analog to digital PLL implementation.

While the benefits of a digital PLL approach are obvious to many, there remain basic questions regarding their achievable performance. In particular, can such structures achieve low jitter comparable to analog approaches? Can high PLL bandwidth be achieved to more easily support wide bandwidth modulation and fast settling? Can traditional voltage-controlled oscillators (VCO) be efficiently leveraged in such systems?

In this paper, we attempt to address the above questions by presenting a wide-bandwidth, low-jitter digital synthesizer prototype which leverages a hybrid LC VCO [2] in its implementation. Hybrid VCOs, which leverage a switched capacitor array for frequency band selection and an analog varactor for fine tuning, have become a popular choice in many recent PLLs due to their ability to achieve a wide tuning range with excellent phase noise.

As shown in Fig. 2, key components of the proposed structure are a high-resolution time-to-digital converter (TDC)-based on a gated ring oscillator (GRO) [3], a digital-to-analog converter (DAC) with a passive implementation to control the hybrid VCO through coarse and fine tuning paths, an all-digital quantization noise cancellation circuit, and an asynchronous divider structure that achieves low jitter with a low-power implementation. Measured results of the prototype demonstrate that $<$300 fs of jitter can be achieved with a PLL bandwidth of 500 kHz.

An overview of the paper is as follows. In Section II, we focus on the key issues involved in achieving low jitter with

Manuscript received April 07, 2008; revised July 21, 2008. Current version published December 10, 2008. This work was supported in part by C2S2, the Focus Center for Circuit and System Solutions, one of five centers funded under FCRP, an SRC program.

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Digital Object Identifier 10.1109/JSSC.2008.2005704

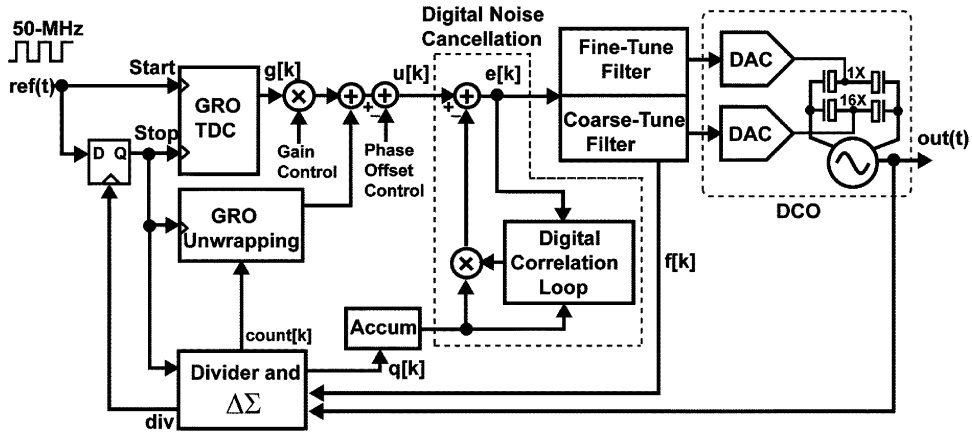

Fig. 2. Block diagram of proposed digital fractional-N frequency synthesizer.

high PLL bandwidth in digital PLL structures. Here we will see the need for a high-resolution TDC as well as quantization noise cancellation. In Section III, we will provide details of supporting blocks such as the DAC structures used for control of the VCO and the asynchronous divider. Section IV then focuses on system level issues associated with the coarse/fine tuning approach used to control the PLL frequency. Finally, Section V presents measured results of the system, and Section VI concludes.

II. Techniques for Achieving Low-Noise and Wide-Bandwidth

In this section, we investigate the challenges in achieving a low-noise, wide-bandwidth digital fractional-N synthesizer. We will show that the key challenges of attaining this goal lie in developing a high-resolution TDC and performing cancellation of the quantization noise caused by dithering of the divider. The proposed synthesizer architecture leverages a recently published noise-shaping GRO TDC [3], [4] to achieve the desired resolution, and introduces an all-digital approach to perform quantization noise cancellation.

A. Noise-Shaping TDC

Fig. 3 provides an intuitive view of the need for improved TDC resolution when a high PLL bandwidth is desired. As shown in the figure, the output phase noise of a digital synthesizer is primarily influenced by the quantization noise of the TDC and the phase noise of the digitally-controlled oscillator (DCO), where the DCO is realized as the combination of a DAC and hybrid VCO in our proposed system. As the figure shows, TDC noise is lowpass filtered by the PLL dynamics, whereas DCO noise is highpass-filtered. Therefore, while raising the PLL bandwidth has the benefit of suppressing DCO noise at low frequency offsets, it also carries the penalty of increasing the influence of TDC noise. As such, the combination of high bandwidth and low noise for the PLL demands high resolution of the TDC.

To provide a sense of the TDC resolution requirements when seeking a high-bandwidth fractional-N synthesizer, let us consider the example of striving for < -100 dBc/Hz in-band phase noise performance with a 500-kHz PLL bandwidth, 3.6-GHz

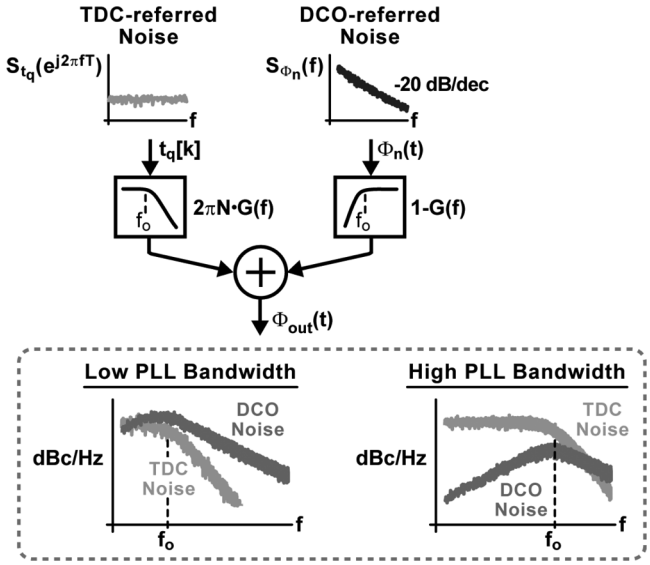

Fig. 3. Phase noise of narrow-BW and wide-BW digital PLLs.

output frequency, and 50-MHz reference frequency. If we assume that the quantization noise of the TDC is white, then the in-band phase noise floor of the PLL (PN) for a given TDC resolution $(T_{\rm res})$ is calculated as

$$PN = 10\log\left(1/T \cdot (2\pi \cdot N)^2 \cdot \left(1/12 \cdot T_{\rm res}^2\right)\right) \quad \text{(dBc/Hz)} \tag{1}$$

where T is the reference period (1/50 MHz) and N is the nominal divide value (3.6 GHz/50 MHz). Given the above expression, we calculate that 6-ps TDC resolution is necessary to achieve < -100 dBc/Hz in-band noise floor.

For a classical TDC structure [5], the TDC resolution corresponds to an inverter delay, and the goal of 6-ps resolution ends up being quite challenging. However, an alternative approach to obtain higher *effective* resolution is to pursue noise shaping of the TDC quantization noise and leverage the fact that the TDC output is lowpass filtered by the PLL such that the high frequency portion of that noise is removed.

Such noise shaping can be achieved by using a gated ring oscillator (GRO) topology for the TDC [6], as shown in Fig. 4. As the figure reveals, a GRO TDC measures the phase error

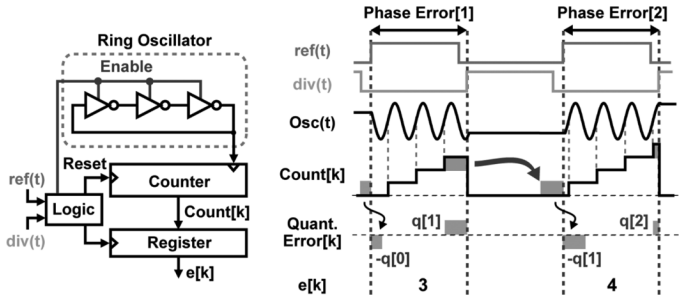

Fig. 4. Concept of a GRO TDC.

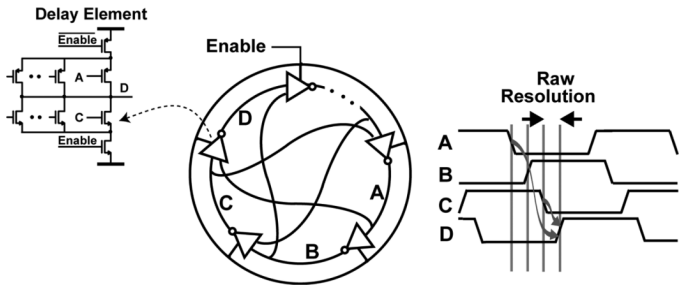

Fig. 5. Concept of a multipath gated ring oscillator TDC.

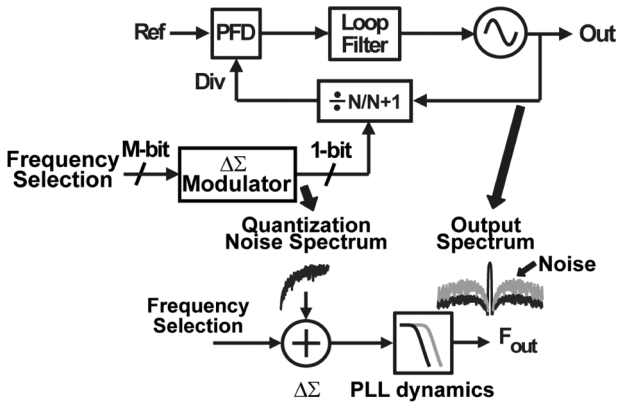

Fig. 6. Wider PLL bandwidth results in less quantization noise suppression.

between two signals by enabling a ring oscillator during the measurement window and counting the resulting transitions that occur in the oscillator. Between measurements, the GRO is disabled such that its internal state is kept intact. When the GRO is enabled in the next measurement, it ideally picks up where it left off such that the quantization error from the end of the previous measurement is directly related to the quantization error at the beginning of the current measurement. The overall quantization noise becomes

$$e[k] = q[k] - q[k-1] \tag{2}$$

where $q[k]$ denotes the *raw* quantization error at the end of each measurement. The first-order difference operation indicated by the above equation reveals that first-order shaping of the quantization noise is achieved with the GRO structure.

In practice, we note that we can count transitions in all of the oscillator stages [6] rather than just the output transitions as shown in Fig. 4. By doing so, the raw resolution corresponds to an inverter delay, which is similar to the case for the commonly used TDC described in [5]. The advantage of the GRO TDC is that the *effective* resolution is reduced well below an inverter delay by virtue of the noise shaping that it offers. Also, a subtle point is that mismatch between delay stages will be first order noise shaped due to the barrel-shifting action of the transitions through the ring oscillator structure, so that excellent linearity of the TDC can be achieved without the need for calibration [7].

To further improve the GRO resolution, we apply the multipath technique of reducing the delay per stage of a ring oscillator [8] by connecting the inputs of each delay stage to a *combination* of previous delay stages. As shown in Fig. 5, application of this technique to the GRO entails the use of multiple devices for each delay element and connection of their gates to an appropriate combination of delay stages [3]. The relative weight of each delay stage input is controlled through appropriate sizing of its given device. In the 0.13-μm CMOS prototype presented in this paper, the multipath technique allows reduction of the delay per stage from 35 ps (i.e., one inverter delay) to 6 ps, hence yielding a factor of five improvement in TDC resolution.

B. All-Digital Quantization Noise Cancellation

The noise analysis shown in Fig. 3 ignored the fact that quantization noise is produced by dithering of the divide value in fractional-N synthesizers. As shown in Fig. 6, this quantization noise is highpass-shaped due to the action of the $\Delta\Sigma$ modulator, and much of it will be attenuated by the lowpass filtering action of the PLL dynamics. However, as indicated in the figure, the impact of seeking a higher PLL bandwidth will be to let more of the quantization noise through such that the high-frequency noise performance of the PLL is adversely impacted. Following the same example given in the previous subsection, a 500-kHz PLL bandwidth with a third-order $\Delta\Sigma$ modulator results in -138 dBc/Hz output phase noise at 20 MHz offset, which is 12 dB higher than the -150 dBc/Hz VCO phase noise at 20 MHz offset in the prototype.

Recent research has demonstrated that quantization noise in a $\Delta\Sigma$ fractional-N synthesizer can be significantly reduced through cancellation [9]–[12]. As shown in Fig. 7, cancellation is achieved in an analog fractional-N synthesizer by first computing the quantization error using a simple digital subtraction circuit between $\Delta\Sigma$ input and output, accumulating it (to convert from a frequency to phase signal), and then canceling it at the charge pump output through the use of a current DAC. Unfortunately, high levels of cancellation require the gain of the DAC to be precisely matched to the effective gain of the charge pump, so that complicated analog calibration circuits are required to achieve high performance [11], [12].

In contrast, a digital fractional-N synthesizer can deal with the quantization noise directly in the digital domain, and thereby avoid the need for extra analog circuits in performing cancellation. As such, we propose an all-digital cancellation loop which can be implemented with standard logic cells, as shown in Fig. 8. Similar to the analog approach, the quantization noise is fed into an accumulator (to convert from frequency to phase) and then subtracted from the TDC output after being properly scaled. Unlike the analog approach, the scale factor is easily computed by

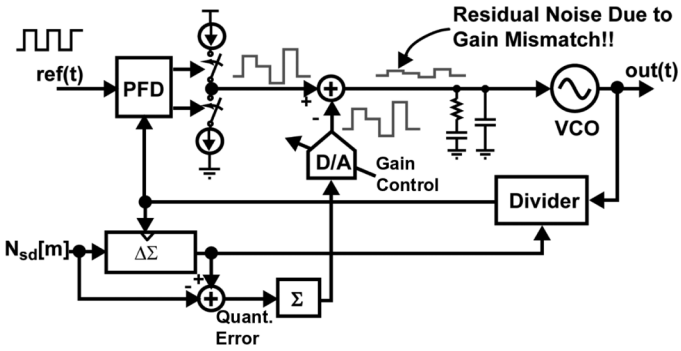

Fig. 7. Classical quantization noise cancellation technique in analog domain.

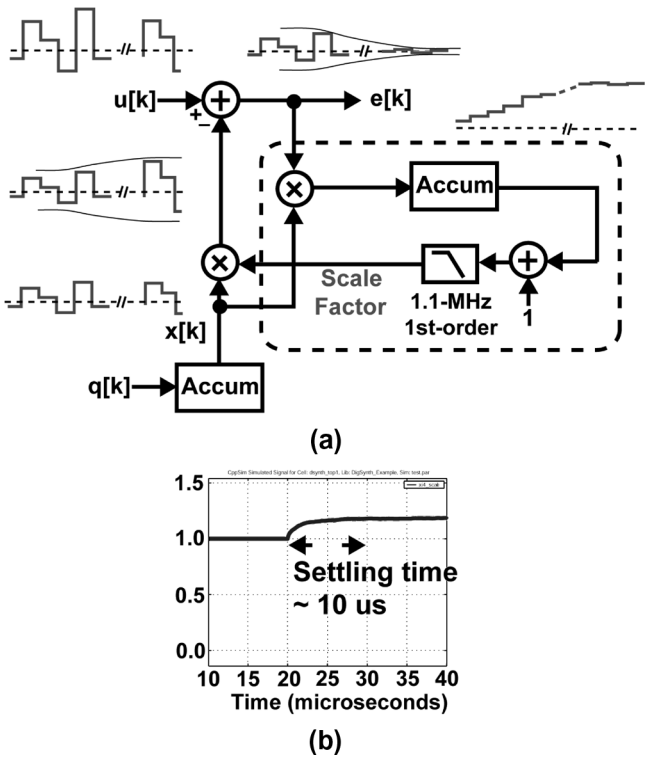

Fig. 8. All-digital quantization noise cancellation: (a) simplified view of the circuit and (b) settling behavior of the scale factor.

a simple digital correlator (i.e., a 16-bit digital multiplier) and accumulator circuit, as shown in the figure. In the case where the quantization noise is completely cancelled, the correlation will become zero and the accumulator will hold its value at the proper scale factor. An IIR lowpass filter with cutoff frequency of 1.1 MHz is used to further smooth the scale factor signal. Due to the high resolution of the TDC, the correlation feedback loop can be designed to have a reasonably fast settling time without introducing a significant amount of additional noise into the synthesizer. In the prototype system presented here, the loop is designed to settle in less than ten microseconds without adverse effects to the phase noise of the synthesizer.

One side benefit of the quantization noise cancellation circuit is that it can be used to precisely track the TDC gain. In the prototype, this information was not used since coarse open-loop gain calibration of the PLL, which was implemented by a 12-bit digital multiplier as shown in Fig. 2, was sufficient for the academic context of this work. However, future applications may benefit from this information in the case where TDC gain plays a critical role in the system performance.

III. Supporting Circuit Components

While the TDC and digital noise cancellation circuits play the key roles in achieving low noise with high bandwidth, the DCO and frequency divider circuits present their own challenges in striving for an elegant implementation of the overall digital synthesizer. As mentioned earlier, we consider the case of using a combination of a DAC and hybrid VCO to implement the DCO. While there is much literature on designing such VCOs [2], there has been very little research in determining appropriate DAC structures for this application space. As for the divider, current digital PLL structures commonly use a synchronous structure with the argument that it has excellent jitter characteristics. Unfortunately, such structures also have relatively high power consumption due to the fact that many elements must be clocked at the highest frequency in the system (i.e., the VCO frequency).

In this section, we propose a passive DAC implementation that requires minimal analog content, and a 3.6-GHz, low-jitter, asynchronous divider structure with 1.5-mW power consumption. We also say a few words about the hybrid VCO structure that is used.

A. Passive DAC

While the recent trend in digital phase-locked loops is to create a sophisticated DCO using a high-resolution switched capacitor network [1], it is worthwhile to note that the design effort required to achieve good performance from such an approach may be prohibitive in many PLL applications. Also, some applications that could benefit from the small loop filter size of a digital PLL may be constrained to using older technology which does not support the fine capacitor values required for a switched capacitor DCO. In such cases, it is worthwhile to consider the combination of a DAC and VCO for this function. Since VCO design is well understood from the available literature, we will focus on the issue of achieving a DAC implementation with adequate performance which avoids analog blocks such as opamps and transistor bias networks.

Fig. 9 displays a simplified circuit diagram of the proposed DAC structure, which provides 10-bit, 50-MHz operation with a full output range using a passive circuit structure. The key idea of the proposed DAC structure is to perform a two step conversion process using a 5-bit resistor ladder in combination with a 5-bit capacitor array. In step one, as illustrated in Fig. 9(a), the resistor ladder is used to form two voltages of value $V_L = M/32 \cdot V_{\rm DD}$ and $V_H = (M+1)/32 \cdot V_{\rm DD}$, where M ranges from 0 to 31, and $V_{\rm DD}$ corresponds to the 1.5-V supply voltage. Simultaneously, V_H is connected to N unit cell capacitors, and V_L to (32-N) unit cell capacitors, where N ranges from 0 to 31. In step two, as illustrated in Fig. 9(b), the capacitors are first disconnected from the resistor ladder, and then connected to a common capacitor $C_{\rm load}$. The combination of these steps at 50 MHz achieves 10-bit resolution as well as first-order filtering with cutoff frequency $f_o = 32 \cdot C_u/(2\pi \cdot C_{\rm load}) \cdot 50$ MHz.

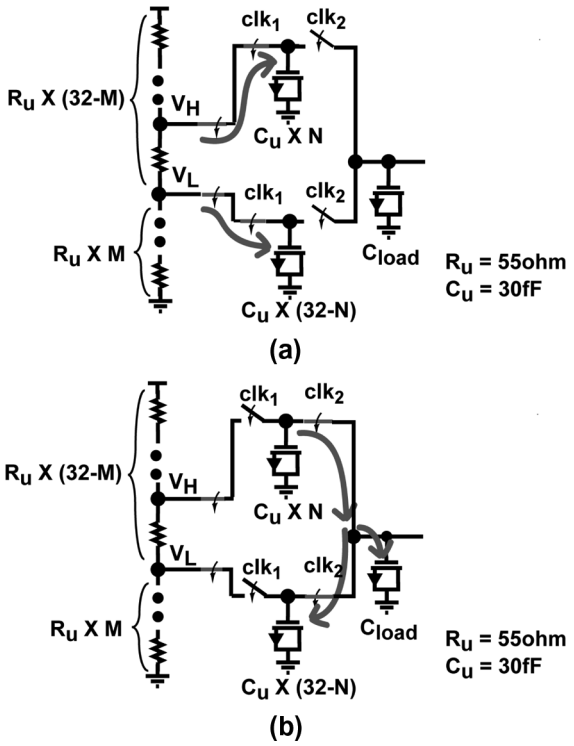

Fig. 9. DAC operation. (a) Step 1: unit capacitors charged. (b) Step 2: charge redistributed and filtered.

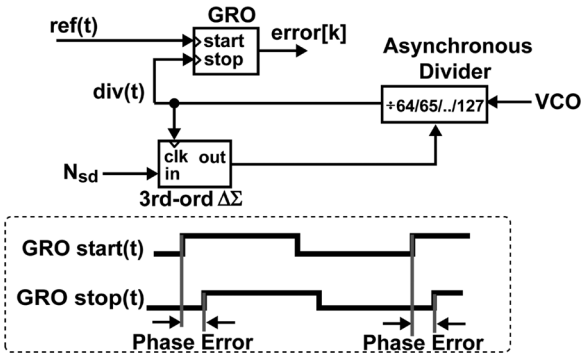

Fig. 10. Classical approach to using an asynchronous divider in a digital fractional-N PLL.

Therefore, the filtering bandwidth of each DAC can be adjusted by proper selection of the $C_{\rm load}$ capacitor value.

The unit resistance R_u and the on-resistance of the switches should be designed to be low enough in value such that the unit capacitors completely settle to V_H and V_L during step one. As such, low-V_T MOS devices are used to implement the switches in order to minimize their on-resistance. As for the capacitor array, the unit capacitor sizes must be chosen to be appropriately large to achieve acceptably low kT/C noise across the full range of the DAC. To achieve low area for these capacitors, zero-V_T nMOS capacitors are used for their implementation. Standard digital logic is used to performing the necessary decoding operations for control of the switch settings for a given input value to the DAC.

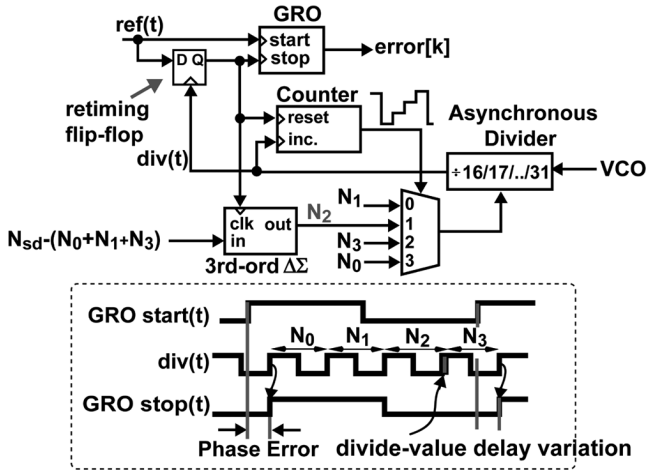

Fig. 11. Proposed asynchronous divider structure achieving low power and jitter.

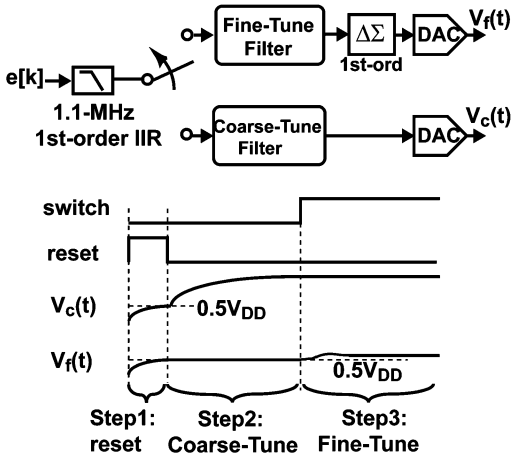

Fig. 12. Coarse/fine tuning of the PLL output frequency.

One crucial issue for the DAC is to appropriately clock it in a manner that does not introduce fractional spurs into the VCO. A standard clock generator is used to produce the non-overlapping clocks to drive the switches, but this generator must be driven by a clock which is synchronous to the VCO. For fractional-N synthesizers, this means that the divider output rather than reference input must be used as the master clock source.

If designed properly, the passive DAC structure supports monotonic operation without the need for any calibration. The key issues in design are to guarantee adequate settling of the resistor ladder to capacitor array voltage transfer, and to minimize charge injection effects through proper design of the switches. These issues are commonly understood from the literature.

Unfortunately, while monotonic operation is fairly easy to achieve without calibration, the mismatch between the unit resistors and capacitors will result in nonlinearity of the DAC transfer function. Since the DAC will be driven by a first-order $\Delta\Sigma$ modulator to improve its effective resolution, such nonlinearity will cause noise folding of the $\Delta\Sigma$ quantization noise. Fortunately, the 10-bit resolution offered by the passive DAC

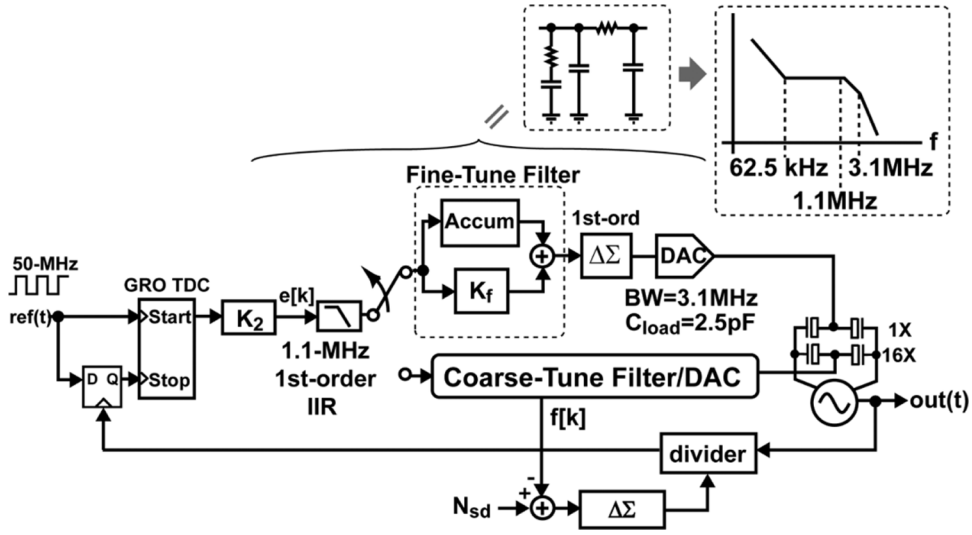

Fig. 13. Fine-tune digital loop filter.

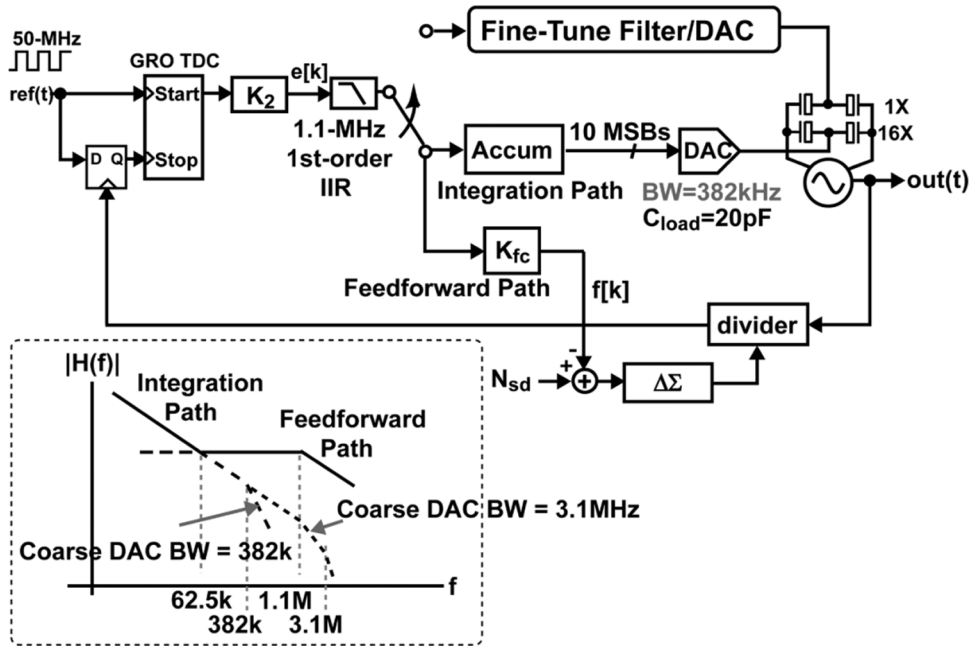

Fig. 14. Coarse-tune digital loop filter.

limits the magnitude of such noise folding, and detailed behavioral simulation shows that mismatch with a standard deviation of 5% does not have a significant effect on the overall noise performance of the synthesizer given the coarse/fine tuning method discussed later in this paper [13].

B. Asynchronous Divider

For classical analog fractional-N synthesizers, it is common to use an asynchronous divider structure [14] due to its low power and compact layout. As shown in Fig. 10, application of this structure to a digital fractional-N synthesizer is straightforward in principle. However, the key issue that arises is that the GRO TDC must support a very large time range during locking since the phase error can span the entire reference period. Since the nominal phase range required after the PLL is locked is much smaller than the reference period, this constraint can lead to wasted power and area in the GRO to support such a wide range since it is only briefly utilized during locking. Also, a subtle issue with the asynchronous divider structures is that the delay from input to output can shift slightly as a function of the divide value, which leads to additional jitter when dynamically varying the divide value according to a ΔΣ modulator [10], [15]. The common approach to dealing with such delay variation is to reclock the divider output with a register that is timed by the VCO output, but this approach is costly in power and also opens the door to metastability problems [10].

We propose a very simple divider modification that alleviates both of the issues described above. As shown in Fig. 11, the proposed structure reduces the divide value range of the core asynchronous structure such that the nominal frequency of the

core output $\mathrm{div}(t)$ becomes four times that of the reference frequency, $\mathrm{ref}(t)$. By using the core divider output to retime the reference (i.e., shown as the retiming flip-flop in the figure), the *effective* divider output impacting the GRO TDC has the same frequency as the reference. This retiming technique has similarities to a technique proposed in [1], but has the advantage of having fewer components operating at high frequencies. By multiplexing a series of four divide values into the divider each reference period, the effective divide value, N, becomes the sum of those values (i.e., $N = N_0 + N_1 + N_2 + N_3$). Note that only one of the divide values needs to be dithered by the $\Delta\Sigma$ modulator (i.e., N_2 in this example), whereas the rest can be kept at static values which are chosen according to the desired output frequency of the synthesizer.

To explain the advantage offered by the proposed divider structure with respect to TDC range, consider the fact that since the retiming flip-flop (shown in Fig. 11) is clocked at four times the reference frequency, the maximum time span seen by the TDC is 1/4 the reference period rather than the full reference period. In the case where the actual phase error exceeds the TDC range, it is a simple manner to keep track of the resulting cycle slips such that a net "unwrapped" phase is computed as indicated in Fig. 2. Once the PLL is locked, such cycle slipping will disappear and a TDC range of 1/4 the reference period will be more than adequate to track the PLL phase error. In the prototype presented here, the required TDC range becomes $1/(50\,\mathrm{MHz})/4 = 5$ ns, which leads to an 11-bit GRO implementation given that the raw resolution of the GRO is 6 ps.

As for the advantage offered with respect to divider delay variation, note that only one of the four edges of the core asynchronous divider output has an impact on the TDC each reference period. By choosing the divide value associated with that key TDC edge to be constant, the corresponding core divider delay from input to output will also be constant for that key edge (ignoring thermal noise effects). Therefore, if we simply choose the $\Delta\Sigma$ modulated divide value to control any of the *other* three core divider edges *not* corresponding to the key edge that impacts the TDC, we can avoid variation in the timing of that key edge due to the $\Delta\Sigma$ divide value variation [16]. As shown in the figure, we chose N_2 to be the divide value controlled by the $\Delta\Sigma$ modulator.

Implementation of the asynchronous divider was achieved with full swing TSPC logic [16], and the average current dissipation of the overall divider is 1 mA in 0.13-μm CMOS.

C. Hybrid VCO

The hybrid VCO used in the prototype is a well understood structure [2] that consists of a 4-bit switched capacitor network for coarse frequency tuning, and two varactors for continuous tuning at a coarse and fine level. A simplified view of the structure is shown in Fig. 2. The 4-bit switched capacitor network is implemented with MIM capacitors and is tuned by hand in the prototype through a serial interface on the chip to achieve an overall VCO range of 3.2 to 4.2 GHz. The coarse and fine tuning varactors correspond to accumulation-mode devices, with the coarse varactor sized to be 16 times larger than the fine tune varactor. Therefore, the K_v and tuning range of the coarse tune varactor is 16 times larger than the fine tune varactor. The consequence of this difference in K_v is discussed in the next section.

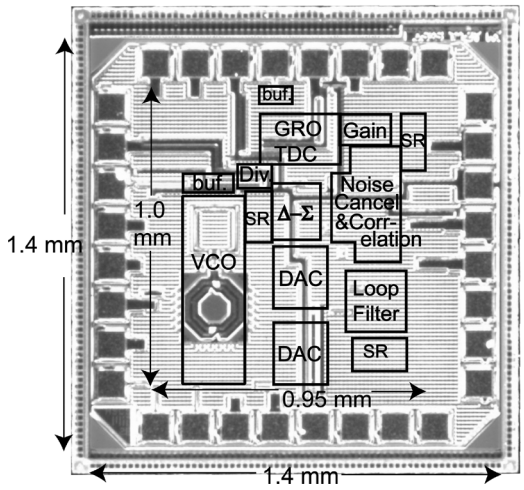

Fig. 15. Die photo of implemented 0.13-μm digital frequency synthesizer.

IV. PLL System Design

Fig. 12 provides a conceptual picture of the coarse/fine tuning method used to acquire phase-lock for the PLL, where we assume that the 4-bit control of the MIM capacitor array of the VCO has already been set to achieve the proper frequency band of operation. We see that the TDC output is first filtered by a 1.1-MHz IIR filter in order to reduce high frequency quantization noise of the TDC as well as any residual quantization noise produced by the dithered divide value that was not eliminated by the all-digital quantization noise cancellation circuit. During frequency acquisition, the filtered TDC output is first fed into a coarse-tune path while the fine-tune path is locked to its mid-range value. After the coarse-tune path is given a specified amount of time to settle, its value is locked in place and the filtered TDC output is then fed into the fine-tune path and the digital quantization noise cancellation is enabled. The state of the filters (i.e., reset, coarse-tune, and fine-tune) and the amount of time assigned to each state are controlled through a shift-register in the prototype. We discuss each of these tuning paths in more detail in this section.

We begin by providing further details of the simpler fine-tune path. As shown in Fig. 13, this path is designed to correspond to the analog lead-lag filter topology shown in the figure. A digital accumulator and feedforward gain of K_f realize a zero of 62.5 kHz, while the initial IIR filter and switched capacitor network of the fine-tune DAC realize poles of 1.1 and 3.1 MHz, respectively. Note that the DAC bandwidth is set according to its load capacitor, which has a value of 2.5 pF. Also, note that a first-order $\Delta\Sigma$ modulator is placed between the fine-tune loop filter and DAC in order to increase the effective resolution of the DAC.

The approximated s-domain open-loop transfer function of the PLL in steady state can be derived as [16]

$$A(s) = \frac{T}{T_{\mathrm{res}}} \cdot \frac{V}{2^B} \cdot \frac{K_v}{N_{\mathrm{nom}}} \cdot \frac{1}{s} \cdot H(z)|_{z=e^{sT}} \qquad (3)$$

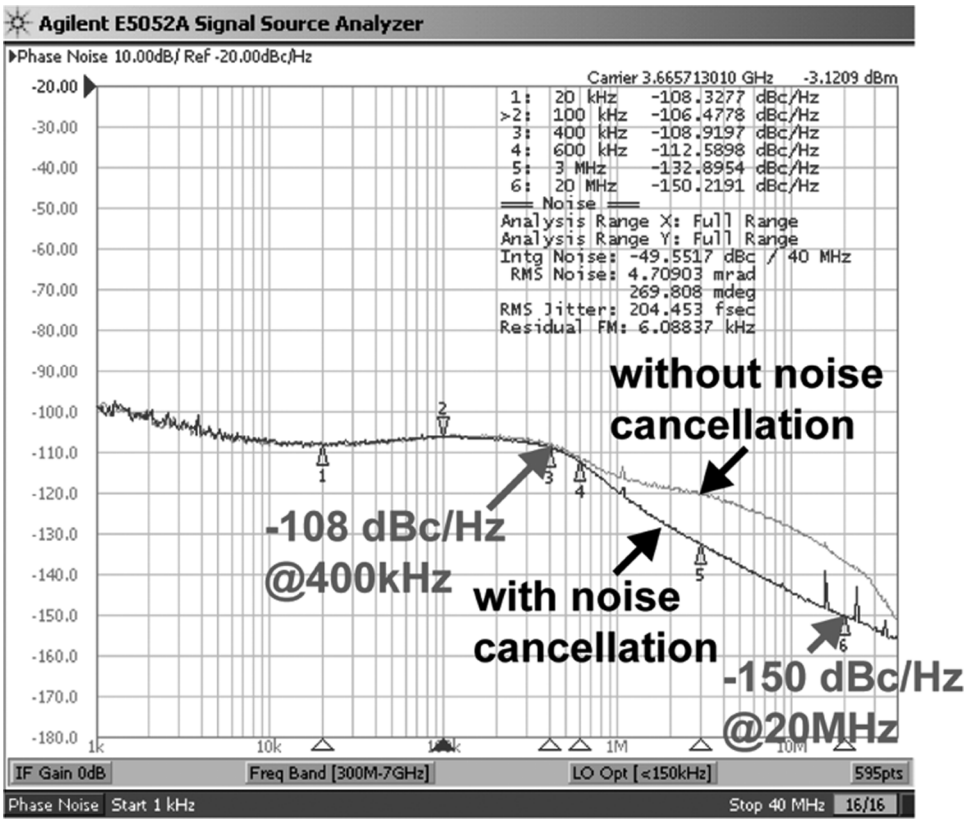

Fig. 16. Measured phase noise at 3.67 GHz with a 50-MHz reference clock.

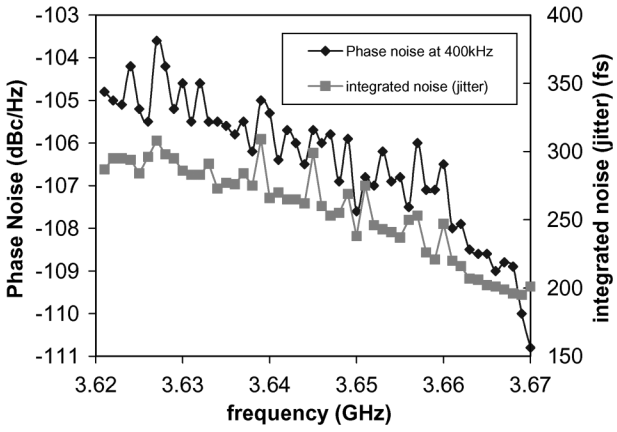

Fig. 17. Measured jitter and phase noise at 400-kHz offset over 50-MHz range with 1-MHz increments.

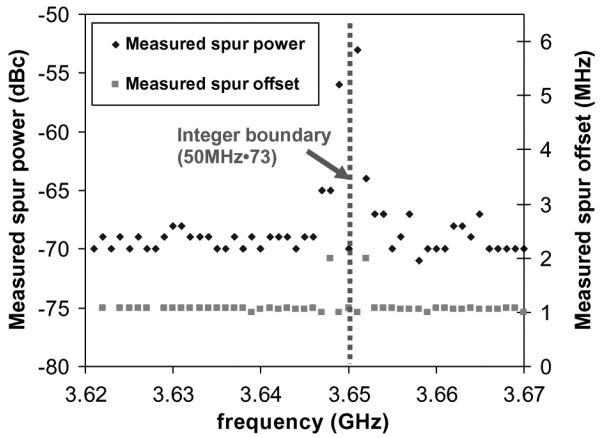

Fig. 18. Measured worst case fractional spurs over 50-MHz range with 1-MHz increments.

where $V/2^B$ is the gain of the DAC with V and B denoting the values of $V_{\rm DD}$ (1.5 V) and number of bits (10 bits), respectively. The VCO gain K_v is 5 MHz/V. In addition, $H(z)$ is the z-domain transfer function of the digital loop filter

$$H(z) = K_2 \cdot \frac{1-\alpha}{1-\alpha z^{-1}} \cdot \left(K_f + \frac{1}{1-z^{-1}} \right) \qquad (4)$$

where α sets the pole of the first-order IIR filter. The final s-domain open-loop transfer function can be obtained by plugging (4) into (3) and using the approximation of $z^{-1} = e^{-\rm sT} \sim 1 - {\rm sT}$. The parameters of the filter used in the prototype are $K_2 = 0.048$, $K_f = 128$, and $\alpha = 0.875$.

In contrast, the more complicated coarse-tune path is shown in Fig. 14. The key challenge in designing this path is to achieve fast settling despite the fact that the coarse-tune DAC bandwidth must be set to an $8\times$ lower value than the fine-tune DAC bandwidth. The decrease in bandwidth is achieved by increasing the load capacitor of the coarse-tune DAC to 20 pF (as compared to the 2.5 pF capacitance of the fine-tune DAC). The reason for the lower bandwidth is that the coarse-tune varactor K_v is $16\times$ higher than the fine-tune varactor (due to its $16\times$ larger tuning range), so that the KT/C and thermal noise of the coarse-tune DAC need to be more aggressively filtered to avoid degradation of the synthesizer noise performance.

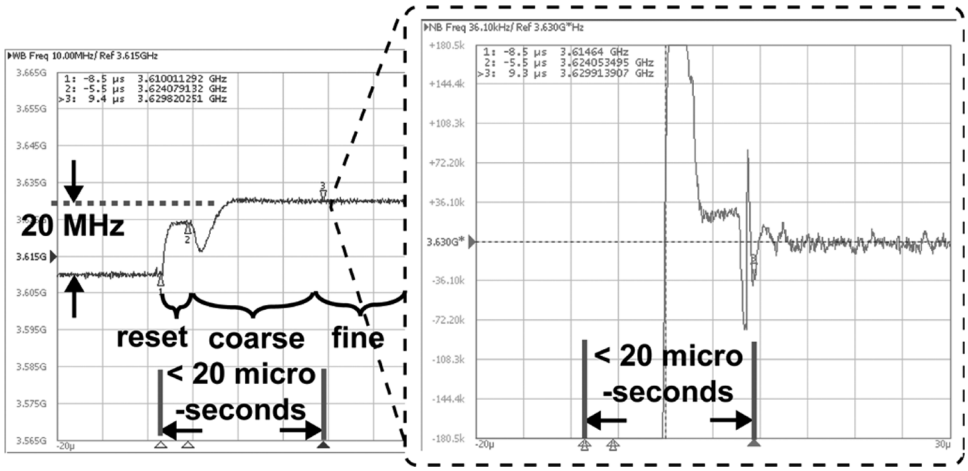

Fig. 19. Measured settling time achieves 10-ppm accuracy in less than 20 μs.

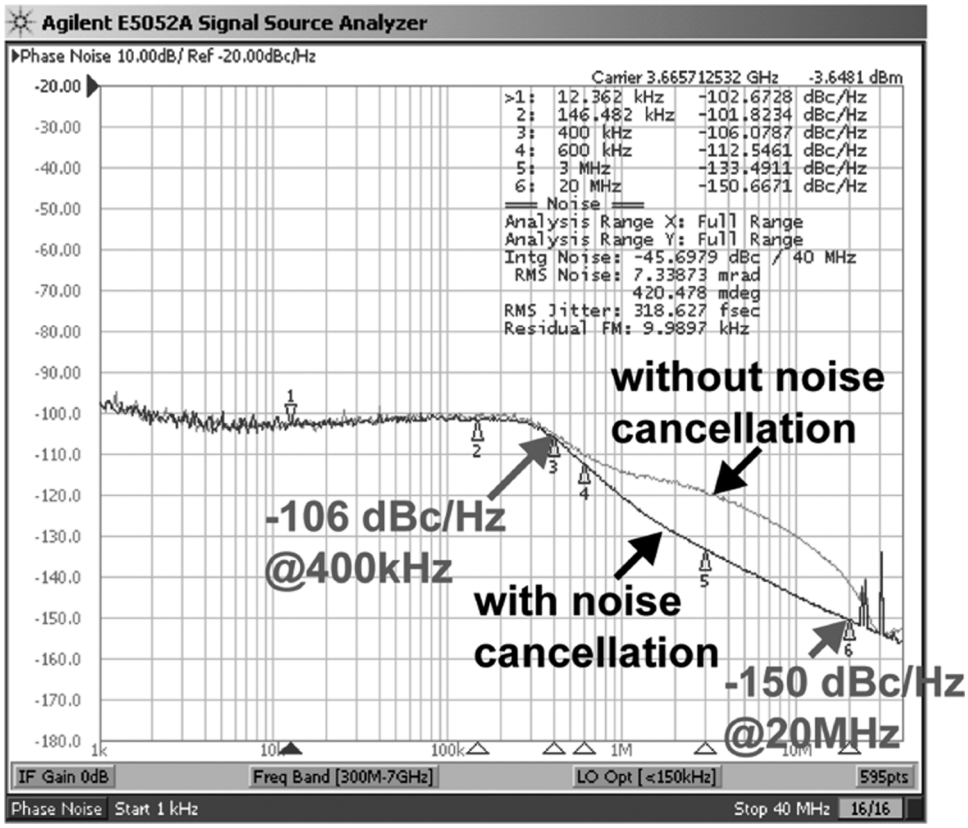

Fig. 20. Measured phase noise at 3.67 GHz with a 30.5-MHz reference clock.

To improve the coarse-tune settling time, we alter the loop filter topology of the fine-tune path such that only the accumulator path feeds into the coarse-tune DAC, as shown in Fig. 14. Since the accumulator path requires much less bandwidth to operate than the feedforward path, a much lower DAC bandwidth can be tolerated while still achieving reasonable settling times. Of course, the feedforward path is required to stabilize the PLL feedback loop, but this path can be implemented by bypassing the coarse-tune DAC and instead making use of the $\Delta\Sigma$ modulator and divider circuits as shown. This technique is similar to that proposed in [17], and has the interesting property of effectively turning the PLL feedback dynamics into a Type I system [16] despite the fact that two integrators are in the open loop system (i.e., the accumulator and VCO). A Type I system has the advantage of a faster settling time than its Type II counterpart, but has the disadvantage of providing less attenuation of VCO noise at low frequency offsets. However, since the coarse-tune path is used only during initial frequency acquisition, the reduced suppression of VCO noise is not of concern.

One additional benefit of reducing the coarse-tune DAC bandwidth is that it reduces the magnitude of the reference spur caused by clock feed-through within the DAC. While the fine-tune DAC also has such clock feed-through, its impact on the PLL output is 16 times lower due to the lower K_v of the fine-

TABLE I
COMPARISON BETWEEN PUBLISHED DIGITAL FREQUENCY SYNTHESIZERS

	[1]	[18]	[17]	[19]	[20]	**This Work**
Technology (um)	0.09	0.13	0.13	0.13	0.065	**0.13**
Reference Frequency (MHz)	26	40	185.5	26	25	**50**
Carrier (GHz)	0.9	2	2.2	3.6	3	**3.67**
Bandwidth (kHz)	40	3000	142	50	1200	**500**
Phase Noise (in-band)	-81 [1] (at 30kHz)	-96.9 [2] (at 400kHz)	-76 [3] (at 30kHz)	-78 (at 10kHz)	-100	**-108 (at 400kHz)**
Phase Noise at 400kHz	-110 [1]	-96.9 [2]	-92 [3]	-116	N/A	**-108**
Phase Noise at 20MHz	-153 [1]	-135 [2]	N/A	-152	N/A	**-150**
Jitter(ps)	N/A	N/A	N/A	N/A	N/A	**0.2**
Reference spur (dBc)	-92	N/A	N/A	-84	N/A	**-65**
Fractional spur (dBc)	N/A	-42	N/A	under phase noise level	-45	**-42**
Locking time (us)	10	N/A	N/A	N/A	N/A	**20**
Power	50.4mW [4]	25mW	14mW	40mA	9.5mW [4]	**46.7mW**
Active Area (mm^2)	1.5 [4]	0.8	0.7	0.86	0.4 [4]	**0.95**

1) Phase noise numbers are normalized to 3.6 GHz by adding 12 dB to the original reported numbers.
2) Phase noise numbers are normalized to 3.6 GHz by adding 5.1 dB to the original reported numbers.
3) Phase noise numbers are normalized to 3.6 GHz by adding 4.2 dB to the original reported numbers.
4) Include circuits to achieve frequency and/or amplitude modulation.

tune varactor. Also, note that a $\Delta\Sigma$ modulator is not required in the coarse-tune path since 10-bit resolution is more than adequate for achieving a small enough frequency error for the fine-tune path to stay within range [16].

V. MEASUREMENT

To verify the techniques presented in this paper, a prototype chip with die photo shown in Fig. 15 was implemented in a 0.13-μm CMOS process. The chip has an active area of 0.95 mm^2, of which the GRO TDC occupies 157×252 μm^2. The overall current consumption of the chip is 26 mA from a 1.5-V supply, excluding the VCO output buffer which consumes 7 mA from a 1.1-V supply. Assuming a steady-state time offset of about 1.2 ns (i.e., 4 to 5 VCO cycles), the GRO dissipates 2.3 mA. This offset value is programmable in the prototype, and is set to a small value to both lower the average GRO power dissipation and also lower its in-band noise.

The chip was first tested with a 50-MHz reference clock. Fig. 16 shows the best measured phase noise at 3.67 GHz from an Agilent Signal Source Analyzer E5052A, where the results are shown with and without cancellation of the quantization noise. As the figure reveals, greater than 15 dB noise cancellation is achieved such that out-of-band noise is dominated by the VCO. With noise cancellation enabled, the in-band noise is -108 dBc/Hz at 400 kHz offset, and out-of-band noise is -132 and -150 dBc/Hz at 3 and 20 MHz offsets, respectively. The integrated noise from 1 kHz to 40 MHz is 204 fs at this frequency. Phase noise was also tested from 3.620 to 3.670 GHz with intervals of 1 MHz. As illustrated in Fig. 17, the phase noise at 400 kHz offset as well as the integrated noise (i.e., jitter) degrades as the carrier frequency is lowered, but the overall jitter still remains less than 300 fs for most of that frequency range. In addition, measured worst case phase noise at 3 and 20 MHz offset are -131.5 and -148.5 dBc/Hz, respectively, in this frequency range.

The reference spur was measured with an Agilent Spectrum Analyzer 8595E to be -65 dBc at 3.67 GHz. Fractional spurs were also tested from 3.620 to 3.670 GHz with intervals of 1 MHz, as illustrated in Fig. 18. Worst case spurs occurred close to the integer boundary and were measured to be -53 dBc at carrier frequencies of 3.649 and 3.651 GHz, -64 dBc at carrier frequencies of 3.648 and 3.652 GHz, and were less than -65 dBc at all the other carrier frequencies. At frequency offsets less than 1 MHz away from the integer boundary, worst case fractional spurs were measured to be -42 dBc at a 400 kHz offset frequency.

A settling time of 20 μs for 10-ppm accuracy was measured when a frequency step of 20 MHz was applied to the synthesizer, as illustrated in Fig. 19.

The phase noise performance at 3.67 GHz with a lower reference clock was also measured, as illustrated in Fig. 20. The lowest reference frequency supported in the prototype is 30.5 MHz due to a limitation on the divider range. At this reference frequency, the PLL bandwidth scales to 300 kHz in proportional to the reference clock, and proper adjustment of the open-loop gain of the PLL is required to maintain stability. Although the in-band noise becomes higher, the phase noise at 400 kHz can still achieve -106 dBc/Hz.

Finally, Table I displays a comparison of the synthesizer to other recently published digital frequency synthesizers.

VI. CONCLUSION

This paper presented a 3.6-GHz, 500-kHz bandwidth digital $\Delta\Sigma$ frequency synthesizer architecture that leverages a recently published noise-shaping time-to-digital converter and an all-digital quantization noise cancellation technique to achieve excellent in-band and out-of-band phase noise, respectively. In addition, a passive DAC structure was proposed as an interface between the digital loop filter and a hybrid VCO to create a DCO, and an asynchronous divider structure was presented

which lowers the required TDC range and avoids divide-value dependent delay variation. The prototype was implemented in a 0.13-μm CMOS process and its active area occupies 0.95 mm^2. Operating under 1.5 V, the core parts excluding the VCO output buffer dissipate 26 mA. Measured phase noise at 3.67 GHz with a 50-MHz reference achieves -108 dBc/Hz and -150 dBc/Hz at 400 kHz and 20 MHz offsets, respectively. Integrated phase noise at this carrier frequency yields less than 300 fs of jitter (measured from 1 kHz to 40 MHz).

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