A Wide-Range, High-Resolution, Compact, CMOS Time to Digital Converter

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Abstract

This paper describes a wide range, area efficient, high resolution Time to Digital Converter (TDC), which has applications in digital frequency synthesizers used in wireless applications. The proposed architecture removes the need for long Vernier delay stages while measuring large phase differences using the Vernier delay line method. Resolution of a Vernier TDC is extremely susceptible to process, voltage and temperature (PVT) variations. The proposed compact implementation thereby minimizes the susceptibility of the TDC resolution to PVT variations. In the proposed method, time is digitized to the nearest multiple of a constant buffer delay and finer time digitization, less than one buffer delay is carried out using Vernier delay line. The TDC Circuit was designed and implemented in 0.18μm CMOS technology and achieves a resolution less than 10ps. The resolution variation in all the process corners was analyzed and the simulation results, layout implementation details and the linearity plots are presented.

Index Terms— TDC, Time to digital converters, phase detectors, Vernier delay line.

1. Introduction

In wireless communication transceivers, high performance frequency synthesizer is one of the key building blocks. To reduce cost and power consumption in the end mobile application, integration of RF circuitry in a conventional deep submicron CMOS process is desired. Recently, many all-digital implementations of RF frequency synthesizers have been reported [1] [2], which enable RF circuitry integration in a conventional CMOS process.

In a digital RF frequency synthesizer, phase frequency detection operation is carried out using a Time to Digital Converter (TDC) circuit, which converts very small intervals of time into its equivalent digital representation. The resolution offered by the TDC and its dynamic range of operation are few important factors that determine the operating parameters of the frequency synthesizer. Typically, TDC circuits digitize time by utilizing the propagation delay of delay cells, which can vary significantly due to process, voltage and temperature (PVT) variations. A wide range, high resolution TDC implementation spans a large area and hence the resolution of the TDC can be affected significantly due to PVT variations. Hence there is a need for area efficient implementations of wide range, high resolution TDCs and the proposed architecture successfully caters for this requirement. In addition to application in frequency synthesis, high resolution TDCs are extensively used in time of flight (TOF) applications in particle physics [3] as well.

The rest of this paper is organized as follows. Section 2 introduces the parameters of a TDC and explains the time digitization techniques currently used in digital frequency synthesizers. Section 3 explains the operation of two variants of the proposed TDC architecture. Section 4 elaborates the circuit and layout design issues for the proposed TDC architecture. Section 5 and 6 summarize the simulation results and the layout implementation details and illustrates the area reduction achieved without any compromise on resolution, using the proposed TDC architectures. We will conclude the paper in Section 7.

2. Background

2.1. Definitions and TDC Parameters

Digital frequency synthesizers have a digitally controlled oscillator (DCO), which generates a high frequency clock based on a digital input control word. The phase error between the DCO clock (CLKA) and a reference clock (CLKB) is calculated in the feedback loop of the frequency synthesizer and is used to control the DCO. The phase error is determined by the Time to Digital converter, which functions as phase frequency detector in the digital frequency synthesizer system. A new paradigm in RF circuit design as defined in [1] is, "*In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals*". Since resolution of the TDC directly dictates the time domain resolution in RF circuits, it is an important circuit under this paradigm.

In RF frequency synthesizers, since small intervals of time, typically in the order of picoseconds are to be measured, design approach for a TDC is significantly different from conventional logic circuits. The smallest time interval that can be digitized in a TDC is the resolution of the TDC. The maximum phase error that can be detected using the TDC circuit is the dynamic range of phase detection (T_p) of the TDC. Between successive time digitization operations, if a

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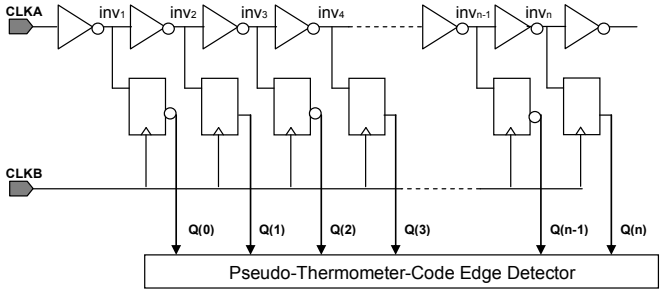

Figure.1 TDC built with chain of inverters

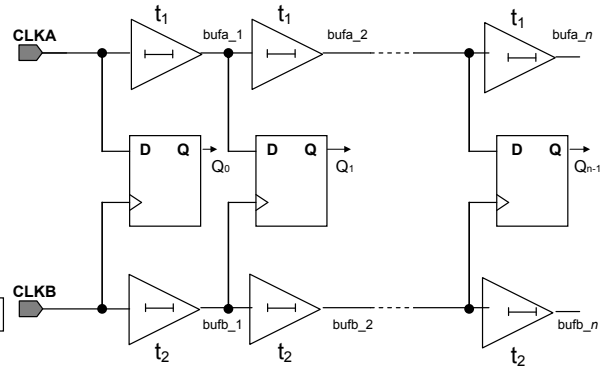

Figure.2 TDC built with Vernier Delay Line

delay is incurred, it is referred to as dead-time in the TDC. In RF frequency synthesizers, a high resolution, wide range TDC with zero dead-time is desired. Further, the process of time digitization should be linear across the dynamic range of the operation of the end application.

2.2. Prior Art

TDCs have been implemented digitally using either the inverter chain method or Vernier delay line method.

2.2.1 Inverter chain method. If the end application does not require a very high resolution, time digitization can be carried out using a chain of inverters [4]. The implementation is shown in Figure.1. The resolution achieved using such an implementation is one inverter delay (t_{inv}) and is about 40ps in deep-submicron CMOS process. This resolution can be further improved by time-averaging [4]. This implementation is very compact but the resolution achievable is limited to one inverter delay. Even though t_{inv} is decreasing with scaling of technology, any finer time digitization is impossible. The number of inverters required in the inverter chain to cover a dynamic range of T_p is $\{T_p / t_{inv}\}$

The TDC output is typically a *thermometer* or *pseudo-thermometer code* that provides a digital representation of the phase difference between CLKA and CLKB.

2.2.2 Vernier Delay Chain method. Vernier delay lines can be used to achieve time digitization with a very high resolution [5]. In the Vernier delay line method illustrated in Figure.2, two buffer lines with delays of t_1 and t_2 are used in each stage. The resolution achieved is of the order of (t_1-t_2). Since resolution is determined by the differential delay, this method enables us to digitize time with a very high resolution [3][5]. Time resolutions of the order of 30ps in 0.7µm CMOS technology have been reported using this method [3].

The number of Vernier stages required to cover a dynamic range of T_p is $\left\{\frac{T_p}{(t_1 - t_2)}\right\}$.

However, if the dynamic range (T_p) is large, the area of the phase detection circuitry grows linearly requiring long chains of delay elements. Since layout of such an implementation can span a large area, process variations introduced may nullify the resolution gain achieved using the Vernier line method.

3. Proposed Architecture

We propose a new wide range, high resolution, compact TDC architecture that exploits the advantages offered by both the inverter chain method and the Vernier delay method. Instead of a chain of inverters, a buffer (non-inverting) chain is used. The time digitization operation is done in two phases: A coarse time delay calculation to the nearest multiple of buffer delay (t_{buf}) is carried out using the buffer chain and a finer delay t_d (always less than t_{buf}) is calculated using the Vernier delay line.

Thus the maximum phase difference to be calculated (T_p), is determined in this architecture as follows:

$$T_p = n \times t_{buf} + t_d \quad \textbf{(1)}$$

where n is an integer value determined using the buffer chain and t_d is determined using the Vernier delay line.

A representative diagram of the proposed architecture is illustrated in Figure.3.

We eliminate the need for lengthy Vernier delay chains without compromising the time resolution of the TDC. Since the circuit implementation spans a smaller area, as illustrated in the simulation results in Table 1, PVT variations in delay cells in the TDC are minimized. Further, in the proposed architecture, the phase difference between the input clocks is calculated without any dead time.

Two variants of the proposed TDC architecture are presented in this paper: Linear implementation of the Vernier delay line and a Folded implementation of the Vernier delay line.

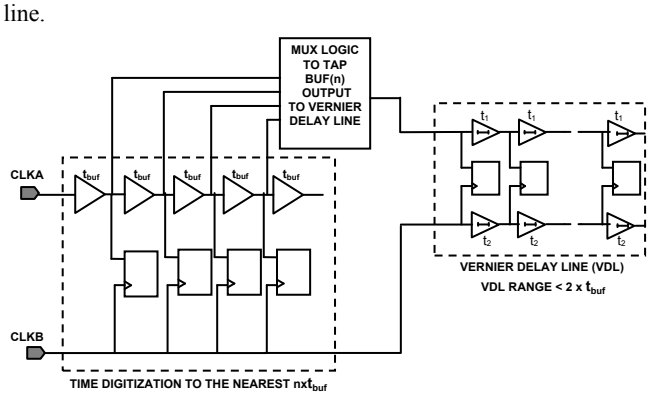

Figure.3 Proposed TDC Architecture

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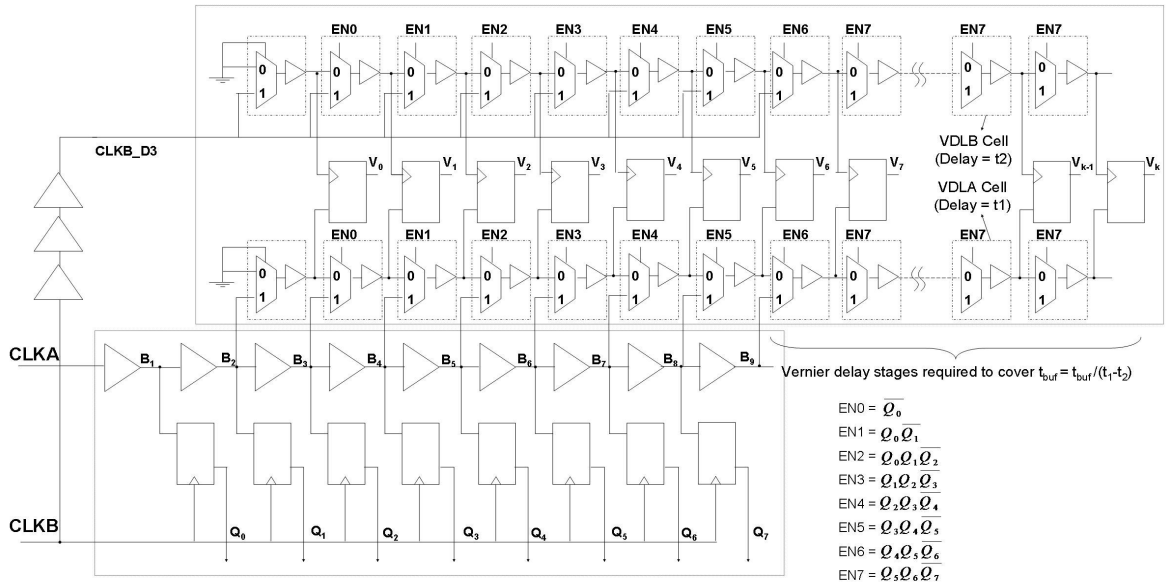

Figure.4. Linear Implementation of TDC

3.1. Linear Implementation of Vernier delay line

The TDC architecture shown in Figure.4 is the linear implementation of Vernier delay line.

A series of distributed multiplexers, which are actually part of the Vernier delay line, are used to tap the buffer outputs from the buffer chain into the Vernier delay chain. The output of any buffer in the buffer chain can be tapped into the Vernier delay line by enabling the respective multiplexer and the phase difference between that particular buffer output and CLKB is calculated in the Vernier delay line.

Each delay cell in the Vernier stage is substituted by a combination of a multiplexer and a delay cell, as illustrated in Figure.5. The multiplexers are used to either tap the buffer outputs or pass the signal from the previous Vernier stage. The Vernier delay line has delay cells VDLA cell and VDLB cell in the upper and lower chain with delays d_1 and d_2 respectively. Since the multiplexer is part of the Vernier delay line, its delay T_{mux} gets added to each of the delay chains. But since the resolution of the Vernier delay line is determined by the differential delay, the multiplexer delay gets cancelled out.

Hence the time resolution of the TDC is:

$$(t_1-t_2) = (T_{mux}+d_1) - (T_{mux}+d_2) = (d_1-d_2) \qquad \textbf{(2)}$$

which is the differential delay between the delay cells used in the chain.

The architecture limits the maximum range of the Vernier delay line to only one buffer delay. Hence the length of the Vernier chain is very short compared to 'Vernier only' delay lines. The operation of the TDC is explained using the Timing diagram shown in Figure.6.

The phase difference T_p is calculated according to the equation $T_p = n \times t_{buf} + t_d$. The thermometer code output of the buffer chain (Q_0, Q_1, Q_2 etc in Figure.4) determines n. The Vernier delay chain is used to calculate the residual time difference t_d. Since t_{buf} is known a-priori, instead of measuring t_d directly, time difference (t_{buf} -t_d) (denoted by * in Figure.6) is calculated using Vernier delay line. This is accomplished by passing a tapped output from buffer chain and a delayed replica of CLKB through the Vernier delay line.

The key challenge in the architecture is to enable the corresponding multiplexer to tap a desired buffer output into the Vernier chain. A thermometer code edge detection circuit implemented using the logic gate $z = ab\overline{c}$, is used to enable the respective multiplexer. This logic gate, along with the clock-to-Q delay of the flip-flop incurs a delay (equivalent to two buffer delays in 0.18μm CMOS technology). Due to this delay incurred by the multiplexer enable logic, the first multiplexer immediately after thermometer code edge cannot be enabled. Only subsequent buffer outputs can be tapped into the Vernier delay line. In the illustration shown in Figure.4, the third multiplexer after the thermometer code edge is enabled and the third buffer output from the thermometer code edge is tapped into the Vernier delay line. Hence CLKB is also delayed by a similar buffer delay, resulting in signal CLKB_D3 which is used in the Vernier delay line.

In the waveform example illustrated in Figure.6, the Vernier delay line is expected to measure the time duration (t_{buf} -t_d). The thermometer edge detection logic enables signal EN1, which in turn enables the third multiplexer from the thermometer edge and taps signal B_4 into the Vernier delay line. It can be observed that signals B_4 and CLKB_D3 maintain the same time difference (t_{buf} -t_d), which is the desired time duration expected to be measured by the Vernier delay line.

If the last buffer output in the buffer chain is tapped, the Vernier delay line should be able to calculate the residual time t_d after that. This decides the number of delay stages required in the Vernier delay line in this linear implementation. The number of Vernier stages required = number of buffers in

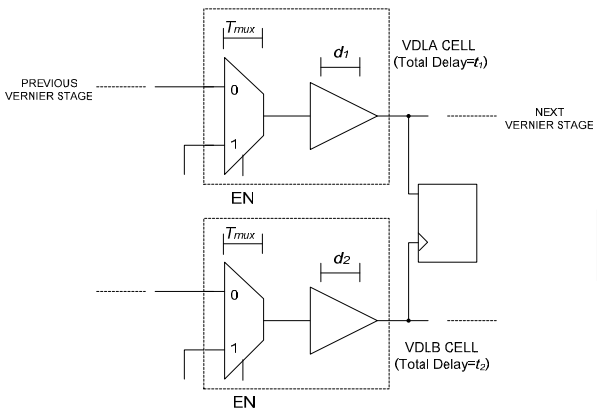

Figure.5.A single Vernier stage in the Vernier delay line

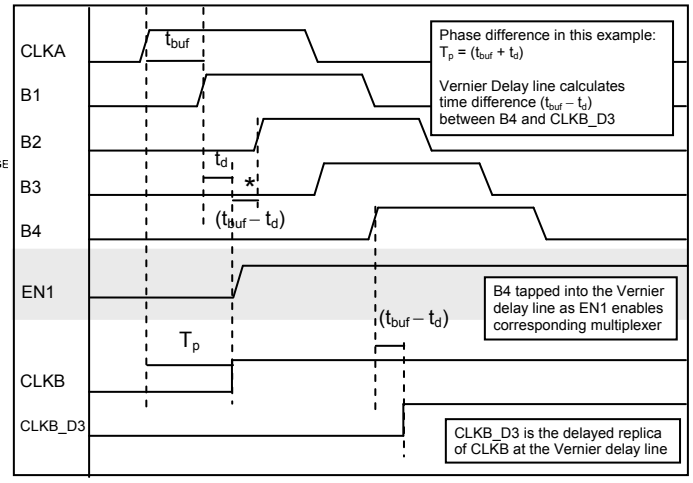

Figure.6 Operation of proposed TDC

buffer chain $+\left\{\frac{t_{buf}}{(t_1 - t_2)}\right\}$ + extra stages to cover corner cases due to PVT variations.

3.2. Folded Implementation of Vernier delay line

Number of Vernier stages in the linear implementation can be reduced by reusing cells, thereby resulting in a folded Vernier delay line. The proposed folded implementation is shown in Figure.7. In this architecture, the output of the last stage of the Vernier delay line is looped back to the first stage. Hence, the number of delay stages required in the Vernier delay line = *max{number of buffers in buffer chain*, $\left\{\frac{t_{buf}}{(t_1 - t_2)}\right\}$}+ extra cells to cover corner cases due to PVT variations. If the number of buffers in the buffer chain is large, this method will provide considerable reduction in area, as compared to the linear implementation.

In this architecture, only one tap from the buffer chain has to be active at all times. Two or more active taps will lead to corruption of delay calculation in the Vernier delay line. Hence the multiplexer select logic for each multiplexer is dependent on a circular shift of the pseudo-thermometer code from the buffer chain. The circular nature of the signal connections in such an implementation mandates a very careful layout and necessitates extensive circuit simulations to ensure proper operations under all PVT variations.

4. Design Issues

The Vernier line thermometer code calculation is extremely susceptible to metastability. The flip-flops tied to the chain try to measure very small units of time and even few picoseconds delay addition due to process variations or jitter can result in a metastable output from the chain. To ensure proper measurement along the Vernier delay line, two precautions are taken:

1. Improved sense amplifier type flip-flop [6] is used to latch the data in the Vernier delay line. This flip-flop has negative setup time and narrow metastability window. This flip-flop is chosen despite its large area overhead.
2. The output of the buffer chain (V_0, V_1, V_2 etc in Figure.4 and Figure.7), is a pseudo-thermometer code. Edge detection is carried out in this thermometer code in order to enable the respective multiplexer in the Vernier delay line. A bubble introduced in the pseudo-thermometer code due to metastability can enable an incorrect multiplexer and hence can corrupt the delay calculation. Therefore the decoding logic assumes that a bubble is always present in the thermometer code. The edge detection circuit is implemented using a $z = ab\bar{c}$ logic gate. Better bubble detection and elimination algorithms [7] can be implemented if the decoding logic can be designed with no dead time in the TDC.

If CLKA time period is less than the total delay in the buffer chain, two or more valid edges may be detected in the pseudo-thermometer code. This could lead to non-linear characteristics in the TDC operation. Hence the count of buffers required in the buffer chain is determined by the number of buffers needed to cover the full CLKA time period under strong process corner and some design margin.

The TDC implementations shown in Figure.4 and Figure.7 have two delay cells: A VDLA cell which is part of the upper chain of the Vernier delay line and VDLB cell which forms part of the lower chain. The delay cells are implemented digitally as a current starved delay cell with digital control, as shown in Figure.8. The circuit implementation of both the delay cells is basically the same and it functions as either of them depending on the digital inputs C_1 and C_2. The delay cells are sized such that both the rise and fall time of the cells differ by the resolution required in the Vernier delay line. In 0.18μm CMOS technology, a time difference of 10ps was maintained between the delay cells. The fan-outs of the individual delay cells vary, as one of them is supplied as data to the flip-flop and the other as clock to the flip-flop. Since inside the flip-flop, data and clock signals have non-uniform fanout, we have characterized the delays

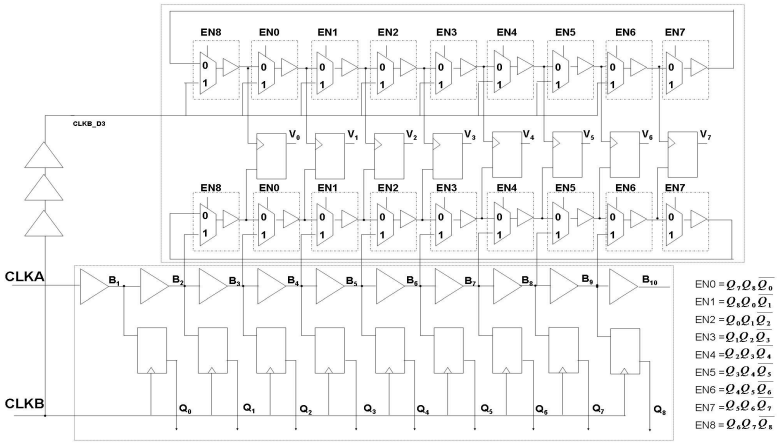

Figure.7 Folded Implementation of TDC

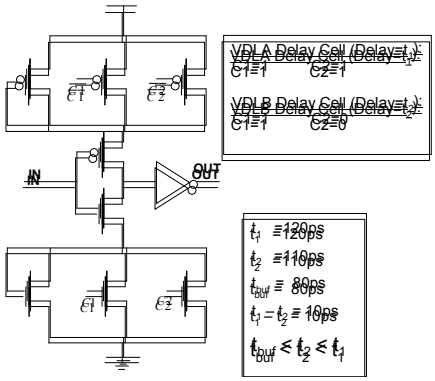

Figure.8 Current starving Delay Cell with digital control

carefully to maintain the delay difference despite the fanout variation.

Time resolution of the TDC can be further improved by tracking the time difference from both positive edge and negative edge of the DCO clock (CLKA) and normalizing the time differences. This normalizing technique has been used in other TDC implementations [4]. Normalizing can also remove the metastability errors introduced in the decoding of the thermometer code. But if an inverter chain is to be used instead of the buffer chain, the area of final implementation might increase in order to maintain the same dynamic range (T_p) and resolution and sizing of the transistors has to be done extremely carefully to match both rise and fall times of the signals in the circuit.

5. Simulation Results

The TDC circuits were simulated using SPICE in 0.18µm CMOS technology for all PVT corners. Using SPICE simulations, the worst case delay numbers for each cell was calculated. Based on the propagation delay values obtained from SPICE, Verilog Behavioral simulation was used to validate the operation of the TDC for an exhaustive set of phase difference inputs and for all PVT variations.

The actual phase difference versus calculated phase difference plots are presented in Figure.9 and Figure.10, which illustrate the linearity of operation for both linear and folded TDC implementations.

It can be observed that the operation of both the architectures is linear for all the process corners. The calculated output of the TDC saturates when its range is exceeded. Since range of the TDC is slightly different for each process corner, the saturating threshold is also different for each process corner. The encircled area in each of the plots denotes the region where the TDC range is exceeded.

We summarize the area requirements of both implementations in Table 1. The minimum time resolution for all the methods was kept at 10ps. The table shows that a significant reduction in area is achieved without any compromise in resolution. This area reduction also reduces the effects due to PVT variations across the layout of the TDC circuit in the chip. Further, the area reduction also will result in reduced power consumption in the TDC circuit, which is very important for mobile applications.

6. Layout Implementation

Layout of the Linear TDC Implementation was drawn in CMOS 0.5µm technology and is shown in Figure.11. The design occupied an area of 850µm x 620µm. The final layout along with TDC test logic is shown in Figure.12. The resolution of the Linear TDC is 30ps in this CMOS 0.5µm technology layout implementation. The buffer delay t_{buf} in this implementation is 110ps and the dynamic range of the TDC layout is 1200ps.

Extreme care was taken during the layout implementation of the TDC to maintain the differential delay of 30ps across all the Vernier delay stages despite the unequal fan-outs and parasitic effects of interconnects.

Table.1 Area requirements of the TDC implementations in CMOS 0.18µm technology

Case 1: T_p = 600ps, (t_1-t_2) = 10ps and t_{buf} = 80ps.		
Method	Estimated Area in CMOS 0.18µm Technology (µm^2)	% Reduction in Area with respect to Vernier delay line only method
Vernier delay line only	75840	--
Proposed architecture (linear)	11200	85.2%
Proposed architecture (folded)	5960	92.1%

Case 2: T_p = 1200ps, (t_1-t_2) = 10ps and t_{buf} = 80ps.		
Method	Estimated Area in CMOS 0.18µm Technology (µm^2)	% Reduction in Area with respect to Vernier delay line only method
Vernier delay line only	151680	--
Proposed architecture (linear)	16500	89.1%
Proposed architecture (folded)	8600	94.3%

7. Conclusion

A wide range, area efficient, time digitization circuit has been implemented with the proposed TDC architecture while maintaining a very high resolution of less than 10ps in 0.18µm CMOS technology. With technology scaling, better Vernier

delay lines with less than 5ps accuracy can be built and used in the TDC architecture. Further, the current CMOS technology allows us to build precise digital delay locked loops, which can also be used to stabilize the delays of the delay chains in the architecture. Due to its wide range of operation, area efficiency, reduced power consumption and very high resolution, the proposed TDC architecture has potential applications in digital RF frequency synthesizers and TOF applications in particle physics.

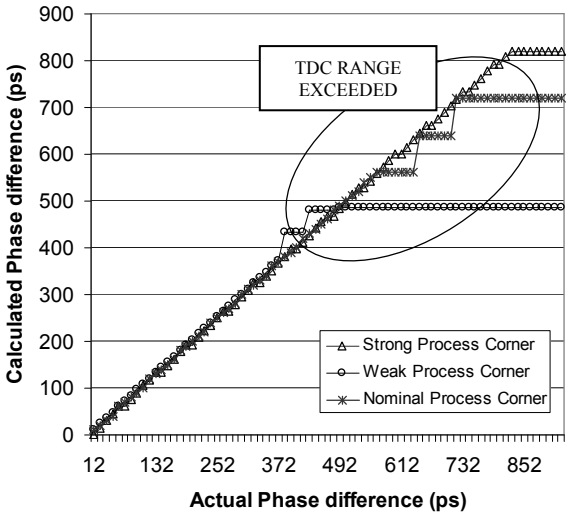

Figure.9 Linearity plot of Linear TDC implementation

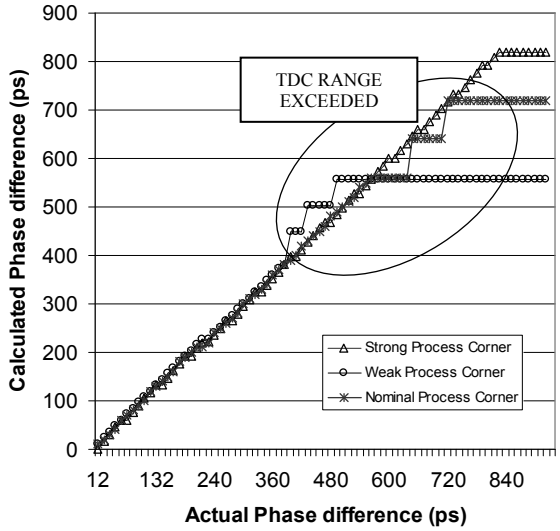

Figure.10 Linearity plot of Folded TDC implementation

8. Acknowledgment

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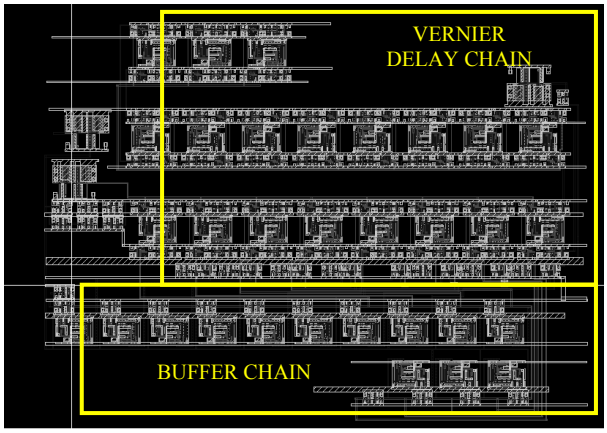

Figure.11 Layout of Linear TDC in CMOS 0.5µm technology

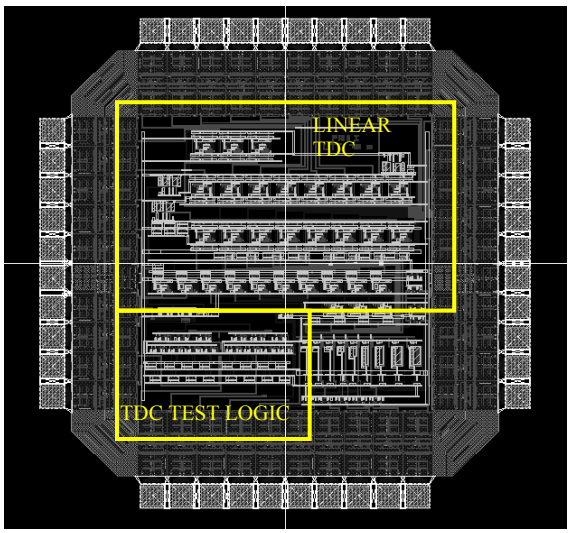

Figure.12 Layout of Linear TDC and TDC test logic in CMOS 0.5µm technology