# A $1.75-\mathrm{GHz} / 3-\mathrm{V}$ Dual-Modulus Divide-by-128/129 Prescaler in $0.7-\mu \mathrm{m}$ CMOS 

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#### Abstract

A dual-modulus divide-by-128/129 prescaler has been developed in a $0.7-\mu \mathrm{m}$ CMOS technology. A new circuit technique enables the limitation of the high-speed section of the prescaler to only one divide-by-two flipflop. In that way, a dual-modulus prescaler with the same speed as an asynchronous divider can be obtained. The measured maximum input frequency of the prescaler is up to 2.65 GHz at 5 V power supply voltage. Running at a power supply of 3 V , the circuit consumes 8 mA at a maximum input frequency of 1.75 GHz .


## I. Introduction

RECENT publications have demonstrated the everincreasing importance of CMOS RF circuits [1]-[3]. CMOS offers the big advantage of cheap processing and single-chip integration with digital building blocks. But to obtain the high frequencies required in modern telecommunication systems, at a reasonable power consumption, new circuit techniques must be developed.

The frequency synthesizer is one of the major building blocks for integrated transceivers. It requires a lot of effort to achieve the required specs in a standard CMOS process without any external components. Most frequency synthesizers are of the phase-locked loop (PLL) type, as shown in Fig. 1. The only two blocks operating at the full frequency are the voltage-controlled oscillator (VCO) and the prescaler. For reasons of low noise and low power, the VCO must be an oscillator based on the resonance frequency of an LC-tank with passive on-chip inductors [4], [3].

The prescaler must also operate at the full frequency. It divides the VCO output frequency ( $F_{\text {out }}$ ) by a certain ratio to a low-frequency signal ( $F_{\text {div }}$ ). This signal is locked by the PLL onto a very stable reference frequency ( $F_{\text {ref }}$ ). The division ratio must be variable to allow a fast changing of the synthesized frequency. In the configuration of Fig. 1, the modulus is controlled by the overflow bit of of the accumulator. The synthesized frequency is then equal to

$$
\begin{equation*}
F_{\text {out }}=(N+n) \times F_{\text {ref }} \tag{1}
\end{equation*}
$$

So frequencies equal to a fractional multiple of the reference frequency can be synthesized, which explains the term fractional- $N$ frequency synthesizer. High-speed dual-modulus prescalers are more difficult to construct than frequency dividers with a fixed division ratio, because the extra dualmodulus logic slows down the system [5].

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Fig. 1. PLL fractional- $N$ frequency synthesizer.

In this paper, a high-speed CMOS dual-modulus prescaler is presented that does not suffer from this speed degradation. The topology used to obtain this result is explained in the next section. It is based on the $90^{\circ}$ phase relationship between the master and the slave section of a Master/Slave (M/S) toggle flipflop. Section III shows the several high-speed building blocks that were designed to obtain a $1.75-\mathrm{GHz}$ input frequency at a supply voltage of only 3 V . Section IV reports the measured performance of the circuit. The last section draws some conclusions.

## II. Prescaler Topology

A conventional high-speed dual-modulus prescaler generally consists of a synchronous divide-by- $4 / 5$ part and an asynchronous divide-by-32 part as shown in Fig. 2 [5]. The synchronous divider is the only part of the circuit operating at the maximum input frequency. Most of the time, its control signal Ctrl is low, so the output frequency $F 4$ is determined by the loop over the first two $D$-flipflops and equals one-fourth of the input frequency. This frequency is divided by 32 in the asynchronous divider to obtain an output frequency $F_{\text {out }}$ equal to $F_{\text {in }} / 128$. The divide-by- 129 operation is enabled by setting the Mode-input high. When the outputs of all flipflops of the asynchronous divider are high, i.e., once every period of the output signal $F_{\text {out }}$, the Ctrl -signal becomes high. This causes the loop in the synchronous divider to be closed over three flipflops instead of two. This extra delay is equivalent to a divide-by-five operation. So the prescaler divides once by five and 31 times by four, which results in a division by 129.


Fig. 2. Conventional dual-modulus prescaler architecture.

The problems with this prescaler topology are, of course, situated in the synchronous divider. It is the only part of the circuit operating at the maximum frequency, the rest of the circuit runs at maximum one-fourth of the input frequency. The synchronous divider contains three high-frequency fully functional $D$-flipflops. These flipflops are the reason for a lot of power consumption and clock load. Moreover, the NANDgates in the critical path of the synchronous divider loop will cause a decrease in the maximum input frequency. Clever design can reduce this effect by embedding the NAND-gate into the first stage of the flipflop, but can never eliminate it completely. Therefore, a dual-modulus prescaler will always have a smaller operating speed than an asynchronous frequency divider [5].

The new dual-modulus prescaler topology proposed here solves all these problems. The block diagram is shown in Fig. 3. It consists of a chain of seven pure divide-by-two circuits interrupted by a phase-select block. Since the frequencylimiting first stage is only one toggle-flipflop, input frequencies as high as asynchronous dividers can be obtained. The dualmodulus operation is based on the 90 -degrees phase relationship between the outputs of the master and the slave of a Master/Slave (M/S) $D$-flipflop.

The new prescaler operates as follows. The differential input signal $F_{\text {in }}$ is fed to a first high-speed divide-by-two flipflop. This flipflop is the only one operating at the full input frequency. It must not be a fully functional flipflop, but can be optimized for divide-by-two operation. The resulting signal $F 2$ is once again divided by a second high-speed divide-by-two flipflop. For the dual-modulus operation, this flipflop must be of the master/slave kind as shown in Fig. 4(a). Four output signals result: the differential output of the master (F4.I and $\overline{F 4 . I}$ ) and the differential output of the slave ( $F 4 . Q$ and $\overline{F 4 . Q}$ ). When the Mode-input is low, the frequencycontrol block is disabled and its output signal Ctrl will be constant. Therefore, the phase-select circuitry simply picks one of its four input signals and connects it to the input of the asynchronous divide-by- 32 block. This block is a chain of five divide-by-two flipflops operating at a relatively low speed (maximum one-fourth of the input frequency). The resulting


Fig. 3. New dual-modulus prescaler architecture.
output frequency is thus a factor of $2 \times 2 \times 32=128$ smaller than the input frequency.

The divide-by-129 operation is enabled by setting the Modeinput high. The frequency-control block is now working. On every positive edge of the output signal $F_{\text {out }}$, the control signal Ctrl will be changed in such a way that the phase-select block will connect $F 4$ to the signal that is $90^{\circ}$ delayed with respect to the present signal. So when $F 4$ is initially connected to F4.I, after the rising edge of $F_{\text {out }}$, a connection will be made to $F 4 . Q$. This is shown in Fig. 4(b). Since the signal F4.Q lags the signal $F 4 . I$ by $90^{\circ}$, the signal $F 4$ will be delayed. The delay is equal to $90^{\circ}$ of a signal with period $4 \times T_{0}$, or equal to $T_{0}$. So also the output period is increased with this delay and now equals $128 \times T_{0}+T_{0}$. The prescaler division factor is now 129, and a dual-modulus operation is obtained by using only divide-by-two toggle-flipflops.

This new prescaler architecture is thus inherently faster than a conventional one. Instead of three full-speed $D$-flipflops that must be able to perform all logical functions, only one full-speed divide-by-two flipflop is needed. No extra logic is needed as in a $4 / 5$-divider. The next section will discuss the several building blocks used in the block diagram of Fig. 3.

## III. Circuit Design

## A. Full-Speed Divide-by-Two

The frequency-limiting building block in the architecture is of course the first divide-by-two block. The fastest standard CMOS $D$-flipflops up to now are the dynamic circuits of [6], [5], or the level-triggered latches of [7]. However, they both operate with a $5-\mathrm{V}$ power supply and their speed drops rapidly at lower voltages.

For example, we can make an estimation of the maximum frequency obtainable with the dynamic flipflop of [6] by analyzing the oscillation frequency of a three-inverter ring oscillator. This analogy is shown in Fig. 5. The toggle-flipflop can be regarded as being a three-inverter ring oscillator with some additional control transistors that will regulate the oscillation frequency to a certain value, i.e., half of the input toggle frequency. These control transistors will slow down the circuit, so the maximum input frequency obtainable with the dynamic $D$-flipflop is less then twice the oscillation frequency of the ring oscillator.

In our $0.7-\mu \mathrm{m}$ CMOS technology, the oscillation frequency of the ring oscillator is only 1.5 GHz at a $5-\mathrm{V}$ power supply, and only 0.8 GHz at 3 V . This means the maximum input frequency of the toggle-flipflop will be lower than twice


Fig. 4. Phase-selection principle: (a) Master/Slave divide-by-two flipflop and (b) waveforms.


Fig. 5. Analogy between: (a) dynamic CMOS toggle-flipflop and (b three-inverter ring oscillator.
this value, or 1.6 GHz at 3 V . To compare this with the results obtained in [6], the simulation is also performed for $1.2-\mu \mathrm{m}$ design rules. For a $5-\mathrm{V}$ supply, this renders an oscillation frequency 0.8 GHz . So the possible speed enhancement by going from a $1.2-\mu \mathrm{m}$ process to $0.7 \mu \mathrm{~m}$ is completely eliminated by lowering the supply voltage from 5 V to 3 V .

In this design, the output swing of the flipflop is limited. The circuit is based on a standard M/S ECL $D$-flipflop. A straightforward CMOS implementation of one section is shown in Fig. 6(a). To increase the maximum toggle frequency, the current source $I_{\text {bias }}$ can be omitted, and the source


Fig. 6. (a) CMOS implementation of an ECL flipflop, (b) one section of the high-frequency $D$-flipflop.
of transistors $M 1$ and $M 2$ is connected directly to the ground rail. To drive these transistors sufficiently into and out of saturation, the input signal swing must be large enough. In this design, a $1.5-\mathrm{V}_{\mathrm{ptp}}$ input amplitude was used. Since this prescaler can be driven directly by the VCO, this poses no problem because the VCO output swing is maximized for low phase noise [4]. So the circuits exploit the speed enhancement possible by the reduction in voltage swing from input to output. This circuit was already implemented successfully in a 4-V fixed-modulus prescaler [3]. Simulations indicate a speed improvement of $20 \%$ over a standard implementation. Since the second divide-by-two operates at only half the frequency, the smaller output swing poses no problems.

To fit this circuit into a 3-V power supply, another measure must be taken. To avoid the $V_{\mathrm{GS}}$ voltage drop across the diode load transistors $M 7$ and $M 8$, they must be folded to ground. They can then be replaced with NMOS transistors, which is another small advantage because of smaller parasitic capacitances. This circuit is shown in Fig. 6(b).

The sizing of this circuit is not straightforward. Because the circuit is biased with the dc level of the VCO signal, care has to be taken to ensure proper operation over all process variations. This was investigated with numerous Monte-Carlo simulations. Therefore, a SPICE model library was developed

TABLE I
(a) Process Parameters. (b) Transistor Sizes of the Full-Frequency Divide-by-Two Flipflop

|  | NMOS | PMOS |  |
| :---: | :---: | :---: | :---: |
| $V_{T}$ | 0.75 | -0.95 | $V$ |
| $\mu_{0}$ | 470 | 160 | $\mathrm{~cm}^{2} / V_{s}$ |
| $T_{O X}$ | 15 | 15 | $n m$ |

(a)

|  | W $[\mu \mathrm{m}]$ | $\mathrm{L}[\mu \mathrm{m}]$ |  | W $[\mu \mathrm{m}]$ | $\mathrm{L}[\mu \mathrm{m}]$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| M1 | 34.0 | 0.7 | M2 | 12.0 | 0.7 |
| M3 | 17.0 | 0.7 | M4 | 17.0 | 0.7 |
| M5 | 6.0 | 0.7 | M6 | 6.0 | 0.7 |
| M7 | 2.2 | 0.9 | M8 | 2.2 | 0.9 |
| M9 | 15.0 | 0.7 | M10 | 15.0 | 0.7 |

(b)
that contained the dependencies of the model parameters on the possible process variations. This library was used the generate statistically random models, which were used to simulate the circuit under varying process conditions. The 3- $\sigma$ variation of, e.g., the threshold voltage $V_{T}$ was 150 mV . The model parameters were generated consistent with reality, e.g., the oxide thickness of the NMOS and the PMOS model was kept the same. The operating temperature was also varied.

So the circuit was not sized to obtain a maximum operation speed with typical model parameters, but to be robust for process variations and temperature changes. The operating point was chosen to guarantee a reasonable yield (e.g., 95\%) at a somewhat reduced frequency. Of course, the yield under real processing conditions cannot be predicted safely with this procedure, but certainly an improvement over a design with only typical parameter simulations is achieved.

The resulting transistor sizes, together with a summary of the most important process parameters, are shown in Table I. The optimized circuit has a simulated maximum toggle frequency of 2 GHz at 3 V . The output amplitude is approximately $0.7 \mathrm{~V}_{\mathrm{ptp}}$.

## B. Half-Speed Divide-by-Two

The second divide-by-two circuit must be an M/S toggle flipflop. Its design is based on the first divider, but the bias current source is not omitted. This is necessary to cope with the smaller input amplitude and the higher dc level of its input signal, which is the output signal of the first divider-bytwo. Since this divider operates at half the input frequency, the speed enhancement which resulted from omitting the bias current source is no longer necessary. The output amplitude is approximately $0.5 \mathrm{~V}_{\mathrm{ptp}}$.

## C. Phase-Selection

The phase-select circuitry is shown in Fig. 7. The selection of the correct signal is done in two stages. In a first stage both the in-phase $(I)$ and quadrature $(Q)$ signals are amplified


Fig. 7. Phase-selection circuitry.
in a differential-to-single-ended amplifier. This is necessary because the amplitude of the output signals of the second divide-by-two circuit is only $0.5 \mathrm{~V}_{\mathrm{ptp}}$. The amplifier can be switched between positive and negative amplification, thereby making a selection between the positive signals ( $F 4 . I$ and $F 4 . Q$ ) or the negative signals ( $\overline{F 4 . I}$ and $\overline{F 4 . Q}$ ). The control signals $C 1$ and $C 2$ are used for this.

The circuit schematic of this amplifier is shown in Fig. 8. By changing the polarity of the control signals $C$ and $\bar{C}$, the bottom current mirror can be coupled to the rest of the circuit in a positive or a negative mode. Because of the high dc level of the input signals, this configuration was not possible with a PMOS current mirror directly above the: input differential pair. The currents had to be mirrored down first.

A selection between the two remaining signals $F . I$ and $F . Q$ is made with three simple NAND-gates and the control signal $C 0$ (see Fig. 7). A very important aspect of this circuit is what happens at the transfer from one selection to another. Uncareful design can cause spikes in the signal $F 4$, resulting in an improper division by the divide-by- 32 block. A smooth conversion in $F 4$ must be guaranteed for all possible variations in processing or temperature and for all input frequencies. This is only important for the NAND-gates controlled by $C 0$, because the control signals $C 1$ and $C 2$ are changed when the second stage of the circuit has selected the other signal (i.e., when $C 0$ selects $F . I$ to be connected to $F 4, C 2$ is changed). The transients that occur when switching the amplifiers from one amplification mode to another are therefore not important.

For high input frequencies, the risk of creating spikes doesn't exist, because the NAND-gates do not react fast enough. However, for lower input frequencies, there is a possibility of spikes. A simulation of this is shown in Fig. 9. The following waveforms are shown from top to bottom: the signals $F . I$ and $F . Q$ (notice the $90^{\circ}$ delay of $F . Q$ ), the control signal $C 0$ and the resulting signal $F 4$. The simulation is performed with fast transistor models and at an operating frequency of 250 MHz , which corresponds to an input frequency of 1 GHz . When $C 0$ is low, the high-to-low transitions in $F 4$ are determined by the signal F.I. After $0 \rightarrow 1$ change of $C 0$, the transitions are determined by $F . Q$. This is indicated on the figure. However, if the control signal $C 0$ has a very steep slope, $F . I$ can be deselected (and the signal $F 4$ goes from high to low) before $F . Q$ is high enough. This will cause a negative spike in $F 4$, as shown on the bottom of Fig. 9.


Fig. 8. Switchable amplifier for phase-selection.


Fig. 9. Risk of spikes in $F 4$ at the transition from F4.I to F4.Q.

The presence of this effect is dependent on the exact time of arrival and on the slope of the change in $C 0$. The spike only occurs for a very critical time of arrival. But since the delay in $C 0$ cannot be controlled nor guaranteed, the possibility of having exactly that arrival time cannot be ruled out. One could think of controlling the control signal arrival time by inserting a clocked $D$-flipflop into the path of $C 0$. This flipflop could be clocked by, e.g., the signal $F 4$. But even in this case, the
delay of the flipflop is not guaranteed, and the risk of spikes is not eliminated.
However, the problem is solved more easily by lowering the slope of $C 0$. In Fig. 9 it can be seen that the spike disappears as the slope of $C 0$ lowers. So a very small buffer inverter is used to steer the control signals, in order to limit the slope. As for process variations, the range over which the slope can vary without the risk of spikes is very large. So the buffer inverter is


Fig. 10. Microphotograph of the IC.


Fig. 11. Input and output waveforms for both division factors.
designed such that a smooth transition in $F 4$ is guaranteed for all possible arrival times of $C 0$ and for all possible transistor processing variations and operating temperatures.

## D. Low-Speed Divide-by-32

This divider is an asynchronous divider that consists of a chain of five toggle-flipflops. The maximum operating frequency is one-fourth of the input frequency, so the dynamic flipflop proposed in [6], as already shown in Fig. 5(a), can be used.

## IV. Measurement Results

The circuit has been implemented in a standard $0.7-\mu \mathrm{m}$ CMOS process. A chip microphotograph is shown in Fig. 10. The die size, including bonding pads, is $1150 \times 550 \mu \mathrm{~m}^{2}$. Measurements were made at room temperature with the chip bonded on a ceramic substrate. The maximum input frequency of this technique is limited by the parasitic bondwire inductance and bondpad capacitance. The input signals were terminated with on-chip $200-\Omega$ resistances. This results in a small overshoot in the input transfer characteristic in compari-


Fig. 12. Measured maximum input frequency versus supply voltage.
son with a $50-\Omega$ termination, but the maximum input frequency is extended. The required differential input signal was easily made by inserting a small delay into one of the two inputs. This delay is not critical, since the applied phase shift (normally $180^{\circ}$ for a perfect differential signal) can be varied by more than $50^{\circ}$. In this prototype, the bias current for the high-speed flipflops and the switchable amplifier is supplied externally.

The IC consumes, output buffer not included, 8 mA . This is divided over the several building blocks as follows: full-speed divide-by-two: 2.5 mA ; half-speed divide-by-two: 1.5 mA ; phase-selection: 2.5 mA ; low-speed divide-by- $32: 1.5 \mathrm{~mA}$.

The measured maximum input frequency is up to 1.75 GHz at 3 V . The output signal for both division factors, together with the $1.75-\mathrm{GHz}$ input signal, is shown in Fig. 11. It can clearly be seen that the divide-by- 129 signal has a high-to-low transition that is delayed by one period of the input signal with respect to the divide-by- 128 signal. This measured result is about $10 \%$ less than what could be expected from simulations.


Fig. 13. Phase noise measurement. (a) System configuration. (b) Measurement result.

This difference is probably due to insufficient modeling of the high-frequency effects of the transistors.

As for the influence of processing variations, these could not be measured completely since only a limited number of samples were available. However, an indication of the robustness of the circuit is given by the influence of, e.g., the power supply voltage or the externally supplied biasing current on the operating frequency. The maximum input frequency versus supply voltage is shown in Fig. 12. Although this circuit was optimized for $3-\mathrm{V}$ operation, an input frequency as high as 2.65 GHz was measured with a $5-\mathrm{V}$ power supply. This proves that this circuit is capable of operation in future mobile communication circuits, i.e., in the frequency range of $2-2.5$ GHz .

The phase noise of this prescaler was measured with the HP3048A phase noise measurement system, with a configuration as shown in Fig. 13(a). The measurement results for a $1.28-\mathrm{GHz}$ input signal are shown in Fig. 13(b). This frequency was chosen because a very stable $10-\mathrm{MHz}$ reference was available. The measured output phase noise is $-111 \mathrm{dBc} / \mathrm{Hz}$ at 100 Hz offset, $-131 \mathrm{dBc} / \mathrm{Hz}$ at 1 kHz offset, and flattens for higher offset frequencies to a noise floor of $-142 \mathrm{dBc} / \mathrm{Hz}$. This corresponds to an equivalent input phase noise of -141 $\mathrm{dBc} / \mathrm{Hz}$ at on offset frequency of 600 kHz , which is more than enough for the GSM or DCS1800 systems.

## V. Conclusion

A high-frequency dual-modulus divide-by-128/129 prescaler has been developed in a standard $0.7-\mu \mathrm{m}$ CMOS technology. A new circuit topology has reduced the fullfrequency part of the prescaler to only one divide-by-two flipflop. Therefore, this prescaler can operate at the same speed as an asynchronous divider.

A new toggle-flipflop was developed, suitable for a $3-\mathrm{V}$ power supply voltage. The maximum input frequency is 1.75 GHz . The power consumption is only 8 mA , and the output phase noise is as low as $-131 \mathrm{dBc} / \mathrm{Hz}$ at 1 kHz offset.

## References

[1] J. Min, A. Rofourgan, H. Samueli, and A. A. Abidi, "An all-CMOS architecture for a low-power frequency-hopped $900-\mathrm{MHz}$ spread spectrum transceiver," in Proc. IEEE 1994 Custom Integrated Circuits Conf., May 1994, pp. 379-382.
[2] J. Crols and M. Steyaert, "A fully integrated $900-\mathrm{MHz}$ CMOS double quadrature downconvertor," in ISSCC Dig. Tech. Papers, San Francisco, Feb. 1995, pp. 136-137.
[3] J. Craninckx and M. Steyaert, "A $1.8-\mathrm{GHz}$ low-phase-noise voltage controlled oscillator with prescaler," IEEE J. Solid-State Circuits, vol. 30, pp. 1474-1482, Dec. 1995.
[4] ___, "Low-noise voltage controlled oscillators using enhanced LCtanks," IEEE Trans. Circuits Syst. II: Analog and Digital Signal Processing, vol. 42, pp. 794-804, Dec. 1995.
[5] R. Rogenmoser, Q. Huang, and F. Piazza, " $1.57-\mathrm{GHz}$ asynchronous and 1.4-GHz dual modulus $1.2-\mu \mathrm{m}$ CMOS prescalers," in Proc. IEEE 1994 Custom Integrated Circuits Conf., May 1994, pp. 16.3.1-4.
[6] R. Rogenmoser, N. Felber, Q. Huang, and W. Fichtner, "A $1.16-\mathrm{GHz}$ dual modulus $1.2-\mu \mathrm{m}$ CMOS prescaler," in Proc. IEEE 1993 Custom Integrated Circuits Conf., San Diego, May 1993, pp. 27.6.1-4.
[7] N. Foroudi and T. A. Kwasniewski, "CMOS high-speed dual-modulus frequency dividers for RF frequency synthesis," IEEE J. Solid-State Circuits, vol. 30, pp. 93-100, Feb. 1995.


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