ECEN325: Electronics
Summer 2018

Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

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Announcements & Reading

• HW5 due today
• Exam 2 on July 20

• MOSFET Reading
  • Razavi Ch6 – MOSFET Models
  • Razavi Ch7 – MOSFET Amplifiers
MOSFET Circuit Symbols

NMOS

- MOSFETs are 4-terminal devices
  - Drain, Gate, Source, & Body
- Body terminal generally has small impact in normal operation modes, thus device is generally considered a 3-terminal device
  - Drain, Gate, and Source are respectively similar to the Collector, Base, and Emitter of the BJT
- 2 complementary MOSFETS: NMOS, PMOS

PMOS

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\[ v_G \rightarrow v_D \quad i_D = i_S \quad i_B = 0 \]
\[ v_S \rightarrow v_B \quad i_S = i_D \]

\[ v_G \rightarrow v_S \quad i_G = 0 \quad i_S = i_D \quad i_B = 0 \]
\[ v_D \rightarrow v_B \quad i_D = i_S \]
NMOS Physical Structure

- **Source (S)**
- **Gate (G)**
- **Drain (D)**
- **Polysilicon**
- **Body (B)**

[Karsilayan]
CMOS Physical Structure

[Karsilayan]
The threshold voltage, $V_{TH}$, is the voltage at which an “inversion layer” is formed.

For an NMOS this is when the concentration of electrons equals the concentration of holes in the $p^-$ substrate.
The incremental channel charge density is equal to the gate capacitance times the gate-channel voltage in excess of the threshold voltage.

\[ Q = WC_{ox}(V_{GC} - V_{TH}) \]

where Capacitance per unit gate area: \( C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \)
Let $x$ be a point along the channel from source to drain, and $V(x)$ its potential; the expression above gives the charge density (per unit length).

\[
Q(x) = WC_{ox} \left[ V_{GS} - V(x) - V_{TH} \right]
\]
Drain Current Derivation: Charge Density and Current

The current that flows from source to drain (electrons) is related to the charge density in the channel by the charge velocity.

$\mathbf{I = Q \cdot v}$

[Razavi]
**Drain Current Derivation:**

**Triode Region (Small \( V_{DS} \)) Current Equation**

\[
V = +\mu_n \frac{dV}{dx}
\]

\[
I_D = Q(x)v = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}
\]

\[
\int_{x=0}^{x=L} I_D dx = \int_{V(x)=0}^{V(x)=V_{DS}} \mu_n C_{ox} W[V_{GS} - V(x) - V_{TH}]dV(x)
\]

\[
I_D = \mu_n C_{ox} \frac{W}{L} \left[ V_{GS} - V_{TH} - \frac{1}{2}V_{DS} \right] V_{DS}
\]
Triode or Linear Region

- Channel depth and transistor current is a function of the overdrive voltage, $V_{GS} - V_T$, and $V_{DS}$
- Because $V_{DS}$ is small, $V_{GC}$ is roughly constant across channel length and channel depth is roughly uniform

\[
I_{DS} = \frac{W}{L} \mu_n C_{OX} (V_{GS} - V_{Tn} - 0.5V_{DS})V_{DS}
\]

For small $V_{DS}$

\[
R_{DS} \approx \frac{1}{\frac{W}{L} \mu C_{ox} (V_{GS} - V_{Tn})}
\]
MOS Equations in Triode Region (Large $V_{DS}$)

Drain current: Expression used in SPICE level 1

$$I_{DS} = \frac{W}{L} \mu_n C_{OX} (V_{GS} - V_{Tn} - 0.5V_{DS})V_{DS}$$

Linear approximation

$$V_{DSat} = V_{GS} - V_{Tn}$$

This doesn't really happen
If $V_{GC}$ is always above $V_T$ throughout the channel length, the transistor current obeys the triode region current equation:

$$V_{GC}(x) = V_{GS} - V(x) = V_{GS} - V_{DS} \frac{x}{L}$$
Saturation Region Channel Profile

When $V_{DS} \geq V_{GS} - V_{TH} = V_{OV}$, $V_{GC}$ no longer exceeds $V_{TH}$, resulting in the channel “pinching off” and the current saturating to a value that is no longer a function of $V_{DS}$ (ideally).

$V_{GC}(x) = V_{GS} - V(x) = V_{GS} - V_{DS} \frac{x}{L}$
Saturation Region

- Channel "pinches-off" when $V_{DS} = V_{GS} - V_{TH}$ and the current saturates
- After channel charge goes to 0, the high lateral field "sweeps" the carriers to the drain and drops the extra $V_{DS}$ voltage

$$V_{GC}(x) = V_{GS} - V(x) = V_{GS} - V_{DS} \frac{x}{L}$$

$$I_{DS} = \mu_n C_{OX} \frac{W}{L} \left( V_{GS} - V_{Tn} - \frac{V_{DS}}{2} \right) V_{DS} \bigg|_{V_{DS} = V_{GS} - V_{Tn}}$$

$$V_{DSSat} = V_{GS} - V_{Tn}$$

$$I_{DS} = \frac{\mu_n C_{OX} W}{2L} \left( V_{GS} - V_{Tn} \right)^2$$
NMOS $I_D - V_{DS}$ Characteristics

$V_{OV} = V_{GS} - V_{TN}$

[Sedra/Smith]

Curve bends because the channel resistance increases with $v_{DS}$

Almost a straight line with slope proportional to $V_{OV}$

Triode $(v_{DS} \leq V_{OV})$

Saturation $(v_{DS} \geq V_{OV})$

Current saturates because the channel is pinched off at the drain end, and $v_{DS}$ no longer affects the channel.

$v_{GS} = V_t + V_{OV}$

$0$ $V_{DS_{sat}} = V_{OV}$ $v_{DS}$

$i_D$
MOS “Large-Signal” Output Characteristic

\[ i_D = \frac{1}{2} k_n \left( \frac{W}{L} \right) V_{OV4}^2 \]

\[ v_{DS} \leq v_{OV} \]  
Triode region

\[ v_{DS} \geq v_{OV} \]  
Saturation region

\[ v_{GS} = V_t + V_{OV4} \]

\[ v_{GS} = V_t + V_{OV3} \]

\[ v_{GS} = V_t + V_{OV2} \]

\[ v_{GS} = V_t + V_{OV1} \]

Note: \( V_{ov} = V_{GS} - V_T \)
What about the PMOS device?

- The current equations for the PMOS device are the same as the NMOS EXCEPT you swap the current direction and all the voltage polarities.

**NMOS**

Linear: \( I_{DS} = \frac{W}{L} \mu_n C_{OX} (V_{GS} - V_{Tn} - 0.5V_{DS})V_{DS} \)

Saturation: \( I_{DS} = \frac{W}{2L} \mu_n C_{OX} (V_{GS} - V_{Tn})^2 \)

**PMOS**

Linear: \( I_{SD} = \frac{W}{L} \mu_p C_{OX} (V_{SG} - |V_{Tp}| - 0.5V_{SD})V_{SD} \)

Saturation: \( I_{SD} = \frac{W}{2L} \mu_p C_{OX} (V_{SG} - |V_{Tp}|)^2 \)
PMOS \( I_D - V_{SD} \) Characteristics

\[ V_{OV} = V_{SG} - |V_{TP}| \]

[Karsilayan]
### NMOS DC Operation (w/ infinite $r_{out}$)

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- In transistor model, often combine $\mu_n C_{ox}$ term as a parameter $K_{P_N}$ with units $A/V^2$.
- In lab, we combine $\mu_n C_{ox}(W/L)$ term as a parameter $\beta_N$ with units $A/V^2$.
## PMOS DC Operation (w/ infinite $r_{out}$)

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