ECEN325: Electronics  
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A Graphical Approach to BJT Amplifier Design  

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Common Emitter Amp w/ Emitter Resistor

\[ A_v = -\frac{g_m \left( R_C \parallel R_L \right)}{1 + \frac{g_m R_{E1}}{\alpha}} \]

\[ R_{in} = R_B \parallel \left( r_\pi + (\beta + 1)R_{E1} \right) \]

\[ R_{out} = R_C \]
Typical Design Specifications

- Loaded voltage gain, $A_v$
- Max output swing, $v_{omax}$
  - This must be satisfied at a given linearity (total harmonic distortion)
- Input and output resistance, $R_{in} \& R_{out}$
- Power Supply, $V_{CC}$
How to set DC Biasing Conditions?

- In order to meet all design specifications, the DC biasing conditions \((I_C, R_C)\) must be set appropriately.

- Can transform design specifications into functions of \(I_C\) & \(R_C\) and graph them to find acceptable solution space.
$R_{in}, V_{CC}, \text{ & Neg. } v_{omax} \text{ Specifications}$

- $R_{in}$ Spec

\[ R_{in} = R_B \| (r_\pi + (\beta + 1)R_{E1}) \approx \beta R_{E1} \]

\[ R_{E1} \approx \frac{R_{in}}{\beta} \]

- Input resistance is primarily set by $R_{E1}$
R_{in}, V_{CC}, & Neg. v_{omax} Specifications

- Need a minimum V_{CE} to keep transistor in active mode with maximum negative swing

  Set \( V_{CE_{\text{min}}} = 500\text{mV} \)
  (w/ 200mV design margin)

- V_{CC} Spec (w/ max negative swing)

\[
V_{CC} = \frac{I_C}{\alpha} R_{E1} + V_{CE_{\text{min}}} + v_{o_{\text{max}}} + I_C R_C
\]

\[
V_{CE_{\text{min}}} = V_{CC} - I_C R_C - v_{o_{\text{max}}} - \frac{I_C}{\alpha} R_{E1} \geq 500\text{mV}
\]
\( R_{in}, V_{CC}, \ & \text{Neg. } v_{omax} \) Specifications

- Can solve for \( I_C \)

\[
I_C \leq \frac{V_{CC} - v_{omax} - 0.5V}{R_C + \frac{R_{E1}}{\alpha}}
\]

- Combining \( R_{in} \) spec

\[
R_{E1} \approx \frac{R_{in}}{\beta}
\]

\[
I_C \leq \frac{V_{CC} - v_{omax} - 0.5V}{R_C + \frac{R_{in}}{\alpha \beta}}
\]

- Minimum negative AC Swing constraint sets an upper bound on \( I_C \)
Pos. \( v_{o\text{max}} \) Specification

- Need to insure with a positive swing that the output signal doesn’t clip the power supply

\[
V_{CC} - I_C R_C + v_{o\text{max}} \leq V_{CC}
\]

\[
I_C \geq \frac{v_{o\text{max}}}{R_C}
\]

- Positive AC Swing constraint sets a lower bound on \( I_C \)
- Additional linearity constraint (harmonic distortion) generally sets a tighter bound
\[ |A_v| = \left| \frac{v_o}{v_i} \right| \leq \frac{g_m \left( \frac{R_C}{R_L} \right)}{1 + \frac{g_m R_{E1}}{\alpha}} \leq \frac{\frac{I_C}{V_{th}} \left( \frac{R_C}{R_L} \right)}{1 + \left( \frac{I_C}{V_{th}} \right) \frac{R_{E1}}{\alpha}} \]

\[ I_C \geq \frac{|A_v V_{th} \left( \frac{R_C}{R_L} - \frac{|A_v| R_{E1}}{\alpha} \right)}{R_C \left( R_L - |A_v| R_{in} \right) \alpha} \]

- Gain constraint sets a lower bound on \( I_C \)
Harmonic Distortion Specification

- Need a minimum amount of bias current to insure that the AC swing doesn’t distort

Model a as a system which distorts

\[ i_c = a_1 v_{be} + a_2 v_{be}^2 + a_3 v_{be}^3 + \ldots \]

where \( a_1 = g_m \), \( a_2 = \frac{1}{2} \frac{I_{CQ}}{V_{th}} \), \( \ldots \)

Here \( v_{be} = v_b - v_e \approx v_b - f_i c \)

where \( f = R_E \)
Harmonic Distortion Specification

We want to express $i_c$ as a function of $v_b$ because that is our input

$$i_c = b_1 v_b + b_2 v_b^2 + b_3 v_b^3 + \ldots$$

Can show that

$$b_1 = \frac{g_m}{1 + g_m R_E}, \quad b_2 = \frac{I_{CQ}}{2 v^2_{th} (1 + g_m R_E)^3}, \quad \ldots$$

- For single-ended amplifiers with low-distortion, HD2 will dominate the distortion terms

The second-order harmonic distortion is

$$HD2 = \frac{1}{2} b_2 \frac{i_{c_{max}}}{b_1} = \frac{1}{4} \left( \frac{1}{1 + g_m R_E} \right) \left( \frac{i_{c_{max}}}{I_{CQ}} \right)$$
Harmonic Distortion Specification

To satisfy a given HD2 specification

\[ i_{c_{\text{max}}} \leq 4HD2 \left(1 + g_m R_E \right) I_{CQ} \]

\[ I_C \geq \frac{v_{o_{\text{max}}}}{R_C} \approx \frac{v_{o_{\text{max}}}}{4HD2 \left( \frac{I_C}{V_{th}} \right) R_E} \]

\[ I_C \geq \frac{1}{2} \sqrt{\frac{V_{th} v_{o_{\text{max}}}}{R_C R_E HD2}} \]

Using \[ R_E \approx \frac{R_{\text{in}}}{\beta} \]

\[ I_C \geq \frac{1}{2} \sqrt{\frac{V_{th} v_{o_{\text{max}}}}{R_C R_{\text{in}} HD2}} \]

- HD2 will dominate, but is not the only distortion term
- For a -30dB THD, perhaps set HD2 to -40dB or (0.01)
Output Resistance Specification

- Neglecting transistor output resistance, $R_{\text{out}}$ is determined by $RC$

\[ R_C \leq R_{\text{out,spec}} \]
Neg. Swing, Rin, $V_{CC}$:  
\[ I_C \leq \frac{V_{CC} - v_{o\text{max}} - 0.5V}{R_C + \frac{R_{in}}{\alpha\beta}} \]

Pos. Swing:  
\[ I_C \geq \frac{v_{o\text{max}}}{R_C} \]

Gain:  
\[ I_C \geq \frac{|A_v|V_{th}}{R_C \left( R_L - \frac{|A_v|R_{in}}{\alpha\beta} \right)} \]

Harmonic Distortion:  
\[ I_C \geq \frac{1}{2} \sqrt{\frac{V_{th}v_{o\text{max}}}{R_C R_{in} HD^2}} \]

Output Resistance:  
\[ R_C \leq R_{out,\text{spec}} \]
Design Example - Specifications

- $|A_v| \geq |-8|$  
- $R_{in} \geq 200k\Omega$  
- $R_{out} \leq 30k\Omega$  
- $V_{omax} = 20mV_{pk}$ w/ THD $\leq -30$dB  
- $V_{CC} = 5V$
Design Equation Plots

- Pick a design point in the middle for margin
- $I_C = 78 \mu A$, $R_C = 24k \Omega$

Plots done with $\beta = 110$ due to low current level necessary for high $R_{in}$
DC Operating Points

- DC bias points must be reasonable for the circuit to work as designed!
AC Gain, Rin, & Rout

- $|A_v| = 19.2 \text{dB} = 9.12$

- $R_{in} = 106.6 \text{dB} \Omega = 214 \text{k} \Omega$

- $R_{out} = 87.7 \text{dB} \Omega = 24.0 \text{k} \Omega$
Transient & Distortion

- Output with swing $> v_{\text{omax}}$

- FFT of output signal

<table>
<thead>
<tr>
<th>HARMONIC FREQUENCY</th>
<th>FOURIER COMPONENT</th>
<th>NORMALIZED COMPONENT</th>
<th>PHASE (DEG)</th>
<th>NORMALIZED PHASE (DEG)</th>
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TOTAL HARMONIC DISTORTION = 1.080592E-01 PERCENT
This is equal to a THD of -59.3dB.
Adding $R_{E2}$ to Stabilize DC Biasing

- Adding RE2 can help to make the DC biasing less sensitive to the absolute transistor Beta value
  - Assume I want $I_C \approx 80 \mu A$
  - While the nominal $\beta$ is 110, assume that it can vary from 70-200
  - What is the difference in designs with $R_{E2} = 0$ and with 1V across $R_{E2}$?
    
    $\beta \sim 70$ $\beta \sim 110$ $\beta \sim 200$

<table>
<thead>
<tr>
<th>Beta</th>
<th>$I_C$ (No $R_{E2}$)</th>
<th>% Diff. from $\beta=110$</th>
<th>$I_C$ (w/ 1V $R_{E2}$)</th>
<th>% Diff. from $\beta=110$</th>
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<tbody>
<tr>
<td>70</td>
<td>53 $\mu A$</td>
<td>-32.1%</td>
<td>69 $\mu A$</td>
<td>-12.7%</td>
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<td>110</td>
<td>78 $\mu A$</td>
<td>N/A</td>
<td>79 $\mu A$</td>
<td>N/A</td>
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<tr>
<td>200</td>
<td>116 $\mu A$</td>
<td>48.7%</td>
<td>88 $\mu A$</td>
<td>11.4%</td>
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</table>

- What is the impact on the graphical design procedure?
R\text{in}, V_{CC}, \& \text{Neg. } v_{\text{omax}} \text{ Specs w/ } R_{E2}

- The only equation impacted is the Neg. $v_{\text{omax}}$
- Need a minimum $V_{CE}$ to keep transistor in active mode with maximum negative swing

$$V_{CE\text{min}} = 500 \text{mV}$$
(w/ 200mV design margin)

- $V_{CC}$ Spec (w/ max negative swing)

$$V_{CC} = \frac{I_C}{\alpha} (R_{E1} + R_{E2}) + V_{CE\text{min}} + v_{\text{omax}} + I_C R_C$$

$$V_{CE\text{min}} = V_{CC} - I_C R_C - v_{\text{omax}} - \frac{I_C}{\alpha} R_{E1} - I_E R_{E2} \geq 500 \text{mV}$$
R_{in}, V_{CC}, & Neg. v_{omax} Specs w/ R_{E2}

- Can solve for I_{C}, assuming a V_{RE2} across R_{E2}

\[ I_{C} \leq \frac{V_{CC} - v_{omax} - 0.5V - V_{RE2}}{R_C + \frac{R_{E1}}{\alpha}} \]

- Combining R_{in} spec

\[ R_{E1} \approx \frac{R_{in}}{\beta} \]

\[ I_{C} \leq \frac{V_{CC} - v_{omax} - 0.5V - V_{RE2}}{R_C + \frac{R_{in}}{\alpha \beta}} \]

- Minimum negative AC Swing constraint sets an upper bound on I_{C} which is reduced with R_{E2}
Key CE Amp Design w/ $R_{E2}$ Eq. Summary

Neg. Swing, Rin, $V_{CC}$: 
$$I_C \leq \frac{V_{CC} - v_{o \text{max}} - 0.5V - V_{RE2}}{R_C + \frac{R_{in}}{\alpha \beta}}$$

Pos. Swing: 
$$I_C \geq \frac{v_{o \text{max}}}{R_C}$$

Gain: 
$$I_C \geq \frac{|A_v|V_{th}}{R_C \left| R_L - \frac{|A_v|R_{in}}{\alpha \beta} \right|}$$

Harmonic Distortion: 
$$I_C \geq \frac{1}{2} \sqrt{\frac{V_{th}v_{o \text{max}} \beta}{R_C R_{in} HD^2}}$$

Output Resistance: 
$$R_C \leq R_{out,spec}$$
Common Collector Amp

\[
A_v = \frac{R_E \| R_L}{r_e + R_E \| R_L}
\]

\[
R_{in} = R_B \| \left( \rho_\pi + (\beta + 1)R_E \| R_L \right)
\]

\[
R_{out} = R_E \left[ r_e + \frac{R_S \| R_B}{\beta + 1} \right]
\]
Typical Design Specifications

- Loaded voltage gain, $A_v$
- Max output swing, $v_{omax}$
  - This must be satisfied at a given linearity (total harmonic distortion)
- Input and output resistance, $R_{in}$ & $R_{out}$
  - If you know $R_L$, then $R_{out}$ spec is somewhat redundant with $A_v$ spec
- Power Supply, $V_{CC}$
How to set DC Biasing Conditions?

- In order to meet all design specifications, the DC biasing conditions ($I_E$, $R_E$) must be set appropriately.

- Can transform design specifications into functions of $I_E$ & $R_E$ and graph them to find acceptable solution space.
R_{in} Specification

- **R_{in} Spec**

\[
R_{in} = R_B \|(r_\pi + (\beta + 1)(R_E \| R_L)) \approx \beta(R_E \| R_L)
\]

\[
R_E \geq \left( \frac{\beta}{R_{in,spec}} - \frac{1}{R_L} \right)^{-1}
\]

- Input resistance is primarily set by \(R_E\) and somewhat independent of \(I_E\)
Neg. $v_{o\text{max}}$ Specification

- Need to insure with a negative swing that the output signal doesn’t clip the power supply

$$I_E R_E - v_{o\text{max}} \geq 0V$$

- Negative AC Swing constraint sets a lower bound on $I_E$
- Additional linearity constraint (harmonic distortion) generally sets a tighter bound
Pos. $v_{o\text{max}}$ & $V_{CC}$ Specifications

- Need a minimum $V_{CE}$ to keep transistor in active mode with maximum positive swing

  \[ V_{CE\text{min}} = 500\text{mV} \]

  (w/ 200mV design margin)

- $V_{CC}$ Spec (w/ max positive swing)

- Maximum positive AC swing constraint sets an upper bound on $I_E$

\[
V_{CC} = I_E R_E + v_{o\text{max}} + V_{CE\text{min}}
\]

\[
V_{CE\text{min}} = V_{CC} - I_E R_E - v_{o\text{max}} \geq 500\text{mV}
\]

\[
I_E \leq \frac{V_{CC} - v_{o\text{max}} - 0.5V}{R_E}
\]
$A_v = \frac{R_E \parallel R_L}{r_e + R_E \parallel R_L} = \frac{R_E \parallel R_L}{\frac{V_{th}}{I_E} + R_E \parallel R_L}$

$I_E \geq \frac{A_v V_{th}}{(R_E \parallel R_L)(1 - A_v)}$

- Gain constraint sets a lower bound on $I_E$
Harmonic Distortion Specification

- Following a similar procedure as the Common-Emitter Amp, can relate the HD2 specification to the ratio of AC current $i_c$ to $I_{CQ}$

$$i_c \leq 4(HD2)(1 + g_m (R_E || R_L))I_{CQ}$$

Now, assuming a high $\beta$ or $\alpha \approx 1$

$$i_e \leq 4(HD2)(1 + g_m (R_E || R_L))I_{EQ}$$

$$I_{EQ} \geq \frac{\frac{V_{o_{max}}}{R_E || R_L}}{4(HD2)(1 + g_m (R_E || R_L))} \approx \frac{\frac{V_{o_{max}}}{R_E || R_L}}{4(HD2)\left(\frac{I_{EQ}}{V_{th}}\right)(R_E || R_L)}$$

$$I_{EQ} \geq \frac{1}{2(R_E || R_L)} \sqrt{\frac{V_{th} V_{o_{max}}}{HD2}}$$

- HD2 will dominate the distortion terms
- For a -30dB THD, perhaps set HD2 to -40dB or (0.01)
Key CC Amp Design Equation Summary

Rin: \[ R_E \geq \left( \frac{\beta}{R_{in,spec}} - \frac{1}{R_L} \right)^{-1} \]

Neg. vomax: \[ I_E \geq \frac{v_{o,\text{max}}}{R_E} \]

Pos vomax, Vcc: \[ I_E \leq \frac{V_{CC} - v_{o,\text{max}} - 0.5V}{R_E} \]

Gain: \[ I_E \geq \frac{A_vV_{th}}{(R_E || R_L)(1 - A_v)} \]

Harmonic Distortion: \[ I_E \geq \frac{1}{2(R_E || R_L)^2} \sqrt{\frac{V_{th}v_{o,\text{max}}}{HD2}} \]
Design Example - Specifications

- $A_v \geq 0.95$
- $R_{in} \geq 1k\Omega$
- $V_{omax} = 500mV_{pk}$ with $THD \leq -30dB$
  - Here I set $HD2=40dB$ or 0.01
- $V_{CC} = 5V$
- $R_L = 50\Omega$
• Pick a low $I_E$ design point to save power
• $I_E=20$ mA, $R_E=100\Omega$

Plots done with $\beta=170$ due to high current level
• DC bias points must be reasonable for the circuit to work as designed!
AC Gain & Rin

- $|A_v| = -0.38\, \text{dB} = 0.96$
- $R_{\text{in}} = 67.6\, \text{dB}\Omega = 2.4k\Omega$
Transient & Distortion

- Output with swing > $v_{\text{omax}}$

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</tr>
</thead>
<tbody>
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<td>COMPONENT</td>
<td>(deg)</td>
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TOTAL HARMONIC DISTORTION = 1.088050E+00 PERCENT