A MULTI-BAND PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER

A Thesis

by

SAMUEL MICHAEL PALERMO

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 1999

Major Subject: Electrical Engineering

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Approved as to style and content by:

José Pineda de Gyvez (Chair of Committee)	Edgar Sánchez-Sinencio (Member)
Sherif H. K. Embabi (Member)	Duncan M. H. Walker (Member)

Chanan Singh
(Head of Department)

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Major Subject: Electrical Engineering

ABSTRACT

A Multi-Band Phase-Locked Loop Frequency Synthesizer. (August 1999)
Samuel Michael Palermo, B.S., Texas A&M University
Chair of Advisory Committee: Dr. José Pineda de Gyvez

A phase-locked loop (PLL) frequency synthesizer suitable for multi-band transceivers is proposed. The multi-band PLL frequency synthesizer uses a switched tuning voltage-controlled oscillator (VCO) that covers a frequency range of 111 to 297MHz with a low average conversion gain of 41.71MHz/V. A key design feature of the multi-band PLL frequency synthesizer is that the VCO tuning switches are controlled only by the normal loop dynamics. No external control is needed for the synthesizer to switch to different bands of operation. The multi-band PLL frequency synthesizer is implemented in a standard 1.2μm CMOS technology using a 2.7V supply. The frequency synthesizer has a measured frequency range of 111 to 290MHz with phase noise up to –96dBc/Hz at a 50kHz carrier offset. Experimental comparisons of the multi-band PLL frequency synthesizer with a similar classic digital PLL frequency synthesizer show the multi-band synthesizer to have a 20% greater frequency range, an average 7.3dB superior phase noise performance, and similar acquisition time.

DEDICATION

This work is dedicated to my wife, Shawn. Her gracious support and countless sacrifices have allowed me to complete this great task.

ACKNOWLEDGMENTS

I would like to thank my family for the support they have given over the years. Especially my wife for providing me the gift of her infinite love. My mother deserves special thanks for the endless encouragement. The support from my father is also greatly appreciated.

I am extremely grateful for the contributions of all my committee members to my research. They have provided me with the tools necessary for the research through their courses and technical discussions. My advisor, Dr. José Pineda de Gyvez, deserves special acknowledgment for the support and guidance he has provided me throughout the years.

I thank all of the students in the Analog and Mixed Signal Group for their friendship and technical support. I am extremely indebted to Antonio Mondragon for the CADENCE support, Fikret Dülger for the high frequency design and testing suggestions, and Ajay Kanji for the printed circuit board help.

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INTRODUCTION

The explosion of the wireless communications industry into areas such as cellular telephony, wireless local area networks, and the Global Positioning System has led to several wireless standards operating at frequencies ranging from 900-5200MHz. Multi-standard transceivers used for these systems should be able to operate over a wide frequency range with minimal amounts of duplicated hardware[1]. A critical element of any transceiver is the frequency synthesizer(FS). A multi-standard frequency synthesizer must be able to synthesize different bands of frequencies for the different wireless standards. Instead of a typical single-band frequency synthesizer that is commonly used to synthesize a narrow frequency band, a multi-band frequency synthesizer is needed to synthesize multiple frequency bands. A multi-band frequency synthesizer must be able to synthesize a wide range of frequencies while satisfying strict phase noise specifications. This poses a challenging design problem. The typical phase-locked loop (PLL) frequency synthesizers used in transceivers are normally designed and optimized for narrow band operation. Architectural changes should be made to the typical loop structure in order to achieve operation over a wide frequency range for multi-band transceivers.

Phase-Locked Loops

The phase-locked loop circuit has been around for quite some time. Appleton's work on oscillator synchronization in the early 1920s and de Bellescize's work in the area of coherent communications in the early 1930s introduced the phase-locked loop to the scientific community[2]. The basic phase-locked loop circuit synchronizes an output signal with an input reference signal. The output signal has the same frequency as the input reference signal and also a constant phase difference. A block diagram of a simple phase-locked loop is given in Figure 1.

This thesis follows the style and format of *IEEE Transactions on Circuits and Systems.*

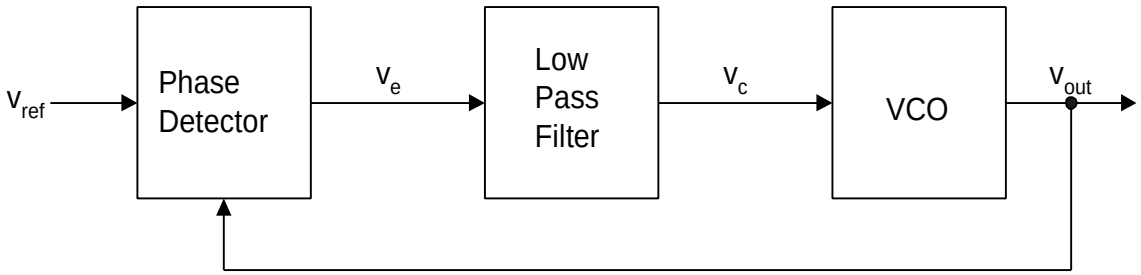

Figure 1 - PLL Block Diagram

The phase-locked loop works by comparing the reference signal, v_{ref}, with the voltage-controlled oscillator's (VCO) output, v_{out}. An error signal, v_e, is produced that is proportional to the phase difference of the reference signal and the output signal. This error signal is filtered to generate the voltage-controlled oscillator control voltage, v_c. The loop is setup in a negative feedback fashion so the voltage-controlled oscillator control voltage will force the output of the voltage-controlled oscillator to lock with the input reference signal within certain frequency limits.

Advances in integrated circuit technology allowed phase-locked loop circuits to be used commonly in many areas such as communications, wireless systems, consumer electronics, and motor control[2-7]. The phase-locked loop is used in motor control to synchronize the motor speed to a reference frequency with extreme accuracy[2,8]. The phase-locked loop is used in the area of consumer electronics for applications ranging from television sets to microprocessors. The phase-locked loop performs the horizontal and vertical synchronization and color subcarrier reconstruction in television sets[7]. The phase-locked loop is used in microprocessors and other digital circuits to generate a low jitter clock signal[3]. Typical communications applications include clock and data recovery, coherent demodulation of amplitude (AM), frequency (FM), and phase-modulated (BPSK) signals, phase-locked loop receivers, and frequency synthesis[3,5,9].

Phase-Locked Loop Frequency Synthesizers

The PLL can be used as a frequency synthesizer by placing a loop divider in the feedback path as shown in Figure 2.

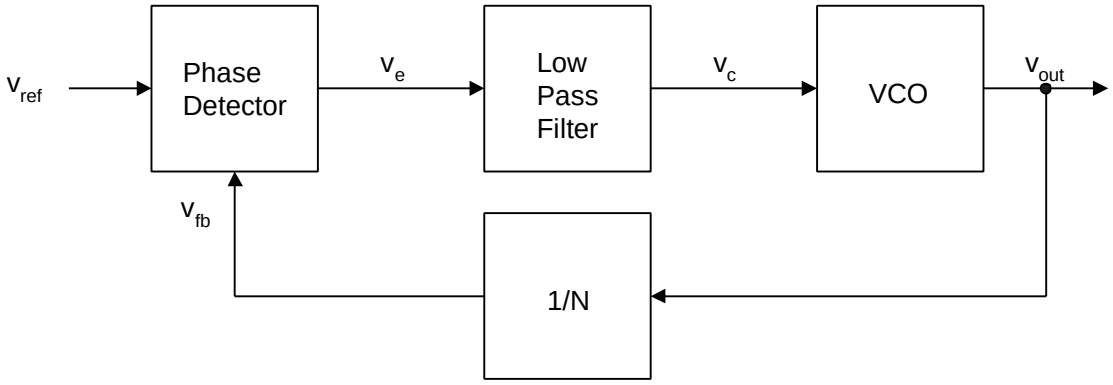

Figure 2 - Phase-Locked Loop Frequency Synthesizer

Here the output frequency, f_{out}, is related to the input reference frequency, f_{ref}, by the following equation:

$$f_{out} = Nf_{ref} = f_0 + v_c K_{VCO} \qquad \textbf{(1)}$$

where f_0 is the VCO center frequency and K_{VCO} is the VCO conversion gain. Adjusting the division factor or modulus can change the frequency that the PLL synthesizes.

The economics of the electronics industry has led to a trend towards increased integration. One goal of many communications system engineers and integrated circuit designers is to have a single-chip transceiver. This chip would perform functions such as radio frequency (RF) up/down conversion and baseband digital signal processing on the same die with no external components. At the present time this goal has not yet been achieved at the production level. This is due to the fact that many of the filtering components used in the RF up/down conversion remain off-chip. Also, the majority of the RF up/down conversion is done in bipolar technology, while most of the digital

signal processing is performed with a complementary metal-oxide semiconductor (CMOS) technology. Combining these two technologies is costly.

The quality of the frequency synthesizer is a key element in the design of a transceiver. Typically, the frequency synthesizers used in radio frequency communications are designed in a bipolar technology with off-chip filtering components. Recent research efforts have been directed towards achieving a fully integrated RF CMOS frequency synthesizer. Table 1 shows the recent research done in the area of PLL frequency synthesizer design.

With the increased interest in multi-band systems, a frequency synthesizer that operates over multiple bands becomes a necessity. There are many challenges faced in designing a multi-band CMOS frequency synthesizer. The research efforts in [10-15] concentrating on narrow (single) band frequency synthesizers and do not have the frequency range necessary for multi-band systems. A wide frequency range is achieved in [16]. However, this is still not wide enough to synthesize the frequencies necessary in multi-band systems. A suitable frequency range is achieved in [17]. However, the power supply of 5V is not suitable for many portable applications. The work done in [18] achieved a very wide frequency range. However, it was achieved with a translinear architecture that cannot be realized effectively in a typical CMOS process. In [19], complex digital to analog converter control is used to achieve a wide frequency range. A double-loop architecture is used to achieve a wide frequency range in [20]. However, this double-loop architecture requires effectively twice the circuitry as the standard single-loop phase-locked loop. This is also observed in typical dual-band synthesizers on the market today. They utilize multiple phase-locked loops with narrow band voltage-controlled oscillators that operate at different center frequencies[21].

Table 1 - State-of-the-Art PLL Implementations

Source	Frequency Range	Phase Noise	Architecture	Technology	Power Supply	Integration Level
[10]	1.4-1.6GHz	-115dBc/Hz @ 600kHz	Single-Loop (Switched Tuning)	0.6µ CMOS	3V	Full
[11]	865-1000MHz	-110dBc/Hz @ 200kHz	Single-Loop	0.5µ CMOS	3.3V	Off-Chip Filter
[12]	1.7-1.9GHz	-123dBc/Hz @ 600kHz	Single-Loop	0.4µ CMOS	3V	Full
[13]	1.7-2.3GHz	Not Reported	Single-Loop	0.5µ BiCMOS	3V	Off-Chip Filter
[14]	902-928MHz	-90dBc/Hz @ 1kHz	Single-Loop	CMOS S-? Bipolar PFD/Divider	3V	2 Chips Off-Chip Filter & VCO
[15]	700-1000MHz	-80dBc/Hz @ 100kHz	Single-Loop	0.8µ CMOS	5V	Off-Chip Filter
[16]	820-1560MHz	Not Reported	Single-Loop	0.25µ CMOS	1.8V	Full
[17]	5-110MHz	Not Reported	Single-Loop	0.8µ CMOS	5V	Full
[18]	1-150MHz	-80dBc/Hz @ 100kHz	Translinear	0.6µ BiCMOS	3V	Full
[19]	0.3-165MHz	Not Reported	Single-Loop (Complex D/A Control)	0.8µ CMOS	3-5V	Full
[20]	950-2150MHz	-94dBc/Hz @ 10kHz	Double-Loop	$f_T \approx 9$GHz Bipolar	5V	Full

A multi-band frequency synthesizer should be realized in a manner that does not increase the loop complexity significantly. An optimal design would be implemented in a typical CMOS process using the power supplies typically found in portable products. A design approach that minimizes the amount of replicated circuitry is to increase the VCO tuning range in such a way that the PLL loop dynamics are not drastically affected.

The integrated VCOs used in frequency synthesizers generally have limited tuning ranges or conversion gain, K_{VCO}. The most common integrated VCO used in RF systems is the LC oscillator because of superior phase noise performance[22]. However, this type of oscillator suffers from a very limited tuning range because it is tuned with varactor capacitors that generally make up only 25% of the total tank capacitance. One way to increase the tuning range of the oscillator is to discretely switch in different capacitive or inductive loads. The use of switched tuning elements to increase the oscillator's tuning range is an old design technique that been seen in recent research[10,23,24]. The concept of switched tuning is illustrated in Figure 3.

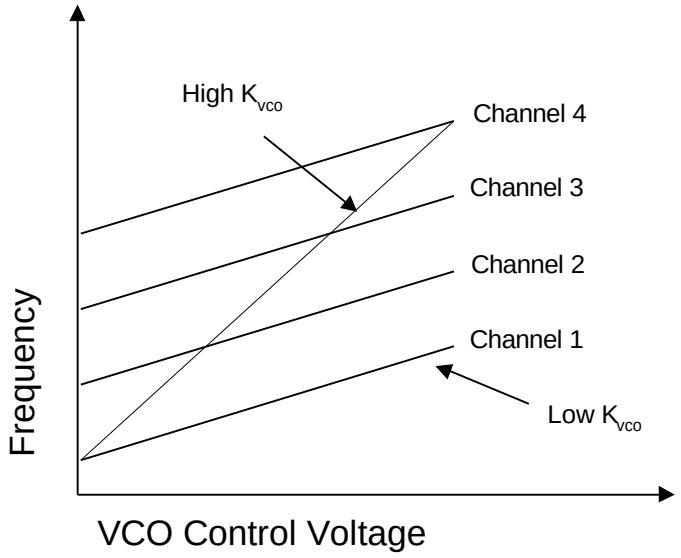

Figure 3 - Utilizing Switched Tuning to Achieve a Wide Tuning Range

Here a wide frequency range is realized by splitting the entire range into four bands of operation. The oscillator changes between the different bands of operation by discretely switching in the different loads. The low K_{VCO} multi-band voltage-controlled oscillator can be used to synthesize the same frequencies as a high K_{VCO} oscillator through the use of switched tuning. This property of switched tuning also aids in the noise performance of the oscillator.

Noise in the control path of a voltage-controlled oscillator translates directly into phase noise in the output signal by frequency modulation. This phase noise degrades the synthesizer's performance and causes the communication system to have a higher bit error rate (BER). If the noise on the control line of the voltage-controlled oscillator is modeled as $V_m \cos w_m t$, the output of the voltage-controlled oscillator will be the following assuming a narrow band frequency modulation approximation[22]:

$$v_{out}(t) \approx A_0 \cos w_0 t + \frac{A_0 V_m K_{VCO}}{2w_m}\left[\cos(w_0 + w_m)t - \cos(w_0 - w_m)t\right] \quad \textbf{(2)}$$

The noise power at $w_0 \pm w_m$ with respect to the carrier power is equal to the following:

$$L(w_m) = \frac{V_m^2}{4}\left(\frac{K_{VCO}}{w_m}\right)^2 \quad \textbf{(3)}$$

Therefore, the phase noise due to control line noise is directly proportional to the square of the voltage-controlled oscillator's conversion gain, K_{VCO}.

The voltage-controlled oscillator's conversion gain must be very large to synthesize a wide range of frequencies if the architecture of Figure 2 is used for a multi-band frequency synthesizer. However, such large conversion gains are not available with conventional integrated voltage-controlled oscillators. Also, the previous analysis shows that this will result in poor phase noise performance. This makes a phase-locked loop with a switched tuning voltage-controlled oscillator ideal for a multi-band frequency

synthesizer because it can tune over a wide range while maintaining a low conversion gain. The system is to be designed with sufficient overlap between the frequency bands. This insures that no switching will take place after the multi-band phase-locked loop has acquired lock. The block diagram of a multi-band phase-locked loop frequency synthesizer utilizing a switched-tuning or multi-band voltage-controlled oscillator is shown in Figure 4.

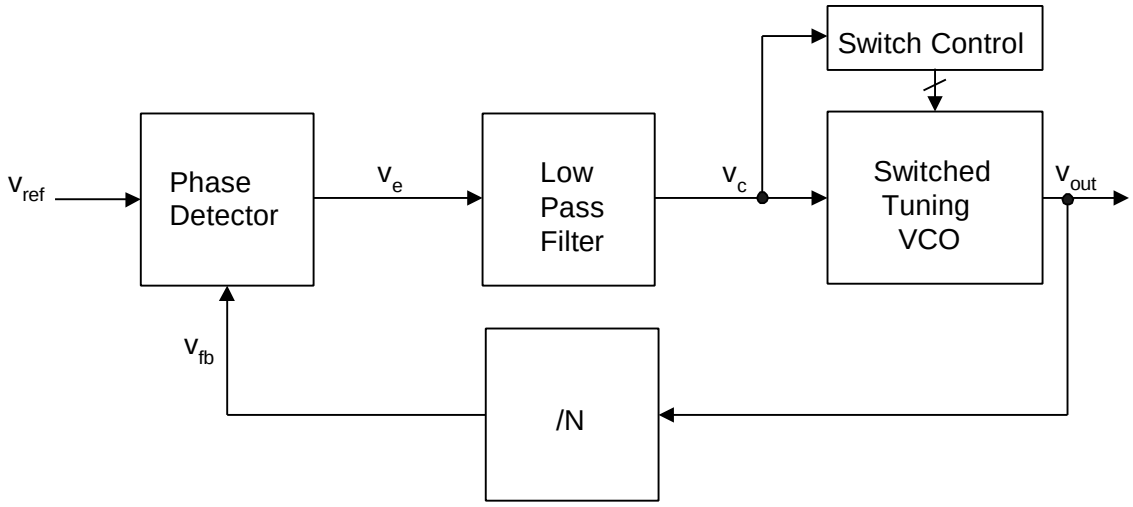

Figure 4 - Multi-Band Phase-Locked Loop Frequency Synthesizer Block Diagram

Here the output frequency, f_{out}, is related to the input reference frequency, f_{ref}, by the following:

$$f_{out} = Nf_{ref} = f_n + v_c K_{VCO} \qquad (4)$$

where f_n is the VCO center frequency for $n = 1,2,...,n$ bands.

Research Objectives

Most of the work presented up to date in fully integrated frequency synthesizer design has been with the traditional (single-band) VCOs [11-13]. While some work has been done with switched tuning oscillators [10,24], their effort was mostly concentrated

on overcoming process variations and not in designing multi-band frequency synthesizers. A multi-band frequency synthesizer realized using a PLL with a switched tuning VCO should be done in a manner that does not increase the loop complexity significantly. The synthesizer should be designed in a typical CMOS process using the power supplies typically found in portable products.

The main objective of this research is to design and implement a multi-band phase-locked loop frequency synthesizer. A synthesizer that operates from 100 to 300MHz is designed in a 1.2µ nwell CMOS process as a proof of concept that the switched-tuning VCO structure is suitable for a multi-band synthesizer. A key design feature in the multi-band phase-locked loop frequency synthesizer is that the switch control will be controlled only by the loop dynamics (VCO control voltage) – no external control is needed. This multi-band PLL frequency synthesizer poses several open-ended questions that need addressing for the optimal silicon implementation. The main research objectives can be enumerated in the following manner:

1. Mathematical formulation of the first integrated single-loop multi-band PLL frequency synthesizer.
2. Design of a fully integrated multi-band PLL frequency synthesizer.
3. IC Fabrication and testing of the multi-band PLL frequency synthesizer.
4. Experimental performance analysis of the multi-band PLL frequency synthesizer.

The first two objectives involve the analysis, design, and simulation of the multi-band phase-locked loop frequency synthesizer. Trade-offs regarding noise performance, frequency range, stability, and silicon area are studied. The design parameters are obtained through mathematical analysis and behavioral simulation. These design parameters are used to implement the multi-band PLL frequency synthesizer in a 1.2µ nwell CMOS process.

The third objective involves the layout, fabrication, and testing of the multi-band PLL frequency synthesizer. This objective is undertaken after the design of the system has been completed through the first objective. The layout is accomplished with good matching and high-frequency techniques. The integrated circuits are fabricated through the MOSIS foundry using the AMI1.2µ CMOS process. Three prototype chips are sent for fabrication. The first prototype chip includes the multi-band frequency synthesizer blocks for individual characterization. The second prototype chip includes the multi-band PLL frequency synthesizer. The third prototype chip has both the multi-band PLL frequency synthesizer and a wide band classic digital PLL frequency synthesizer for comparison. The prototype circuits will be tested in the Analog and Mixed Signal Group Laboratory. High frequency printed circuit boards will be developed to test the prototypes. The prototypes will be tested with the aid of external components and through measurement equipment.

The fourth objective involves the performance evaluation of the experimental prototypes. The building blocks will be evaluated for individual performance outside of the system. The multi-band PLL frequency synthesizer will be evaluated in terms of frequency range and phase noise performance. A comparison between the multi-band PLL frequency synthesizer and a wide band classic digital PLL frequency synthesizer will be made.

The following topics will be discussed in the remainder of the thesis:

- PLL Design Theory- The mathematics behind the linear and charge pump PLL are developed. PLL noise analysis is discussed. The charge pump PLL building blocks are described. Also, a general fully integrated PLL design procedure is presented.
- A Multi-Band Phase-Locked Loop Frequency Synthesizer- The multi-band PLL frequency synthesizer design methodology is presented. The mathematical and behavioral model is explained. The transistor level design and layout is also presented.

- Experimental Results- The experimental results of the three prototype chips are presented. A performance comparison is made between the multi-band and the classic digital PLL frequency synthesizers.
- Conclusions- The goals accomplished through the work of this thesis are summarized.

PLL DESIGN THEORY

In this section the basic operation of the phase-locked loop is explained, along with a presentation of frequency synthesizer architectures. A formal mathematical analysis for the linear and charge pump PLL is shown as well. It includes stability conditions and noise performance characteristics that shape the way the PLL is designed. These overall system design considerations are given in this section. Finally, the building blocks for a charge pump PLL are explained and a general fully integrated PLL system level design procedure is included.

PLL Operation

The phase-locked loop is a circuit that synchronizes the frequency generated by an oscillator with the frequency of a reference signal by means of the phase difference of the two signals. The oscillator's output has the same frequency as the input reference frequency and also a constant phase difference. The PLL utilizes three basic blocks to perform this phase and frequency synchronization.

The first block is the phase detector. The phase detector compares the phase difference between the input reference signal and the oscillator's output signal. The output of the phase detector is a function of the phase difference between the reference and output signal. The main difference between the classic digital PLL and the analog PLL is that the classic digital PLL uses logic gates to realize the phase detector, while the analog PLL uses a multiplier. A classic analog PLL is shown in Figure 5.

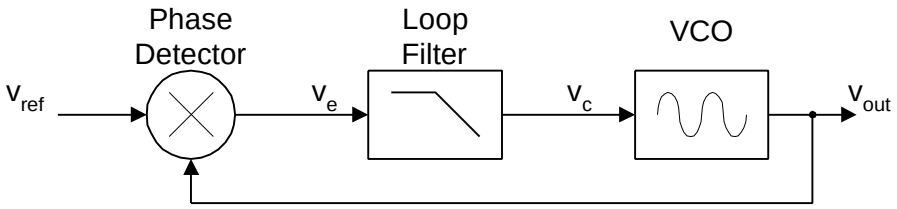

Figure 5 - Analog PLL Block Diagram

Assuming a sinusoidal reference frequency, $v_{ref}(t) = A\cos(w_r t + q_r)$, and a sinusoidal output signal, $v_{out}(t) = B\cos(w_o t + q_o)$, the phase detector output, v_e, is equal to the following:

$$v_e(t) = \frac{K_{mult}AB}{2}\left\{ \cos\left[(w_r - w_o)\, t + q_r - q_o\right] + \cos\left[(w_r + w_o)\, t + q_r + q_o\right] \right\} \qquad \textbf{(5)}$$

where K_{mult} is the conversion gain of the multiplier. This phase detector output has a low frequency component that is a function of the phase difference of the two signals and a high frequency component that is a function of the phase summation of the two signals.

The second block is the loop filter. The loop filter is a low pass filter that filters the output of the phase detector to produce the VCO control voltage, v_c. For the analog PLL, the loop filter removes the term in the phase detector output that is a function of the phase summation of the two signals in (5). In the classic digital PLL the loop filter averages the phase detector output.

The third block is the voltage-controlled oscillator. The voltage-controlled oscillator produces an output signal, v_{out}, with an angular frequency, w_{out}, that is controlled by the output voltage of the loop filter, v_c, by the following relationship:

$$w_{out}(t) = w_0 + \Delta w_{out}(t) = w_0 + K_{VCO} v_c(t) \qquad \textbf{(6)}$$

where w_0 is the center frequency of the VCO and K_{VCO} is the voltage-controlled oscillator's conversion gain. The output phase is equal to the integral over the frequency variation $\Delta w_{out}(t)$.

$$q_{out}(t) = \int \Delta w_{out}(t)\mathrm{dt} = K_{VCO} \int v_c(t)\mathrm{dt} \qquad \textbf{(7)}$$

The PLL has four basic regions of operation shown in Figure 6. These regions describe the PLL in dynamic and static states. The PLL is in a dynamic state when the output signal is not *locked* or synchronized with the reference frequency in frequency and phase. The PLL is in a static state when the output signal is locked with the reference frequency. The four regions of operation are the *hold range, pull-in range, pull-out range,* and the *lock range*.

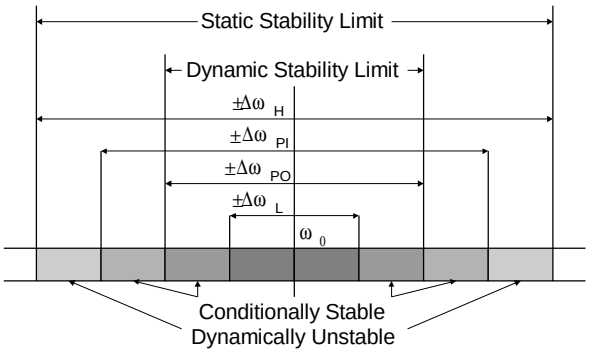

Figure 6 - PLL Regions of Operation

The hold range, Δw_H, describes the PLL in a static or locked state. The hold range is the frequency range in which a PLL can statically maintain phase tracking[7]. The PLL is initially locked with the reference signal. If the reference signal's frequency is slowly reduced or increased too much the PLL will loose lock at the edge of the hold range. The PLL is conditionally stable only within the hold range.

The pull-out range, Δw_{PO}, also describes the PLL in a static state. The pull-out range is the dynamic limit for stable operation[7]. The pull-out range is the value of a frequency step applied to the reference frequency that causes the PLL to unlock. The PLL is initially locked with the reference signal. If a frequency step that is less then the pull-out range is applied to the reference signal the PLL will remain in lock. However, if the frequency step exceeds the pull-out range, the PLL will not be able to track the output

signal and will fall out of lock. The PLL may acquire lock again, but it may be a slow pull-in process.

The pull-in range, Δw_{PI}, describes the PLL in a dynamic state or an acquisition mode. The pull-in range is the range within which a PLL will always become locked through the acquisition process[7]. The PLL is initially unlocked. The PLL will acquire lock if a reference frequency within the pull-in range is applied. However, if the reference frequency is outside the pull-in range, the PLL will not be able to lock onto the reference signal. The process of acquiring lock in the pull-in range may be a slow pull-in process. However, if the reference frequency is inside a subset of the pull-in range, the lock range, the PLL will acquire lock rapidly.

The lock range, Δw_{L}, is a subset of the pull-in range. The lock range is the frequency range in which a PLL locks within a single-beat note between the reference frequency and output frequency. The PLL is initially unlocked. The PLL will acquire lock within a beat-note between the reference frequency and the output frequency if a reference frequency within the lock range is applied. The lock time will be a slower pull-in process if a reference frequency outside of the lock range is applied. The normal operation of the PLL is generally restricted to the lock range.

Frequency Synthesizer Architectures

A frequency synthesizer is a system that generates different output frequencies from a given input reference frequency. The majority of frequency synthesizers utilize a classic digital PLL with a loop divider in the feedback path as shown in Figure 7. This system produces an output frequency equal to the input reference frequency times the division factor, N. The division factor or modulus can be changed to synthesize different frequencies. The technique used to vary the modulus differs with the type of frequency synthesizer architecture that is used.

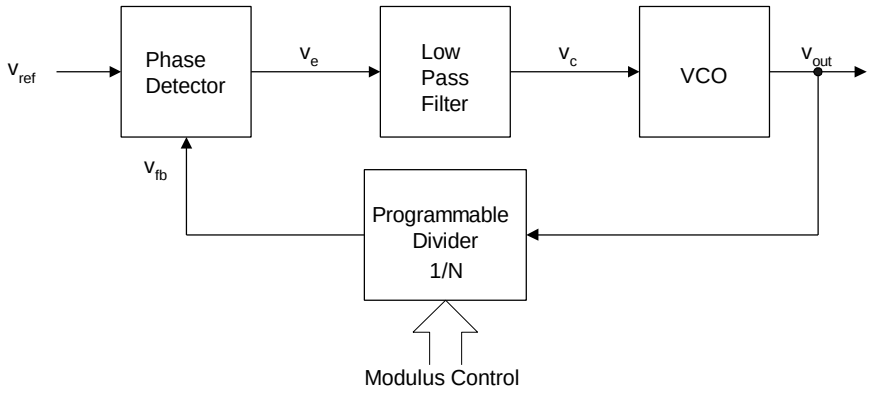

Figure 7 - Classic Digital PLL Frequency Synthesizer Block Diagram

Frequency Synthesizers with Prescalers

PLL frequency synthesizers with prescalers can be used to generate higher output frequencies. The prescaler is a frequency divider that is capable of operating at high VCO output frequencies. The prescaler divides the VCO output frequency by a factor of V. This value V is not tunable. These prescalers are typically designed using dynamic or current mode logic techniques[11,25-30]. Generally following the prescaler is another divider stage that is programmable. A block diagram of a PLL frequency synthesizer with a prescaler is shown in Figure 8.

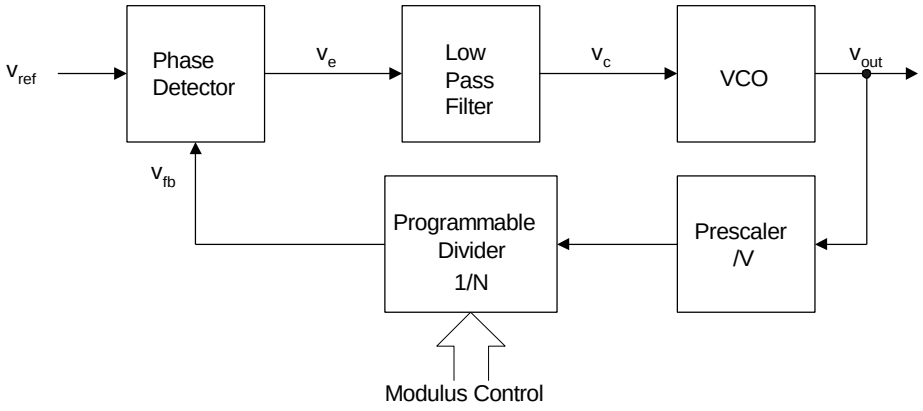

Figure 8 - PLL Frequency Synthesizer with Prescaler

This system produces an output frequency related to the input reference frequency by the following:

$$f_{out} = VNf_{ref} \qquad \textbf{(8)}$$

The addition of the prescaler allows for the synthesis of frequencies well into the GHz range with state-of-the-art submicron technologies.

Frequency Synthesizers with Dual-Modulus Prescalers

Prescaler frequency synthesizers only generate frequencies that are multiples of Vf_{ref}. A dual-modulus prescaler can be used in order to get higher resolution. A dual-modulus prescaler allows the prescaling factor to be changed between V and $V+1$. A block diagram of a PLL frequency synthesizer with a dual-modulus prescaler is shown in Figure 9[7,31].

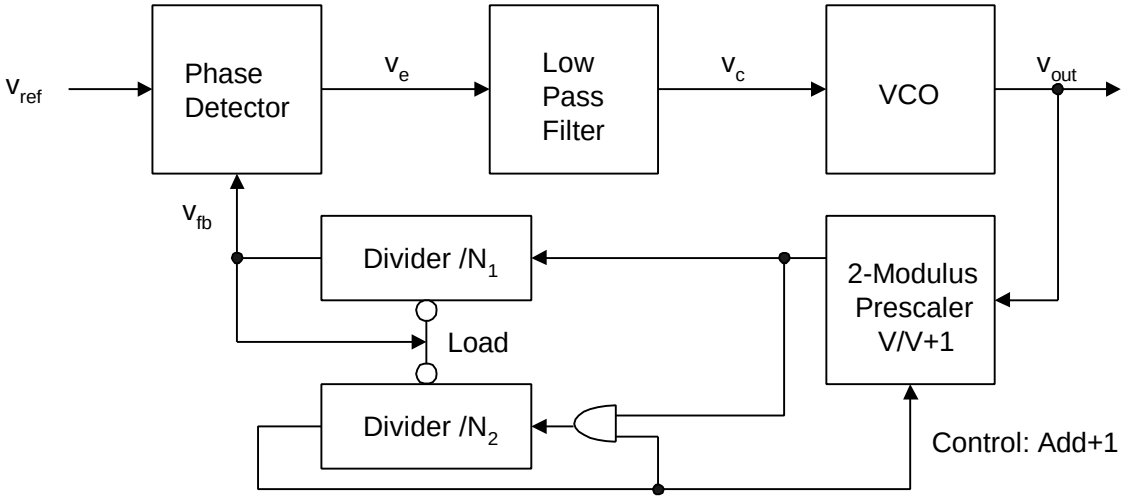

Figure 9 - PLL Frequency Synthesizer with Dual-Modulus Prescaler

The frequency synthesizer uses the $/N_1$ and the $/N_2$ down counters. The output of these counters is HIGH if the counter content has not reached zero. The counters are loaded with their preset values, N_1 and N_2, when the $/N_1$ counter counts to zero and its

output goes LOW. N_1 must be greater than or equal to N_2. N_2 must be less than V for correct operation. The $/N_2$ counter stops counting when it reaches zero and its output remains LOW until it is loaded. While the output of the $/N_2$ is not zero, the prescaler divides by $V+1$, and the VCO generates $N_2(V+1)$ pulses. The prescaler divides by V when the output of the $/N_2$ counter reaches zero and the VCO generates $(N_1 - N_2)\,V$ pulses until the $/N_1$ counter counts to zero. This causes the total number of pulses, N_{tot}, generated by the VCO during a full cycle of the reference signal to be equal to the following:

$$N_{tot} = N_2(V+1) + (N_1 - N_2)V = N_1V + N_2 \qquad \textbf{(9)}$$

This results in an output frequency, f_{out}, equal to the following:

$$f_{out} = (N_1V + N_2)\,f_{ref} \qquad \textbf{(10)}$$

Example: Assume a prescaler with $V = 10$

From (9), this results in the total number of pulses generated by the VCO during a full cycle to be equal to the following:

$$N_{tot} = 10N_1 + N_2 \qquad \textbf{(11)}$$

The valid ranges for the counters are the following:

$$0 \le N_2 \le 9 \;\&\; N_1 \ge 9 \qquad \textbf{(12)}$$

The smallest modulus is 90. This means the lowest possible output frequency is 90 times the reference frequency. Table 2 gives some of the possible modulus and frequencies that can be generated with different combinations of N_1 and N_2 using a reference frequency of 10kHz.

Table 2 - Dual-Modulus Prescaler FS Modulus Combinations with V=10

Modulus	N_1	N_2	Output Frequency (F_{ref} = 10kHz)
90	9	0	900kHz
91	9	1	910kHz
↓	↓	↓	↓
99	9	9	990kHz
100	10	0	1MHz
101	10	1	1.01MHz
↓	↓	↓	↓
108	10	8	1.08MHz
109	10	9	1.09MHz

If there is a need to increase the frequency, either N_1 or V has to be increased. Typically, V is increased because of the technology limitations of the $/N_1$ down counter. If V is increased to 100 (which implies N_2 is in the range from 0-99, and $N_1 \geq 99$) the minimum modulus would be 9900. This results in a minimum output frequency of 99MHz with a reference frequency of 10kHz. The dual-modulus FS allows for increasing the frequency resolution, but it also causes the minimum frequency to increase.

Frequency Synthesizers with Four-Modulus Prescalers

The four-modulus prescaler frequency synthesizer is able to extend the upper frequency range, while still allowing the lower frequencies to be synthesized. The four-modulus prescaler provides four different scaling values controlled by two signals. A block diagram of a four-modulus prescaler frequency synthesizer is shown in Figure 10[7,31].

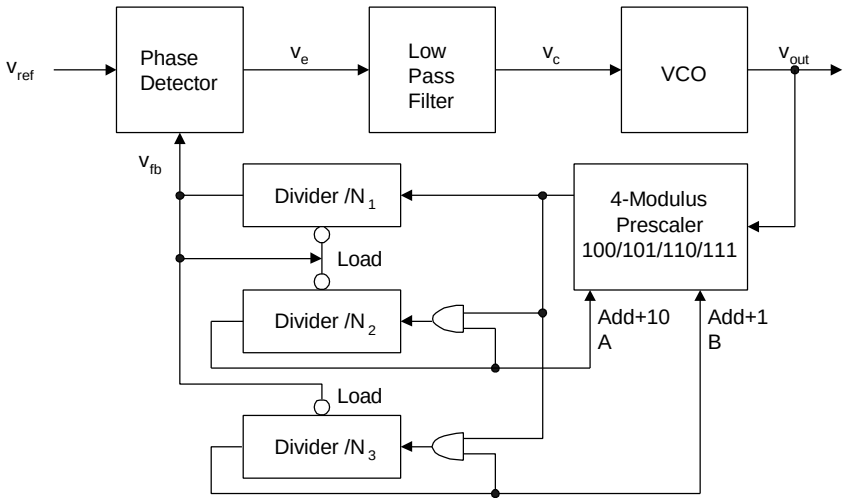

Figure 10 - PLL Frequency Synthesizer with Four-Modulus Prescaler

The four-modulus prescaler has the decimal scaling factors 100, 101, 110, and 111. These scaling factors are selected based on the control signals A & B according to the truth table shown in Table 3.

Table 3 - Four-Modulus Prescaler FS Scaling Factors Truth Table

A	B	Scaling Factor
0	0	100
0	1	101
1	0	110
1	1	111

The frequency synthesizer uses three down counters: $/N_1$, $/N_2$, and $/N_3$. The operation is similar to the dual-modulus prescaler frequency synthesizer. The total number of pulses, N_{tot}, generated by the VCO during a full cycle of the reference signal is equal to the following:

$$N_{tot} = 100 * N_1 + 10 * N_2 + N_3 \qquad \textbf{(13)}$$

This results in an output frequency, f_{out}, equal to the following:

$$f_{out} = (100N_1 + 10N_2 + N_3) f_{ref} \quad \textbf{(14)}$$

N_2 and N_3 must be in the range from 0-9 and N_1 must be greater than or equal to both N_2 and N_3 for correct operation. This results in a minimum division factor of 900. This means that with a 10kHz reference signal the lowest frequency that could be synthesized is 9MHz. A dual-modulus prescaler frequency synthesizer with the same resolution would result in the lowest synthesizable frequency of 99MHz.

Fractional N-Loop Frequency Synthesis

The previous frequency synthesis techniques all described ways to synthesize frequencies that are integer multiples of the reference signal. Fractional N-Loop Frequency Synthesizers allow the synthesis of frequencies that are fractional multiples of the reference signal. A block diagram of a fractional N-loop frequency synthesizer is shown in Figure 11[7, 31].

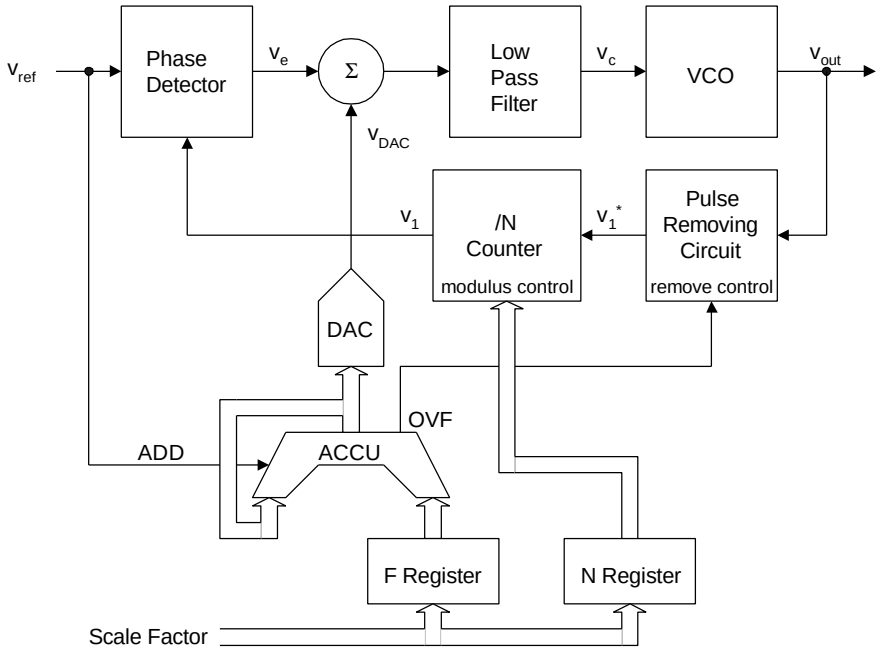

Figure 11 - Fractional N-Loop Frequency Synthesizer

The fractional n-loop frequency synthesizer works by varying the scaling factor between different values and using its average.

Example: It is desired that the VCO generates 67 pulses for every 10 full cycles of the reference signal. This corresponds to the following scale factor.

$$\text{Scale Factor} = 6.7 \qquad \textbf{(15)}$$

This resolution could not be realized by only using integer prescalers. Integer prescalers would only allow a modulus of 6 or 7, which would result in 60 or 70 pulses generated for 10 reference cycles. Fractional N synthesis allows dividing by 6 during three of the ten reference cycles and dividing by 7 during seven reference cycles to realize the scale factor of 6.7.

The integer of the scaling factor (6.7) is stored in the N register and the fraction is stored in the F register. The $/N$ counter divides by 6 during the first reference cycle. An error of 0.7 is added to the accumulator at the beginning of every cycle. The accumulator's contents overflow during the second cycle. The overflow signal is sent to a pulse removing circuit that removes one of the pulses generated by the VCO. The pulse removal effectively increases the division to 7 instead of 6. Seven overflow pulses will be generated during the duration of ten reference cycles. This corresponds to dividing by 6 during three of the ten cycles and dividing by 7 during seven cycles.

One problem associated with fractional n-loop frequency synthesizers is that spurs get generated at the VCO output due to the time-manipulation of the divider modulus. These spurs can be compensated using various techniques. DAC analog compensation, shown in Figure 11, can yield a typical 10 to 20 dB improvement in spurs[7,30,31]. This type of compensation is dependent on the divisor and the phase detector gain. The spurs can also be compensated digitally by using a DSP to generate compensating

waveforms[30]. This digital compensation has an advantage over the analog technique by being independent of the divisor.

Linear PLL Analysis

The PLL is a highly non-linear system[32]. However, it can be described with a linear model if the loop is in lock. The loop is in lock when the phase error signal produced by the phase detector settles on a constant value. This implies that the output signal has the same frequency as the input reference signal. A phase difference between the reference and output signal may exist depending on the type of PLL used. However, this phase difference remains constant while the loop is in lock. If the PLL is used as a frequency synthesizer, the output signal will have a frequency N times the reference frequency. The building blocks of Figure 12 are taken as basis for the mathematical model of a PLL in lock. A loop division factor, N, is included in this model. N can be considered equal to one for PLLs with no loop dividers. The following analysis shows step by step how to obtain the PLL transfer function:

$$H(s) = \frac{q_{out}}{q_{ref}} \qquad \textbf{(16)}$$

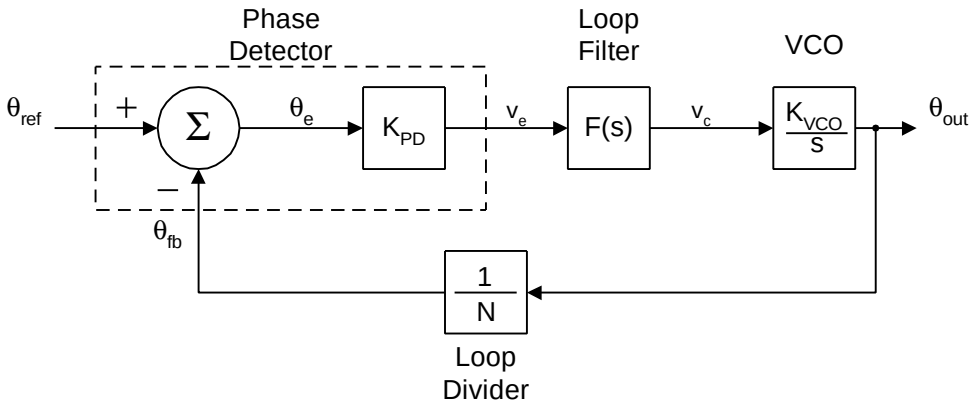

Figure 12 - Linear PLL Model

Note that the phase detector sums the input reference phase, q_{ref}, with the feedback phase, q_{fb}, and amplifies the difference with a gain K_{PD} to produce an error voltage, $V_e(s)$, equal to:

$$V_e(s) = K_{PD}\left[q_{ref}(s) - q_{out}(s)\right] = K_{PD} q_e(s) \quad \textbf{(17)}$$

This error voltage is filtered by the loop filter to produce the VCO control voltage that is equal to the following:

$$V_c(s) = V_e(s) F(s) \quad \textbf{(18)}$$

Recall from (7) that the VCO can be modeled as a phase integrator. This results in an output phase, q_{out}, equal to the following:

$$q_{out}(s) = \frac{V_c(s) K_{VCO}}{s} \quad \textbf{(19)}$$

The output phase is fed back and passes through a loop divider where it is divided by a factor of N to generate the feedback phase, q_{fb}, equal to the following:

$$q_{fb}(s) = \frac{q_{out}(s)}{N} \quad \textbf{(20)}$$

The transfer function of the PLL, $H(s)$, is equal to the following:

$$H(s) = \frac{q_{out}(s)}{q_{ref}(s)} = \frac{K_{PD} K_{VCO} F(s)}{s + \frac{K_{PD} K_{VCO} F(s)}{N}} \quad \textbf{(21)}$$

The phase error transfer function is equal to the following:

$$\frac{q_e(s)}{q_{ref}(s)} = \frac{s}{s + \frac{K_{PD} K_{VCO} F(s)}{N}} \quad \textbf{(22)}$$

The VCO control voltage transfer function is equal to the following:

$$\frac{V_c(s)}{q_{ref}(s)} = \frac{sK_{PD}F(s)}{s + \frac{K_{PD}K_{VCO}F(s)}{N}} \qquad \textbf{(23)}$$

The following observations are made from the transfer functions given in (21), (22), and (23). The PLL transfer function, given in (21), has a low-pass characteristic with a gain of N. This means that for slow (low frequency) variations in the reference phase, the loop will basically track the input signal and produce an output phase that is N times larger. Thus the output frequency is N times the input reference frequency. The phase error transfer function, given in (22), has a high-pass characteristic. This implies that for slow variations in the reference phase, the phase error will be small. However, fast (high frequency) variations in the reference phase will not be filtered and show up as a phase error. The VCO control voltage transfer function can be viewed as the filtered phase error output. It also has a high-pass characteristic. However, depending on the parameters of the loop filter, it can take on a more band-pass shape.

The dynamics of the PLL are dependent on the type of loop filter used. Without loss of generality consider the passive lag filter shown in Figure 13 which is a common filter used in PLL design[7].

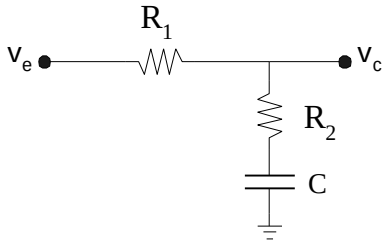

Figure 13 - Passive Lag Filter

This filter is very simple to build and proves to be adequate in most applications. If filter gain is necessary for increased tracking accuracy, active filters with a high gain opamp may be used. The transfer function of the passive lag filter is the following:

$$F(s)=\frac{V_c(s)}{V_e(s)}=\frac{sCR_2+1}{sC(R_1+R_2)+1} \qquad \textbf{(24)}$$

Substituting (24) into (21) we obtain the PLL's transfer function.

$$H(s)=\frac{K_{PD}K_{VCO}\left(\frac{sCR_2+1}{C(R_1+R_2)}\right)}{s^2+s\frac{K_{PD}K_{VCO}CR_2+N}{NC(R_1+R_2)}+\frac{K_{PD}K_{VCO}}{NC(R_1+R_2)}} \qquad \textbf{(25)}$$

It can be observed that using a first order filter in the PLL results in a second order system. In fact, the order of a PLL is equal to the loop filter order plus one.

The second order PLL system can be described in a standard control system format as follows:

$$H(s)=N\frac{s\left(2\zeta w_n-\frac{Nw_n^2}{K_{PD}K_{VCO}}\right)+w_n^2}{s^2+2\zeta w_n s+w_n^2} \qquad \textbf{(26)}$$

where

$$\zeta=\frac{1}{2}\sqrt{\frac{K_{PD}K_{VCO}}{NC(R_1+R_2)}}\left(CR_2+\frac{N}{K_{PD}K_{VCO}}\right) \qquad \textbf{(27)}$$

and

$$w_n=\sqrt{\frac{K_{PD}K_{VCO}}{NC(R_1+R_2)}} \qquad \textbf{(28)}$$

The parameter z is the damping factor and w_n is the natural frequency. An s-plane plot shown in Figure 14 is used to explain these parameters [33].

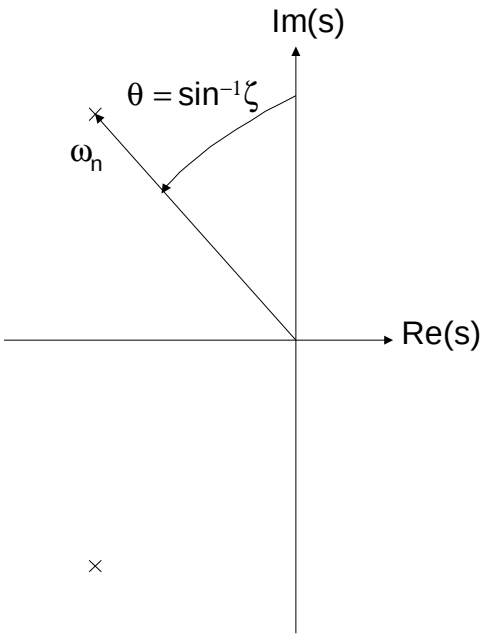

Figure 14 - Pair of Complex Poles S-Plane Plot

One can observe that the poles are located at a distance w_n from the origin and at an angle $q = \sin^{-1} z$. The damping factor, z , is a measure of stability. If z is equal to zero, then the poles of the system lie on the imaginary axis at a distance w_n from the origin. For this case the impulse response of the system results in a steady oscillation at a frequency w_n. On the other hand, as z is increased, the poles move to the left-hand plane and the system becomes stable. For this particular situation the impulse response of the system becomes a damped oscillation at a frequency w_n. Using (26), a plot of the second order PLL frequency response for different damping factors is shown in Figure 15.

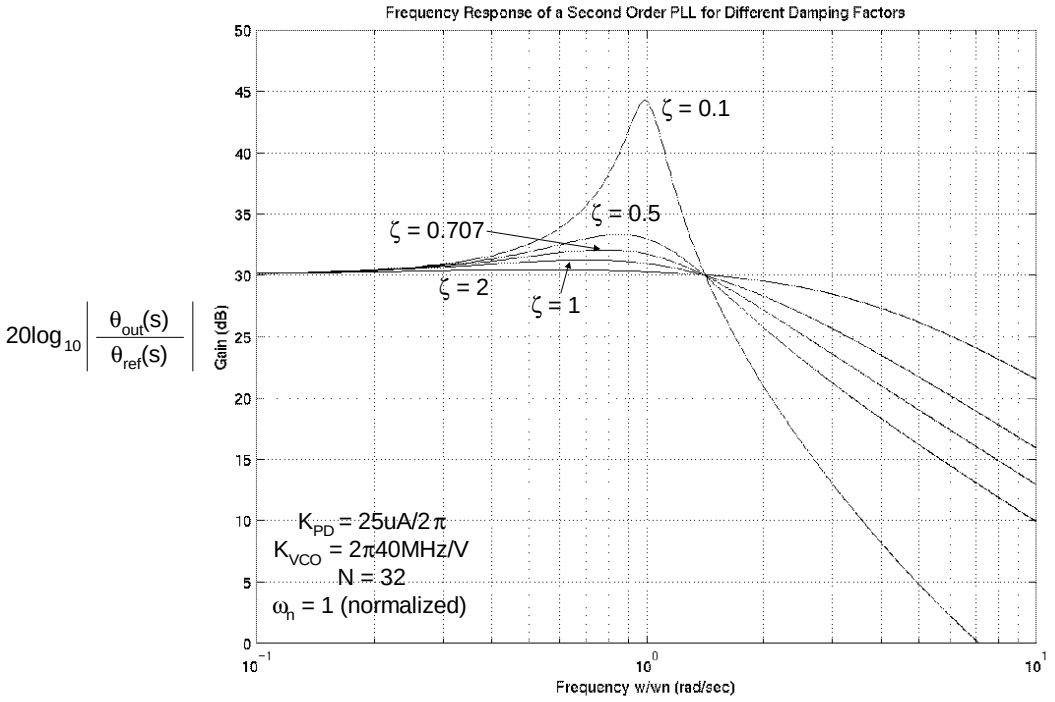

Figure 15 - Second Order PLL Frequency Response for Different Damping Factors

The PLL frequency response shows the expected second-order low-pass characteristic. The Q value of a PLL is inversely proportional to the damping factor, z . High Q values display a frequency response with a sharp peak at w_n. This results in an oscillatory transient response. If the damping factor is high, the Q value of the system is low and the frequency response is flat across a wide bandwidth. This results in a slow, sluggish transient response. Generally, an optimally flat frequency transfer function is desired[7]. This occurs when $z = 1/\sqrt{2} \approx 0.707$, which corresponds to a second-order Butterworth low-pass filter. The values of z and w_n also has an effect on the bandwidth of the PLL. The 3-dB bandwidth is equal to the following[34]:

$$w_{3dB} = w_n\left(a + \sqrt{a^2 + 1}\right)^{1/2} \qquad \textbf{(29)}$$

where a is equal to the following:

$$a = 2\zeta^2 + 1 - \frac{\omega_n N}{K_{PD} K_{VCO}} \left(4\zeta - \frac{\omega_n N}{K_{PD} K_{VCO}} \right) \quad \textbf{(30)}$$

The values of ζ and ω_n have a noticeable effect on the transient response of the PLL. The effect of ζ and ω_n can be seen by applying a phase step to the reference signal of a locked PLL as shown in Figure 16.

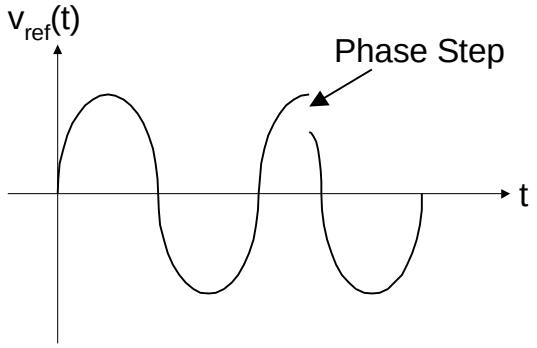

Figure 16 - Phase Step Applied to the Input Reference Signal

The following time domain function describes the input reference signal when a phase step is applied at $t = 0$.

$$v_{ref}(t) = \sin\left(\omega t + \theta_{step}(t)\right) \quad \textbf{(31)}$$

A phase step applied to a locked PLL can be modeled as the following:

$$\theta_{ref}(s) = \frac{\Delta\theta}{s} \quad \textbf{(32)}$$

This results in the following response for the phase error.

$$q_e(s) = \Delta q \frac{s + \dfrac{w_n^2 N}{K_{PD} K_{VCO}}}{s^2 + 2z w_n s + w_n^2} \qquad \textbf{(33)}$$

The VCO control voltage has the following response.

$$V_c(s) = \frac{\Delta q N}{K_{VCO}} \frac{s\left(2z w_n - \dfrac{N w_n^2}{K_{PD} K_{VCO}}\right) + w_n^2}{s^2 + 2z w_n s + w_n^2} \qquad \textbf{(34)}$$

When a phase step is applied to a locked PLL a phase error will result. However, the PLL will remain in the lock range and the loop dynamics will force this phase error to zero. The unit phase step transient response of the phase error for different damping factors is shown in Figure 17, while the VCO control voltage response is shown in Figure 18.

The following observations can be made from the transient response of the phase error and VCO control voltage to a normalized phase step input. Both waveforms respond with a dampened oscillation at a frequency of $f = 1/(2p)$. This corresponds to a normalized natural frequency $w_n = 1$. It can be observed for a low damping factor the oscillation takes a while to die out. The phase error signal initially has a value of 1 because a unit phase step is applied to the input. This phase error eventually dies down to zero after the loop has acquired lock. The VCO control voltage initially has a small value. This small value allows the output signal to catch up with the input reference phase step. The reason why the value is so small is that the VCO gain is very high. The VCO control voltage eventually returns to zero because the reference frequency has not changed.

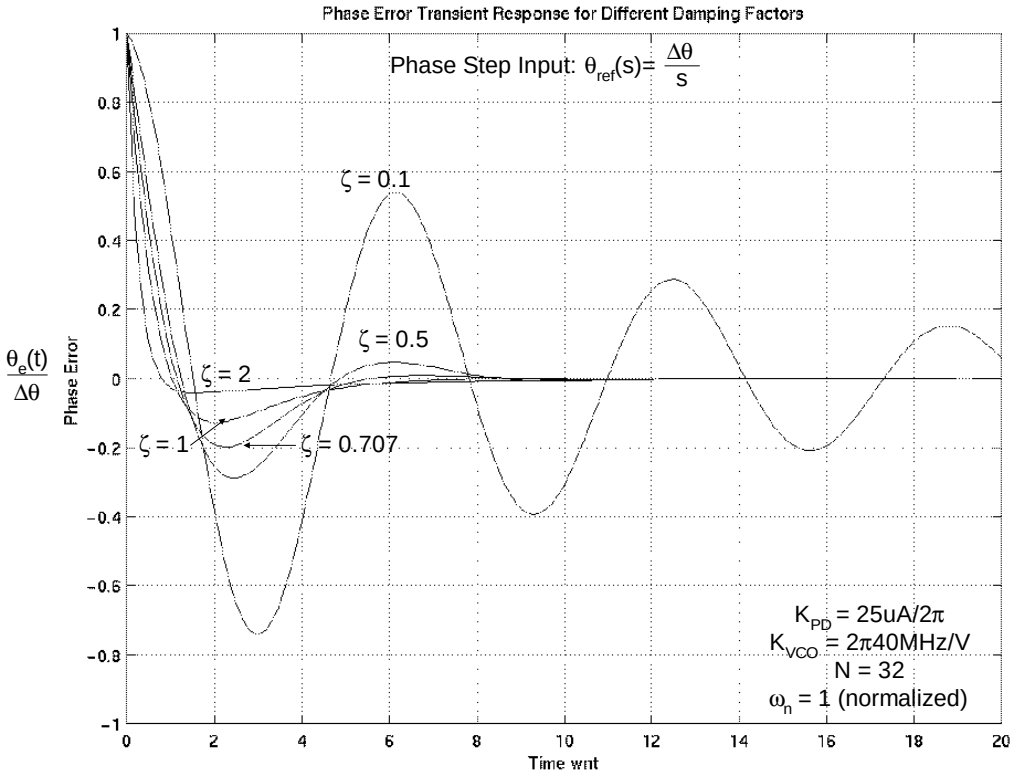

Figure 17 - Phase Error Transient Response - Unit Phase Step Input

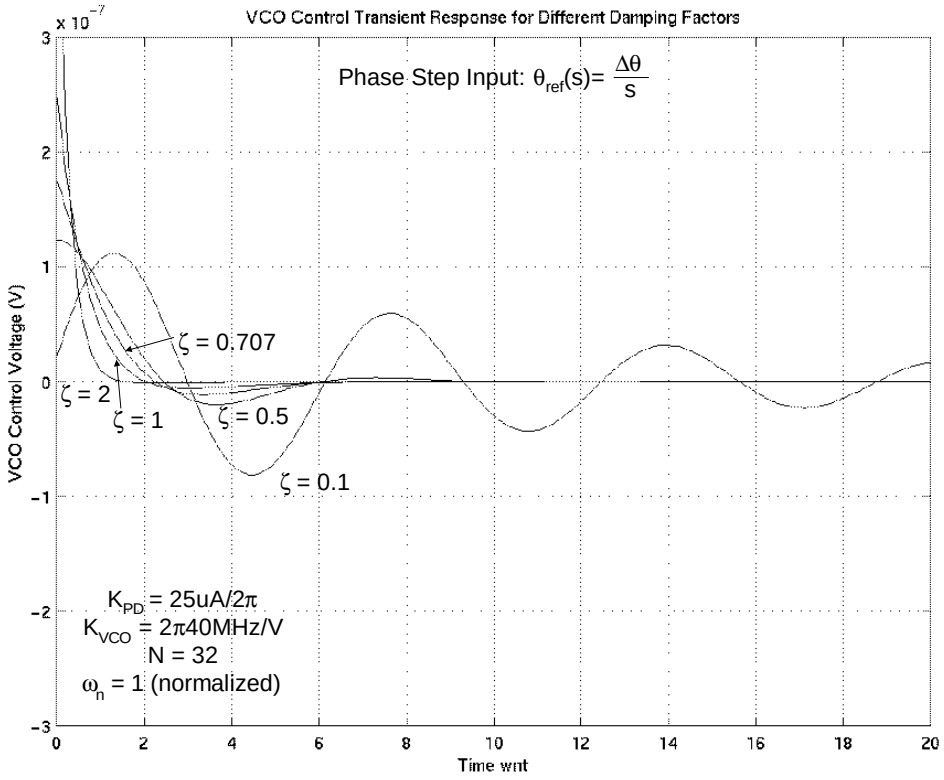

Figure 18 - VCO Control Transient Response - Unit Phase Step Input

The effect of z and w_n can also be seen by applying a frequency step to the reference signal of a locked PLL as shown in Figure 19.

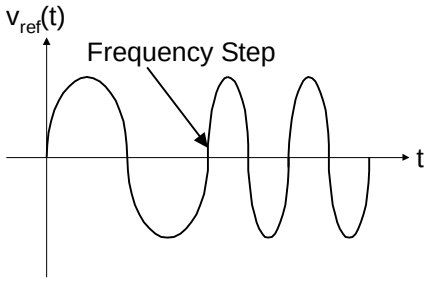

Figure 19 - Frequency Step Applied to the Input Reference Frequency

The following time domain function describes the input reference signal when a frequency step is applied at $t = 0$.

$$v_{ref}(t) = \sin\left(\left(w \quad + \Delta w_{step}(t)\right)\ t\right) \qquad \textbf{(35)}$$

A frequency step input is equivalent to a phase ramp input. Therefore the input to a locked PLL can be modeled as the following:

$$q_{ref}(s) = \frac{\Delta w}{s^2} \qquad \textbf{(36)}$$

This results in the following response for the phase error.

$$q_e(s) = \Delta w \frac{s + \dfrac{w_n^{\,2} N}{K_{PD} K_{VCO}}}{s\left(s^2 + 2z\, w_n s + w_n^{\,2}\right)} \qquad \textbf{(37)}$$

The VCO control voltage has the following response.

$$V_c(s) = \frac{\Delta w N}{K_{VCO}} \frac{s\left(2z\, w_n - \dfrac{N w_n^{\,2}}{K_{PD} K_{VCO}}\right) + w_n^{\,2}}{s\left(s^2 + 2z\, w_n s + w_n^{\,2}\right)} \qquad \textbf{(38)}$$

The frequency step transient response of the phase error for different damping factors is shown in Figure 20, while the VCO control voltage response is shown in Figure 21.

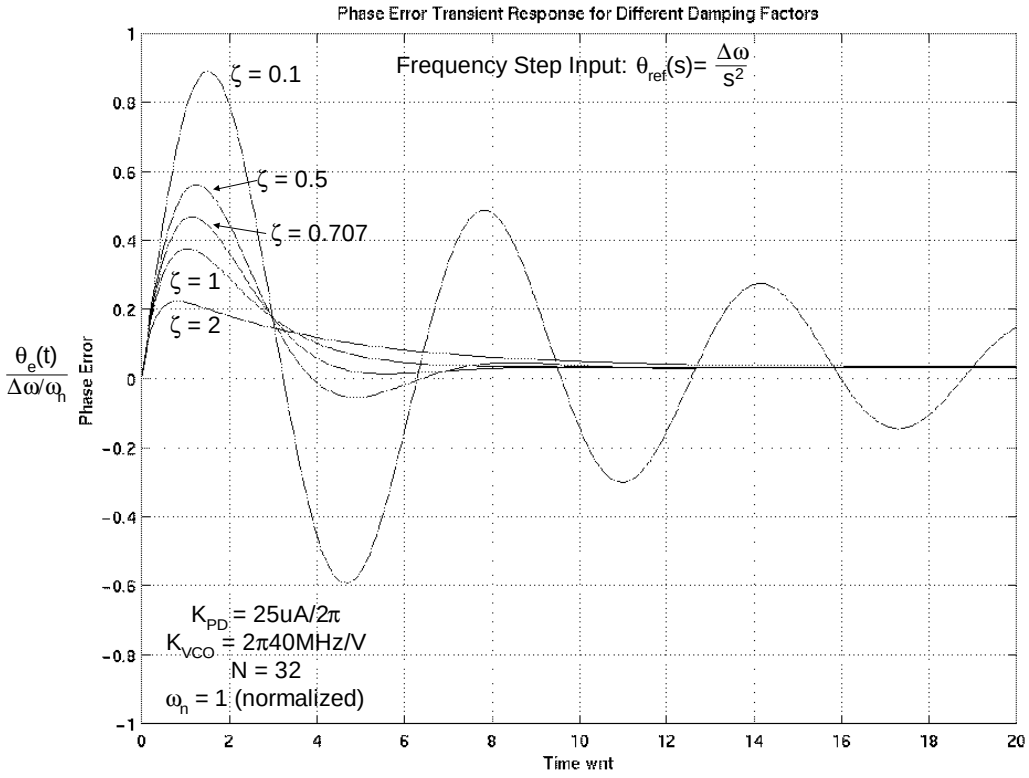

Figure 20 - Phase Error Transient Response - Frequency Step Input

The following observations can be made from the transient response of the phase error and VCO control voltage to a normalized frequency step input. Both waveforms respond with a dampened oscillation at a frequency of $f = 1/(2p)$. This corresponds to a normalized natural frequency $w_n = 1$. The phase error is initially zero because the loop is locked on the VCO center frequency. As the input reference frequency experiences a frequency step, the phase error responds with the dampened oscillation. The phase error eventually dies down to the following value:

$$\lim_{t\to\infty} q_e(t) = \frac{N\Delta w}{K_{PD}K_{VCO}} \qquad \textbf{(39)}$$

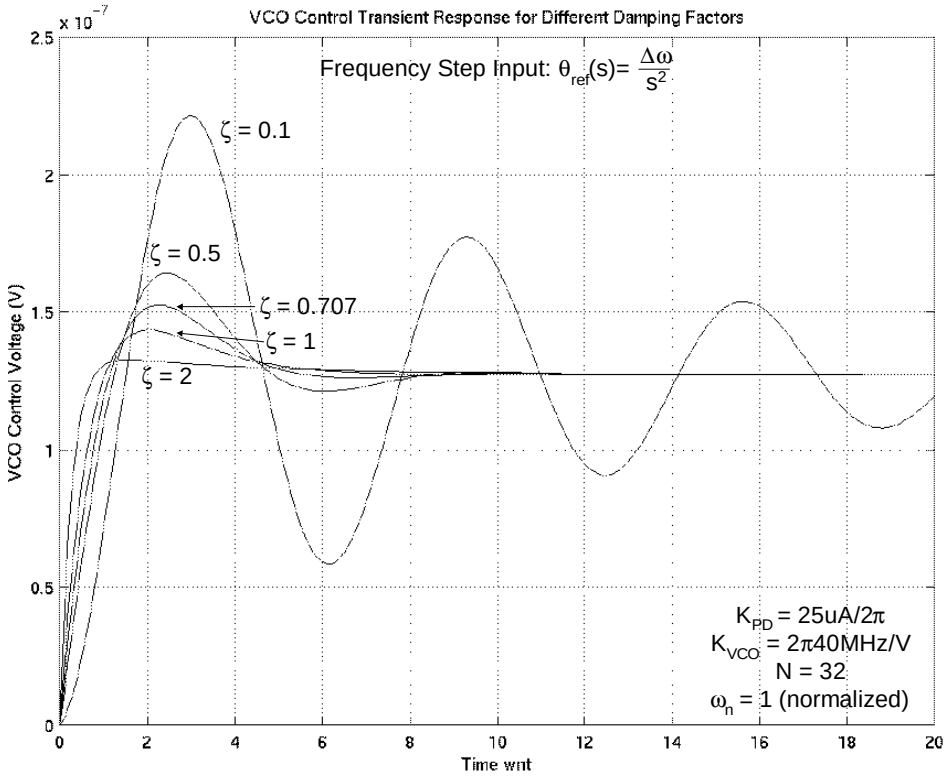

Figure 21 - VCO Control Transient Response - Frequency Step Input

It can be observed that the low damping factor systems are very oscillatory. The high damping factor systems are more stable. However, their settling time to the final value can be long. The optimal damping factor is found to be $\zeta = 1/\sqrt{2} \approx 0.707$. The VCO control voltage is initially zero because the loop is locked on the center frequency of the VCO. After a frequency step is applied to the input, the VCO control voltage rises to increase the output frequency to allow the output signal to synchronize with the input reference signal. The VCO control signal has a step response with a dampened oscillation. The VCO control voltage eventually settles on the following value:

$$\lim_{t\to\infty} V_c(t) = \frac{N\Delta w}{K_{VCO}} \qquad \textbf{(40)}$$

In summary, the dynamic response of the second-order PLL is dependent on the natural frequency and the damping factor. Generally, the damping factor is set equal to $1/\sqrt{2}$ as a compromise between stability and speed. The natural frequency plays an important role in determining the bandwidth of the PLL. How the bandwidth of the PLL is designed depends on the desired noise performance of the PLL and the dominant sources of noise in the PLL.

PLL Noise Analysis

The job of any frequency synthesizer is to generate a spectrally pure output signal. An ideal periodic output signal in the frequency domain has only an impulse at the fundamental frequency and perhaps some other impulse energy at DC and harmonics. In the actual oscillator implementation, the zero crossings of the periodic wave vary with time as shown in Figure 22. This varying of the zero crossings is known as time-domain jitter.

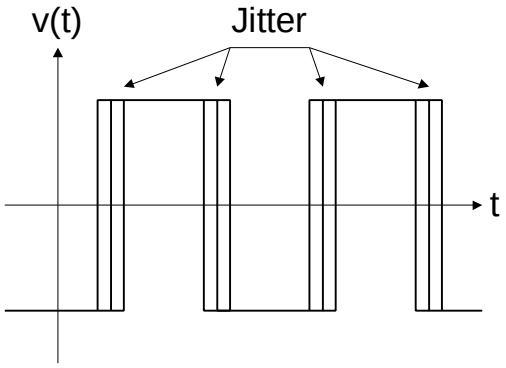

Figure 22 - Periodic Signal with Jitter

A signal with jitter no longer has a nice impulse spectrum. Now the frequency spectrum consists of impulses with skirts of energy as shown in Figure 23. These skirts are known as phase noise.

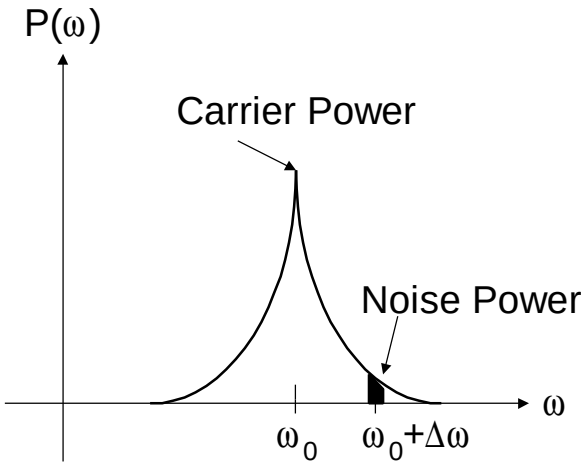

Figure 23 - Frequency Spectrum of a Signal with Phase Noise

Phase noise is generally measured in units of dBc/Hz at a certain offset from the desired or carrier signal. The formal definition of phase noise is the ratio of the sideband noise power in a 1Hz bandwidth at a given frequency offset Δw from the carrier over the carrier power as shown in the following.

$$L\{\Delta w\} = \frac{P_{sideband}\left(w_0 + \Delta w \ , 1\text{Hz Bandwidth}\right)}{P_{carrier}} \qquad \textbf{(41)}$$

The PLL can be designed in such a way as to minimize the phase noise of the output signal. Generally, the dominant sources of phase noise are from a noisy reference signal or from a noisy oscillator. Also other loop non-idealities, such as phase-detector dead zone and power supply fluctuations can contribute to phase noise. The way the PLL is designed depends on what is the dominant source of noise in the loop.

Input Phase Noise

An input reference signal with phase noise can be modeled in the PLL as shown in Figure 24[22]. Without loss of generality, the loop filter is assumed to be the passive lag filter discussed in the previous section.

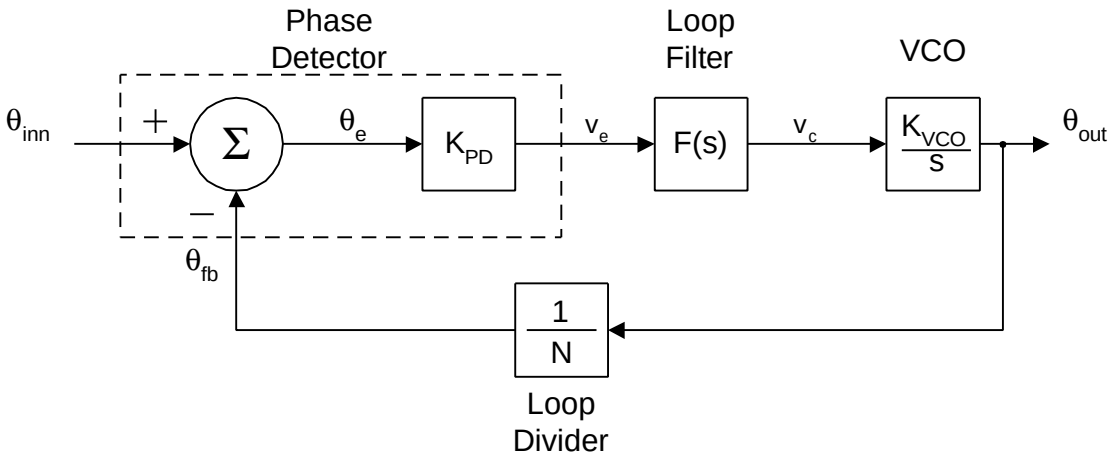

Figure 24 - PLL Input Phase Noise Model

The input noise, q_{inn}, is treated as an input signal and the same PLL transfer function from (26) is derived for the input noise transfer function. The input phase noise transfer function is plotted in Figure 25.

$$\frac{q_{out}(s)}{q_{inn}(s)} = N\frac{s\left(2\zeta w_n - \frac{Nw_n^2}{K_{PD}K_{VCO}}\right)+w_n^2}{s^2+2\zeta w_n s+w_n^2} \qquad \textbf{(42)}$$

The input phase noise is shaped by the low-pass characteristic of the second-order PLL. In order to reduce the phase noise in the output signal due to the input phase noise it is desirable to make the PLL bandwidth as narrow as possible. Notice that the input noise is amplified by a factor of N. If input noise is a concern, the lowest possible value of N should be used. Usually in frequency synthesizer design the input phase noise is not a concern because the reference signal generally comes from a low phase noise crystal oscillator.

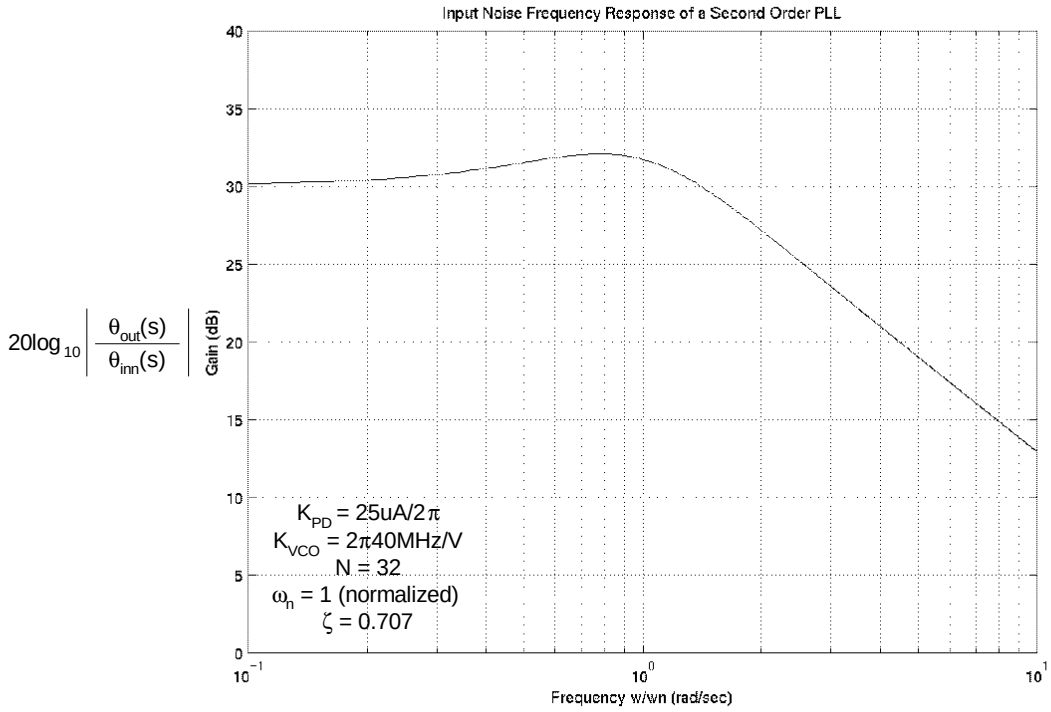

Figure 25 - Input Phase Noise Frequency Response

VCO Phase Noise

The VCO phase noise can be modeled in the PLL as shown in Figure 26[22]. Without loss of generality, the loop filter is assumed to be the passive lag filter discussed in the previous section.

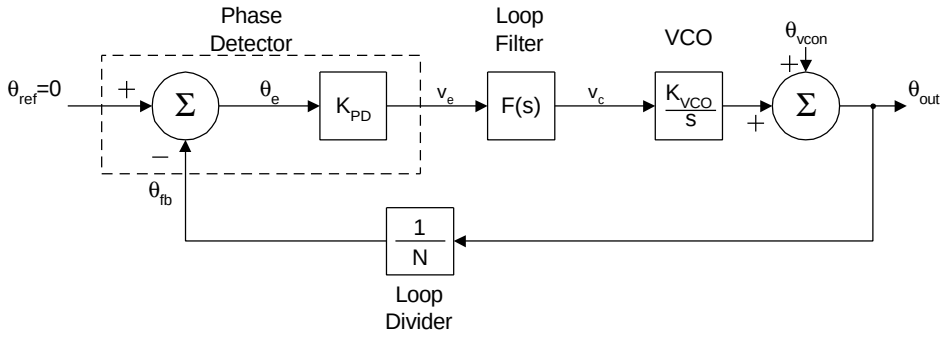

Figure 26 - PLL VCO Phase Noise Model

The VCO phase noise, q_{vcon}, is treated as an input signal and the following transfer function is derived. The VCO phase noise transfer function is plotted in Figure 27.

$$\frac{q_{out}(s)}{q_{vcon}(s)} = \frac{s^2 + \frac{sw_n^2 N}{K_{PD}K_{VCO}}}{s^2 + 2z\,w_n s + w_n^2} \qquad \textbf{(43)}$$

The VCO phase noise is shaped by a high-pass characteristic by the second-order PLL. In order to reduce the phase noise in the output signal due to the VCO phase noise it is desirable to make the PLL bandwidth as wide as possible. Here a tradeoff regarding loop bandwidth position and its effect on input phase noise contribution and VCO phase noise contribution is observed. The optimum loop bandwidth depends on the application. It is optimal to have a narrow loop bandwidth for input noise performance. Narrow band loops aid in the cases where the PLL is operating with a noisy reference signal. It is optimal to have a wide loop bandwidth for VCO noise performance. Usually the dominant source of noise is the VCO in fully integrated frequency synthesizer design[35]. The VCO phase noise is caused by such things as the upconverted $1/f$ noise from the transistors used to design the VCO, noise in the control path, and cycle-to-cycle fluctuations in the power supply[36,37]. With the VCO contributing significant phase noise it is optimal to make the loop bandwidth as wide as possible.

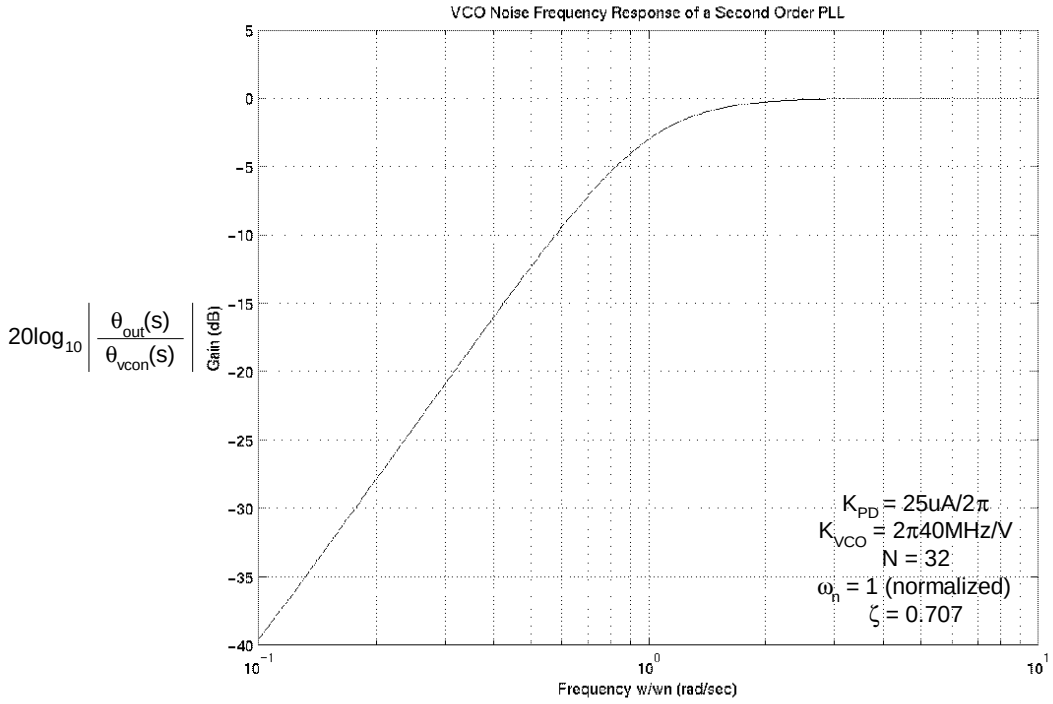

Figure 27 - VCO Phase Noise Frequency Response

Phase Detector Dead Zone

Another source of noise in PLLs is the phase detector dead zone. The dead zone is a region over which the phase detector gain, K_{PD}, becomes very small. The dead zone is illustrated in Figure 28.

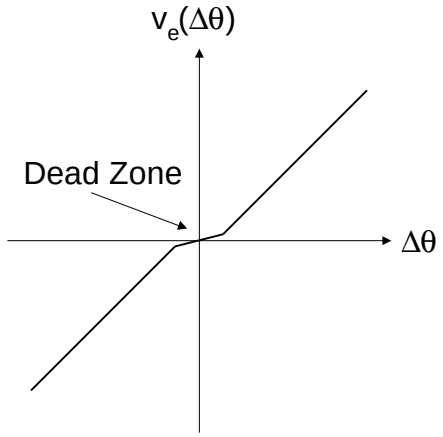

Figure 28 - Phase Detector Dead Zone

This region occurs when the loop is essentially locked. However, the reference and feedback signal still should produce a phase error. Because little phase error is generated for variations in the reference or feedback signal a peak-to-peak jitter approximately equal to the width of the dead zone arises in the output signal[3]. Proper phase detector design techniques minimize this dead zone.

Charge Pump PLLs

The charge pump PLL is popular for integrated circuit applications for the following reasons. The phase/frequency detector used in the charge pump PLL allows the PLL to have a pull-in range that is only limited by the VCO's tuning range[7]. The static phase error is zero between the input reference signal and the feedback signal even if the reference signal is not equal to the center frequency of the VCO[3,38]. The charge pump PLL also displays increased immunity to power supply variations[39].

The charge pump PLL is a digital PLL that uses a charge pump as the output of the phase/frequency detector as shown in Figure 29. The phase/frequency detector compares the input reference signal and the feedback signal to produce two control signals *UP* and *DOWN* . These control signals control how much error current flows

into the loop filter. The loop filter consists of a minimum of one capacitor C_1 in series with a resistor R. The charge pump current charges and discharges the loop filter to produce the VCO control voltage. The VCO signal is then divided in frequency and fed back to the phase/frequency detector.

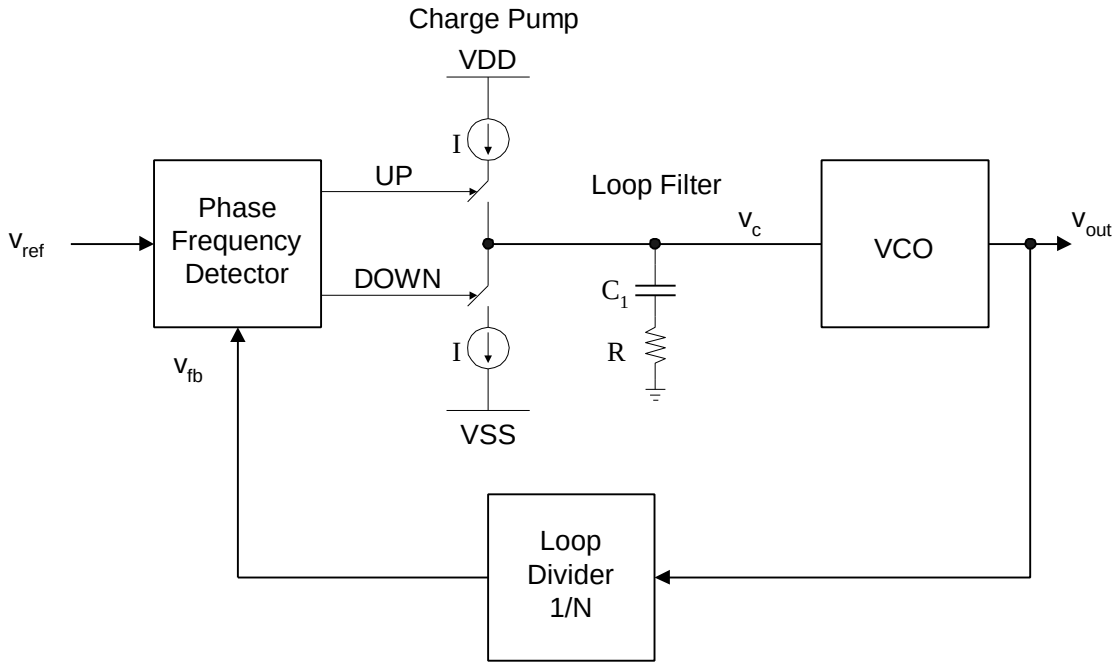

Figure 29 - Charge Pump PLL

The main difference between the digital charge pump PLL and the classic analog PLL is the phase detection circuitry. A multiplier is used as a phase detector in the analog PLL. This produces a non-zero static phase error if the input reference frequency is not equal to the center frequency of the VCO. The charge pump PLL uses a digital phase/frequency detector (PFD) that switches a charge pump's current sources to charge or discharge the loop filter. The type of PFD used allows for a zero static phase error even when the input reference frequency is not equal to the center frequency of the VCO.

Charge Pump PLL Linear Analysis

The switching interaction between the phase/frequency detector and the charge pump make the charge pump PLL a discrete time system. A plot of this interaction for a frequency step input is shown in Figure 30. This is a plot of the VCO control voltage when the charge pump PLL has a frequency step input.

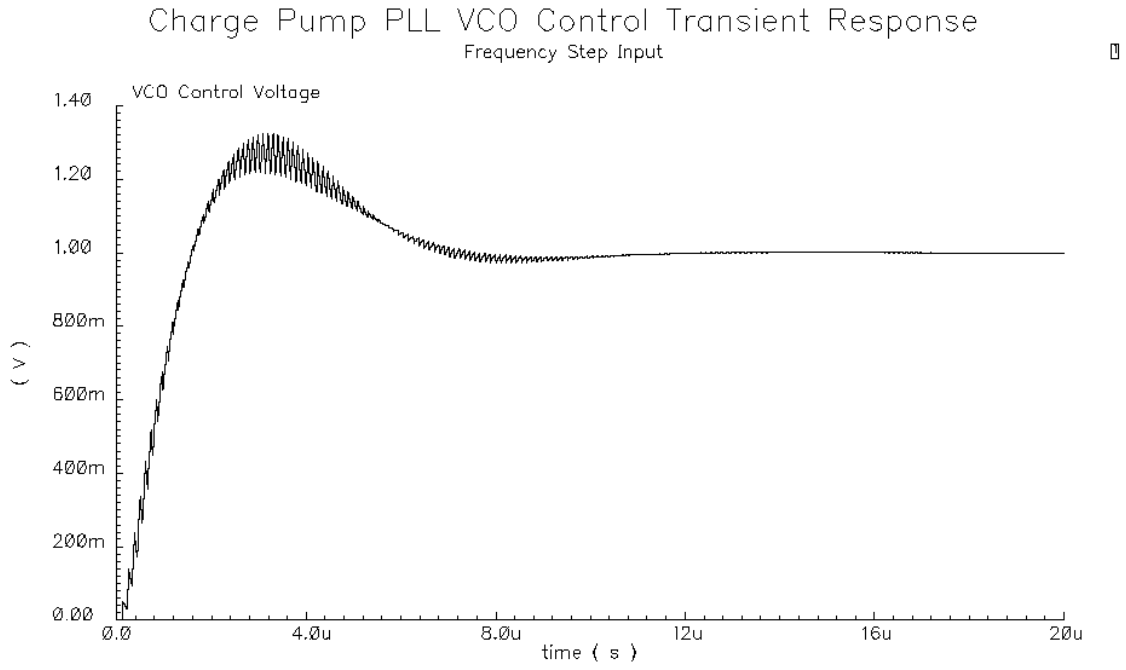

Figure 30 - Charge Pump PLL VCO Control Voltage Transient Response

Notice the ripple on the VCO control voltage that is not evident in the earlier linear PLL analysis in Figure 21. This ripple is due to the charge pump charging and discharging the loop filter. However, even though this is a discrete time system, the response is very similar to the linear PLL. In fact, a linear analysis can be assumed for the charge pump PLL if the loop bandwidth is much less than the input reference frequency[40].

Using the linear PLL model, the same PLL transfer function found in (21) is derived for the charge pump PLL transfer function $H_{CP}(s)$.

$$H_{CP}(s) = \frac{q_{out}(s)}{q_{ref}(s)} = \frac{K_{PD}K_{VCO}F(s)}{s + \frac{K_{PD}K_{VCO}F(s)}{N}} \quad \textbf{(44)}$$

Stability Analysis

There are certain conditions that must be satisfied for the charge pump PLL to be a stable system. Care must be taken in choosing the type of loop filter that is used in the PLL and also in designing the bandwidth of the loop.

The loop filter converts the charge pump current into a voltage for the VCO. One may be tempted to only use a capacitor as the loop filter. However, if only a capacitor is used as the loop filter, the following transfer function is obtained.

$$H_{CP}(s) = \frac{K_{PD}K_{VCO}/C_1}{s^2 + \frac{K_{PD}K_{VCO}}{NC_1}} \quad \textbf{(45)}$$

It can be observed that this is an unstable system because there are two poles on the imaginary axis. This means the damping factor is zero. Any excitation input to the system will result in a steady "phase oscillation" with a frequency equal to the natural frequency of the system.

In order for the loop to be stable a zero must be added to the loop filter in order to move the loop's poles from the imaginary axis into the left plane. This is typically done by adding a series resistor to the loop filter as shown in Figure 29. With the resistor in the loop filter the charge pump PLL transfer function becomes the following:

$$H_{CP}(s) = \frac{K_{PD}K_{VCO}R\left(s + \frac{1}{RC_1}\right)}{s^2 + s\frac{K_{PD}K_{VCO}R}{N} + \frac{K_{PD}K_{VCO}}{NC_1}} \quad \textbf{(46)}$$

Here there is an s term in the denominator. This means that there is a non-zero damping factor. Now, any excitation to the system will result in a dampened oscillation with a natural frequency equal to the following.

$$w_n = \sqrt{\frac{K_{PD} K_{VCO}}{NC_1}} \qquad \textbf{(47)}$$

The damping factor of the system is equal to the following:

$$\zeta = \frac{w_n RC_1}{2} \qquad \textbf{(48)}$$

The switching interaction between the charge pump and the loop filter causes a great deal of ripple on the VCO control voltage with the series RC loop filter. This ripple may be suppressed by adding a small capacitor, C_2, in parallel with the loop filter as shown in Figure 31.

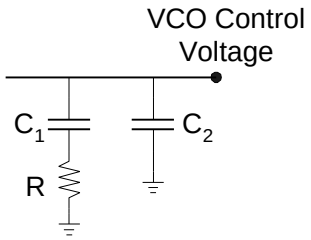

Figure 31 - Addition of C_2 in Loop Filter to Suppress Ripple

The addition of this capacitor adds another pole to the PLL transfer function and makes it a third-order system. However, if the capacitor is small enough the system can be analyzed as a second order system. If C_2 is made smaller then $0.1C_1$ it may be neglected in the loop analysis because it is at a frequency greater then a decade from the zero of the filter[39].

The previous analysis assumes that the charge pump PLL is a linear system, when in fact it is a discrete time system. The linear approximation holds only when the input reference frequency is significantly higher then the loop bandwidth. Generally this means an input reference frequency about 10 times greater then the loop bandwidth. Because the loop bandwidth is closely related to the natural frequency, a stability limit can be derived that is a function of w_n. A formal stability limit is given in the following inequality[3,40].

$$w_n^2 < \frac{w_{ref}^2}{p\left(RCw_{ref} + p\right)} \qquad \textbf{(49)}$$

Charge Pump PLL Building Blocks

The building blocks that make up the charge pump PLL consist of the phase frequency detector, charge pump, loop filter, VCO, and the loop divider. The following explains each block and discusses its role in the loop's performance.

Phase/Frequency Detector

The phase detector is a digital phase/frequency detector (PFD) with a charge pump output stage. The digital phase/frequency detector consists of two D Flip-Flops and an AND gate. A schematic of the phase/frequency detector is shown in Figure 32.

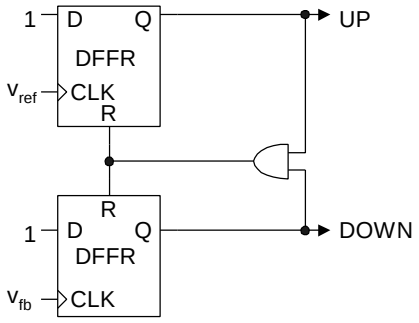

Figure 32 - Phase/Frequency Detector

The phase/frequency detector produces two output signals, *UP* and *DOWN*, that are dependent on the phase and frequency relationship of the two inputs, v_{ref} and v_{fb}. The *UP* and *DOWN* outputs control the charge pump which acts as the phase frequency detector's output stage. The charge pump outputs a current into the loop filter to generate the control signal of the VCO.

The *UP* output signal of the PFD goes high on the rising edge of v_{ref}. The *DOWN* output signal goes high on the rising edge of v_{fb}. The *UP* and *DOWN* signals remain high until they are reset by the AND combination of *UP* and *DOWN*. In other words, the reset signal is produced when both v_{ref} and v_{fb} clock inputs are high. Both *Q* outputs will be essentially low when both signals are in phase and of the same frequency. An example is shown in Figure 33.

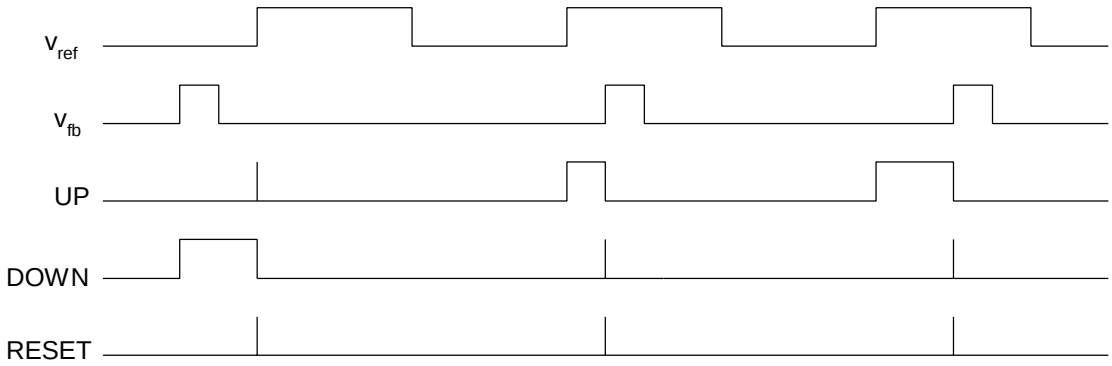

Figure 33 - Phase/Frequency Detector Signal Diagram

In this example, the rising edge of v_{fb} occurs first. This causes the *DOWN* signal to go high. The *DOWN* signal then remains high until reset. The rising edge of v_{ref} occurs later. This causes the *UP* signal to go high. The *UP* signal only remains high for an instance. The reason for this is that now both *UP* and *DOWN* are high. The AND output of these two signals causes the reset signal to go high. This causes both *UP* and

DOWN to return low. After some time the rising edge of v_{ref} occurs. This causes the *UP* signal to go high and remain high until reset. The rising edge of v_{fb} occurs later. This causes the *DOWN* signal to go high. Now both outputs are high and the PFD outputs are reset low. This is repeated again in this example.

The *UP* and *DOWN* output voltages of the phase/frequency detector depend on both the relative frequency difference and the phase error if the two input frequencies are the same. The phase error is the phase difference between the v_{ref} and v_{fb} signals given in the following:

$$q_e = q_{ref} - q_{fb} \text{ (radians)} \qquad \textbf{(50)}$$

The phase/frequency detector's outputs go high on the leading edge of their clock inputs and remain high until they are reset. The time the outputs are high, t_{high}, is related to the phase error, q_e, by the following[40]:

$$t_{high} = \frac{|q_e|}{w_{ref}} \qquad \textbf{(51)}$$

An advantage of the digital phase/frequency detector is that it uses only the rising edges of the input reference signal and the VCO feedback signal to generate the output signals. This means that the width of the input reference signal and the VCO feedback signal are irrelevant. A 50% duty cycle signal is not necessary for this phase frequency detector. Other types of phase detectors, like the XOR gate phase detector, require 50% duty cycle signals[7].

Another advantage of the PFD over the XOR phase detector is that the PFD will not allow the loop to lock on harmonics. This allows the hold range of a PLL using the PFD to be very large. The hold range is only limited by the VCO tuning range.

One potential problem that this phase detector may have is a dead zone. The dead zone occurs when the rising edges of the input reference and VCO feedback signals are almost aligned. If the delay through the reset path is shorter than the delay to the charge pump that the PFD is driving then the charge pump will not get switched even though there is a phase error present. This will result in jitter in the output signal as discussed earlier[3]. The PFD must be designed in such a way as to ensure that the delay through the reset path is longer then the delay to the charge pump.

Charge Pump

Figure 34 shows the charge pump output stage of the phase/frequency detector. It supplies current to the loop filter to produce the VCO control voltage.

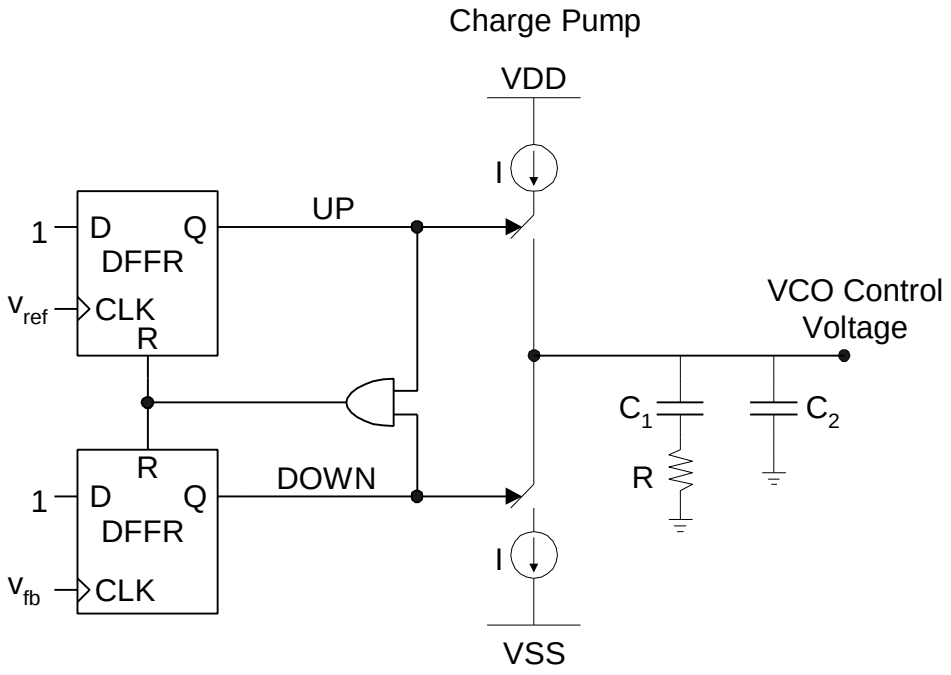

Figure 34 - PFD Charge Pump Output Stage

The *UP* signal is high when the reference signal is operating at a higher frequency than the feedback signal. The charge pump forces current into the loop filter when the *UP* signal is high. This causes the VCO control voltage to rise. This increases the VCO frequency and brings the feedback signal to the same frequency as the reference signal.

The *DOWN* signal is high when the reference signal is operating at a lower frequency then the feedback signal. The charge pump forces current out of the loop filter when the *DOWN* signal is high. This causes the VCO control voltage to fall. This decreases the VCO frequency and brings the feedback signal to the same frequency as the reference signal.

This interaction between the PFD, charge pump, and loop filter is shown in Figure 35. Here the UP signal is high. This forces current into the loop filter and causes the VCO control voltage to rise.

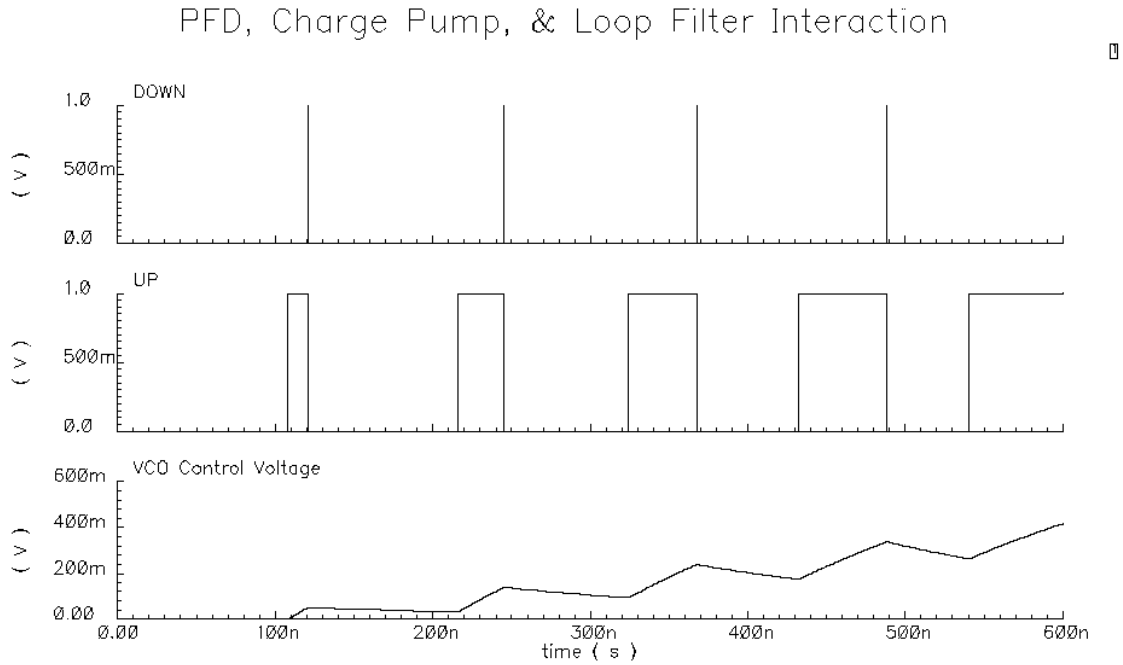

Figure 35 - PFD, Charge Pump, and Loop Filter Interaction

The value of the charge pump current determines the phase detector gain, K_{PD}. Each reference cycle has a duration of $2p/w_{ref}$ seconds. The time that the *UP* or *DOWN* signals are high determine the amount of current that gets delivered to the loop filter. Using the time that the *UP* and *DOWN* signals are high, given in (51), gives the average error current, i_e, over a cycle[40].

$$i_e = \frac{t_{high}}{t_{cycle}}(\text{Charge Pump Current}) = \frac{Iq_e}{2p} \qquad \textbf{(52)}$$

This means that the phase detector gain is the following.

$$K_{PD} = \frac{I}{2p} \text{ (amps/radian)} \qquad \textbf{(53)}$$

Loop Filter

The loop filter converts the charge pump error current, I_e, into the VCO control voltage v_c. Ignoring the smaller capacitor C_2 as explained earlier, the loop filter has the following transfer function.

$$F(s) = \frac{V_c(s)}{I_e(s)} = \frac{R\left(s + \frac{1}{RC_1}\right)}{s} \qquad \textbf{(54)}$$

The frequency response of the loop filter is plotted in Figure 36. The effect of the pole at zero is seen by a very high low frequency gain. The zero causes the transfer function to level off at high frequencies.

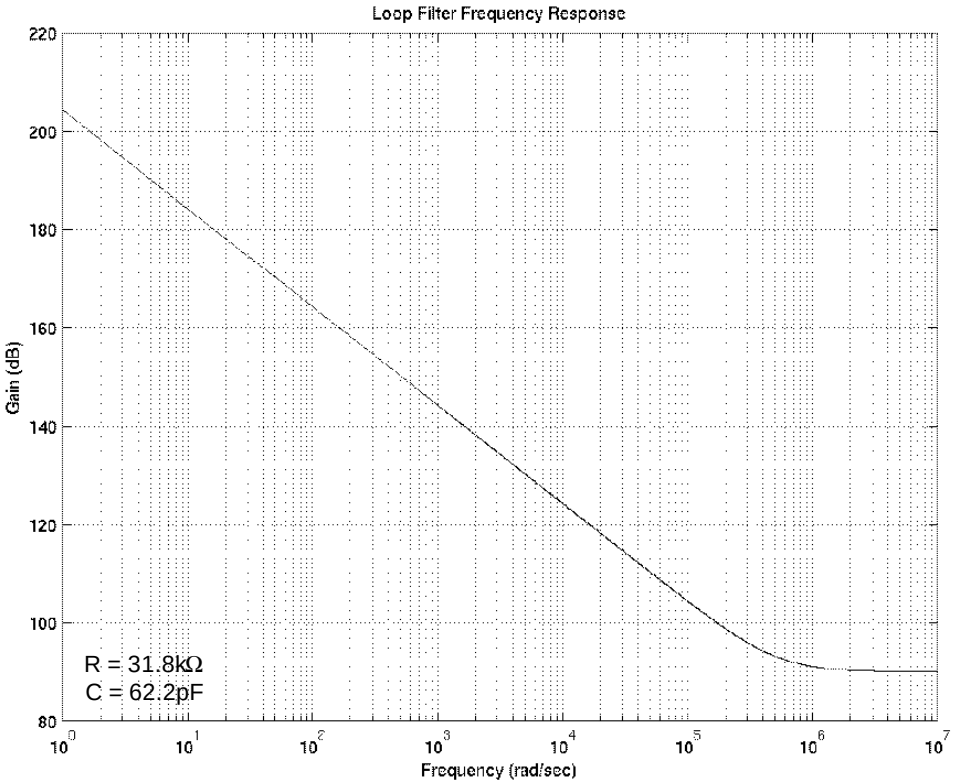

Figure 36 - Loop Filter Frequency Response

The loop filter is the critical building block that determines the loop dynamics. In a charge pump PLL, the natural frequency and the damping factor is set independently by the values of the components used in the loop filter. The capacitor, C_1, sets the natural frequency. The resistor sets the damping factor.

Voltage-Controlled Oscillator

The voltage-controlled oscillator generates an output signal with a frequency that is dependent on the input control voltage by the following:

$$w_{out} = w_0 + K_{VCO} v_c \qquad \textbf{(55)}$$

The transfer characteristic of the VCO is given in Figure 37. It has a center frequency of w_0. The slope of the transfer characteristic in the linear region is equal to the VCO conversion gain K_{VCO}.

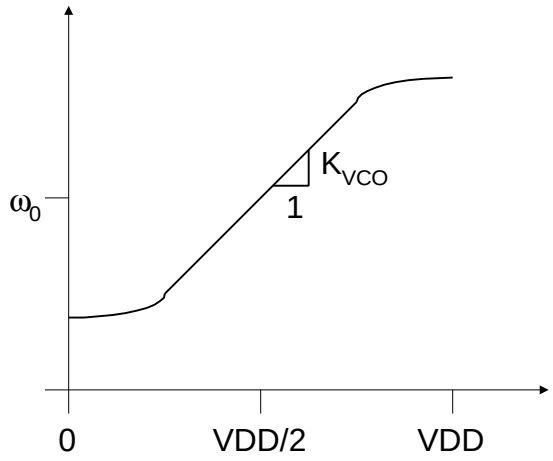

Figure 37 - VCO Transfer Characteristic

There are several different types of VCOs. Some VCO architectures include RC, switched-capacitor, LC, crystal, relaxation, and ring oscillators[38]. The oscillators most commonly used in integrated PLL design are the LC tuned and the ring oscillator[10,22,23,35,41].

The LC oscillator is shown in Figure 38[11]. This circuit is generally preferred in high performance frequency synthesizers because of its superior phase noise performance. Recent integrated LC oscillator results are shown in Table 4.

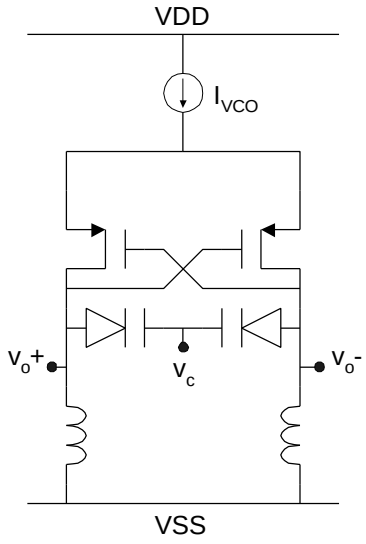

Figure 38 - LC Voltage-Controlled Oscillator

Table 4 - Recent Integrated LC Voltage-Controlled Oscillator Results

Source	Frequency Range	Phase Noise
[35]	1.62-1.99GHz 0.84-1.03GHz	-113dBc/Hz @ 200kHz -108dBc/Hz @ 100kHz
[42]	1.885-2.035 GHz	-136dBc/Hz @ 4.7MHz
[43]	4.9-5.25GHz	-104.5dBc/Hz @ 5MHz
[44]	5.51-6.53GHz	-98.4dBc/Hz @ 1MHz

A ring oscillator is shown in Figure 39[38]. This circuit consists of an odd number of inverting amplifiers placed in a feedback loop. Recent integrated ring oscillator results are shown in Table 5.

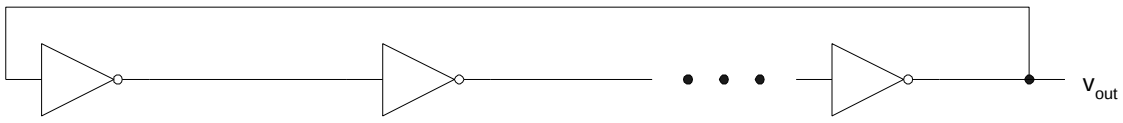

Figure 39 - Ring Oscillator

Table 5 - Recent Integrated Ring Voltage-Controlled Oscillator Results

Source	Frequency Range	Phase Noise
[41]	320-926MHz	-83dBc/Hz @ 100kHz
[45]	660-900MHz	-83dBc/Hz @ 100kHz
[46]	350k – 707MHz	-82dBc/Hz @ 100kHz

The integrated ring voltage-controlled oscillators typically have a wider tuning range then the LC oscillators. However, this increased tuning range comes at the price of poorer phase noise performance when compared to LC oscillators.

Loop Divider Circuitry

The loop divider divides the VCO output frequency to produce the VCO feedback signal. The loop division factor determines the output frequency relation with the input reference frequency. The loop divider can be realized in many different ways depending on the type of synthesizer architecture used. The most common circuits used in the loop divider are prescaler circuits, dual-modulus prescalers, and counters. Detailed applications of these circuits are included in the earlier frequency synthesizer architectures section.

A General Fully Integrated PLL Design Procedure

The PLL is a complex system to design. Performance and stability considerations must be accounted for in the design procedure. The entire design procedure for a fully integrated PLL is generally an iterative process. Typically design parameters are adjusted from the mathematical model to the system level model to the transistor level design. The following design procedure describes how to define the system level parameters for a fully integrated charge pump PLL. As an example, the charge pump PLL will be used as a frequency synthesizer in the GSM cellular communications system. It will be required to synthesize 890 to 960MHz with a resolution of

200kHz[47] using a power supply of 2.7V. The following system level parameters need to be defined.

1. Charge Pump Current I
2. Loop Filter Components $R, C_1, \& C_2$
3. VCO Tuning Range
4. VCO Gain K_{VCO}
5. Loop Division Factor N

Step 1 Determine VCO Tuning Range

The maximum and minimum output frequencies determine the PLL frequency range. This is the range of frequencies under which the PLL is operating. The frequency range for this PLL is 890 to 960MHz. This requires that the VCO have a tuning range at least 890 to 960MHz.

$$\text{VCO Tuning Range} \geq 890 - 960\text{MHz} \quad \textbf{(56)}$$

Step 2 Determine Loop Division Ratio Range.

The loop division ratio range is the range that the modulus, N, is operating. This is largely determined by the synthesizer's frequency resolution. Here the frequency resolution is the channel spacing of 200kHz. If it is assumed that a 200kHz reference is used to achieve a 200kHz resolution, N will have the following range.

$$4450 \leq N \leq 4800 \quad \textbf{(57)}$$

The value of N has an effect on other loop parameters. Therefore, in defining the other parameters the geometric mean of N will be used.

$$N_{mean} = \sqrt{N_{\min} N_{\max}} = 4622 \quad \textbf{(58)}$$

Step 3 Determine Damping Factor, ζ_{mean}

The damping factor, ζ_{mean}, has an effect on the speed and stability of the system. As a compromise between speed and stability, ζ_{mean} is optimally set to the following value.

$$\zeta_{mean} = \frac{1}{\sqrt{2}} \approx 0.707 \qquad \textbf{(59)}$$

Step 4 Determine Natural Frequency, w_n

The natural frequency has a significant effect on the loop bandwidth. For a charge pump PLL with a passive loop filter, the loop bandwidth, w_{3dB}, is related to the natural frequency by the following[34]:

$$w_{3dB} = w_n \left[2\zeta^2 + 1 + \sqrt{\left(2\zeta^2 + 1\right)^2 + 1} \right]^{1/2} \qquad \textbf{(60)}$$

If $\zeta = 0.707$ is assumed, this results in the following:

$$w_{3dB} = 2.06 w_n \qquad \textbf{(61)}$$

It is desirable to make the loop bandwidth less then $1/10$ of the input reference frequency (200kHz) in order to avoid the continuous time approximations of the charge pump PLL breaking down. However, it is desirable to make the loop bandwidth as wide as possible in order to suppress the VCO phase noise that is the dominant source of phase noise for the integrated PLLs. As a compromise between stability and noise performance, the loop bandwidth is set to the following:

$$w_{3dB} = \frac{w_{ref}}{10}(0.75) = 94.2 \, krad/s \qquad \textbf{(62)}$$

This results in the natural frequency equal to the following for $\zeta = 0.707$.

$$w_n = \frac{w_{3dB}}{2.06} = 45.8 \, krad/s \qquad \textbf{(63)}$$

Step 5 Determine VCO Gain

The tuning range of the VCO and the VCO control voltage range set the VCO gain. From step 1 it was shown that the VCO needs to tune a minimum frequency range of 890 to 960MHz. The VCO control voltage range is limited by the power supply and the voltage levels necessary to keep the charge pump in saturation. The charge pump will

no longer behave ideally if the VCO control voltage rises too high or falls too low. Therefore, the VCO control voltage is limited to a minimum of a V_{DSAT} from the supply rails. With a power supply of 2.7V, a VCO control range of 1.6V can be assumed with sufficient margin to handle process variations. This results in the following VCO gain.

$$K_{VCO} = \frac{2p\left(960\text{MHz} - 890\text{MHz}\right)}{1.6\text{V}} \frac{rad}{sV} = 275 \frac{Mrad}{sV} \qquad \textbf{(64)}$$

Step 6 Determine Charge Pump Current and Loop Filter Capacitor

The charge pump current and the loop filter capacitor can be determined by the relationship between the natural frequency, the loop division factor, and the VCO gain. It is desirable to have a high charge pump current because this will result in a higher loop gain and thus a more stable system. However, having a large charge pump current will result in a large capacitor as shown in the following equation which is derived from equations (47) and (53).

$$C_1 = \frac{IK_{VCO}}{2pNw_n^2} \qquad \textbf{(65)}$$

A large capacitor will translate into increased circuit area. Therefore a design tradeoff between loop gain and silicon area arises. The charge pump current can be set so that it will result in a decent loop gain without producing too large of a capacitor as shown in the following:

Set $I = 10mA$

$$C_1 = \frac{\left(10mA\right)\left(275\frac{Mrad}{sV}\right)}{2p\left(4622\right)\left(45.8\frac{krad}{s}\right)^2} = 45.1pF \qquad \textbf{(66)}$$

Step 7 Determine Other Loop Filter Components

The loop filter resistor is used to set the damping factor as shown in the following equation which is derived from (48).

$$R = \frac{2\zeta}{w_n C_1} = \frac{2(0.707)}{\left(45.8\frac{krad}{s}\right)(45.1pF)} = 685k\Omega \qquad \textbf{(67)}$$

The second loop filter capacitor, C_2, used to supress ripple in the control voltage is fixed to be less than a tenth of the main loop filter capacitor C_1 so that the loop can still be considered a second order system.

$$C_2 < \frac{C_1}{10} = 4.51pF \qquad \textbf{(68)}$$

A value of 4pF would be appropriate for C_2 in this design.

This design procedure has defined all the key system level parameters required to start the design. The next step in the circuit design is to construct a system level macromodel which allows simulation of the loop dynamics. Then transistor level design is started. The design process is generally an iterative process. For example, non-idealities introduced by the transistors can be compensated by adjusting parameters in the system level macromodel and then translating those adjustments back to the transistor level. There are usually many design iterations involved in such a complex system level design as a PLL.

A MULTI-BAND PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER

This section describes the development of a multi-band phase-locked loop frequency synthesizer. The design process is explained from the project definition down to the transistor level design. The building block and system level simulations are presented. A design of a classic digital PLL is also produced for comparison.

The Multi-Band PLL System

Unlike typical phase-locked loops which cover a given frequency range with only one band of operation, the multi-band PLL is a phase-locked loop circuit that covers a given frequency range with multiple bands of operation. These bands are cascaded in frequency to cover the entire frequency spectrum of interest. The frequency synthesizer may be designed to synthesize a continuous frequency spectrum or to synthesize discrete bands of frequencies as shown in Figure 40.

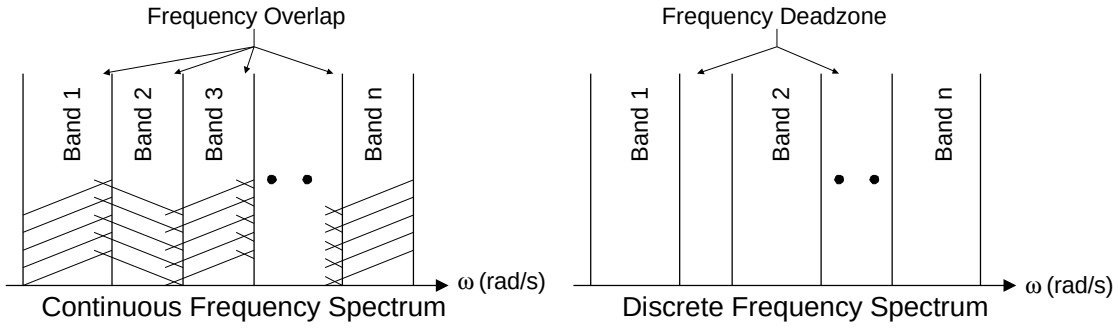

Figure 40 - Multiple Frequency Band Systems

These different frequency bands are realized in the multi-band PLL with a switched tuning VCO shown in Figure 41.

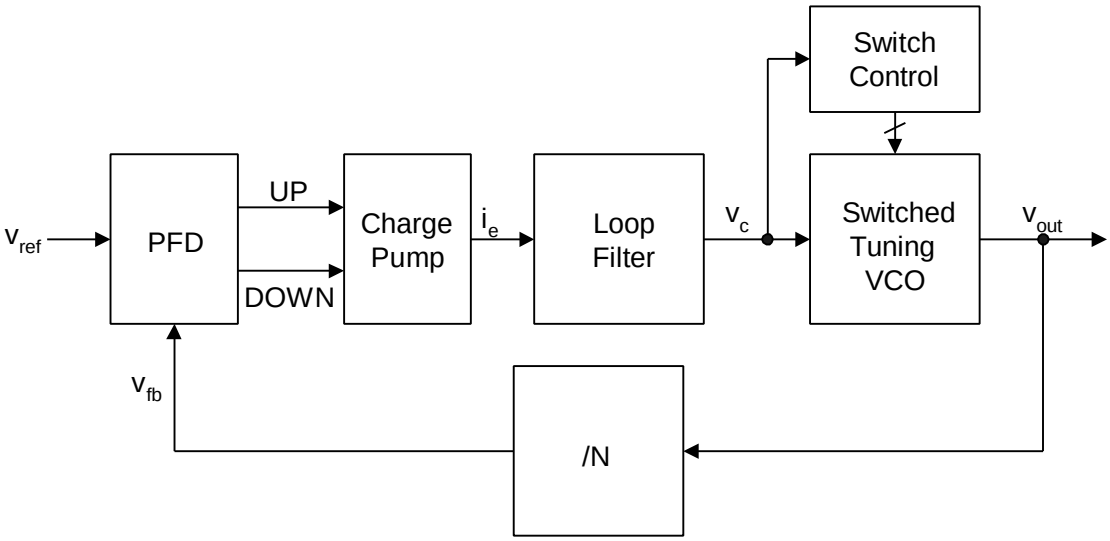

Figure 41 - Multi-Band Phase-Locked Loop Frequency Synthesizer

The switched tuning VCO is a voltage-controlled oscillator that is controlled continuously with a controlling voltage and discretely by switching in different tuning loads. The discrete tuning can be thought of as changing the channel or band of the oscillator. One advantage of using a switched tuning oscillator is that a wide frequency range can be achieved while maintaining a relatively low VCO conversion gain, K_{VCO}. This is critical in high frequency integrated circuit design because it is difficult to design a VCO with a high K_{VCO}. A low VCO conversion gain also aids in the phase noise performance of the PLL system because VCO control line noise is directly proportional to the square of K_{VCO}.

Multi-Band PLL Switch Control Mechanism

The switch control network works by monitoring the VCO control voltage. If the PLL is in a dynamic state trying to acquire lock, the VCO control voltage will rise or fall. This is illustrated in Figure 42 that shows the PLL's VCO control voltage response to a frequency step input.

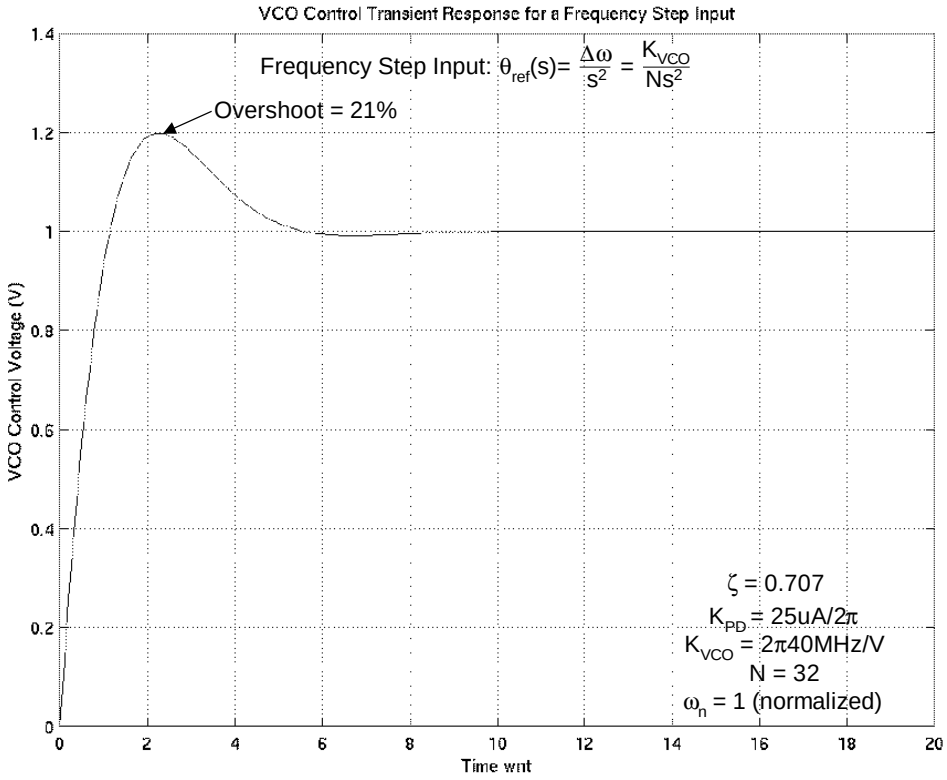

Figure 42 - VCO Control Voltage Response to a Frequency Step Input

The switch control network detects when the VCO control voltage crosses a certain positive or negative threshold and changes the VCO channel by switching in or out different tuning loads. The VCO control voltage is then grounded to set the VCO in the middle of the next channel and to reset the system. This switch control mechanism is shown in Figure 43.

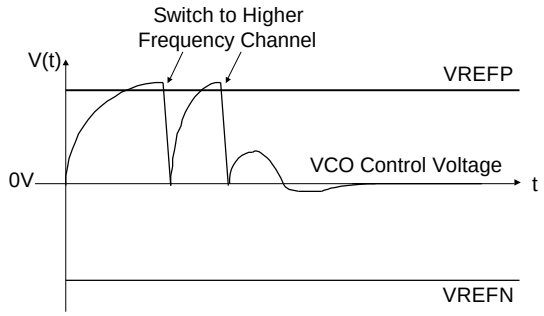

Figure 43 - Discrete Tuning System Mechanism

In this case the output of the PLL is initially oscillating too slow. The VCO control voltage rises as the loop dynamics will take over. After the VCO control voltage passes the positive voltage threshold, *VREFP* , the channel of the oscillator is changed to the next higher frequency channel. The VCO control voltage is then grounded to set the oscillator operating in the mid-band of the new channel. However, the oscillator is still not in the right channel. Therefore the mechanism repeats. The VCO control voltage rises and crosses the positive threshold, the oscillator's channel is changed to the next highest frequency channel, and the VCO control voltage is grounded. Finally, the oscillator is in the right channel and the system locks.

This type of switch control mechanism always keeps the VCO control voltage between the positive and negative thresholds. This mechanism aids in low voltage applications because the VCO control voltage doesn't have to cover a wide range to output a wide frequency range. Instead, the different tuning elements are switched in and the VCO control voltage just sweeps between the two thresholds.

Also, this type of switch mechanism aids in the acquisition time of the PLL. The VCO control voltage doesn't have to climb slowly up or down like in a regular PLL. Instead, the VCO is switched rapidly to the mid-band of the next channel and is able to acquire lock quicker.

Multi-Band PLL Channel Design

It can be seen from Figure 42 that the PLL has a characteristic overshoot when acquiring lock. Attempting to synthesize an edge of band frequency can cause oscillation between the different bands. This is because the overshoot will cause the PLL to jump to the next highest or lowest frequency band that cannot synthesize the desired frequency. The PLL will then return to the previous band. However, the overshoot will again push it out of the band and the system will oscillate between adjacent bands. This is illustrated in Figure 44.

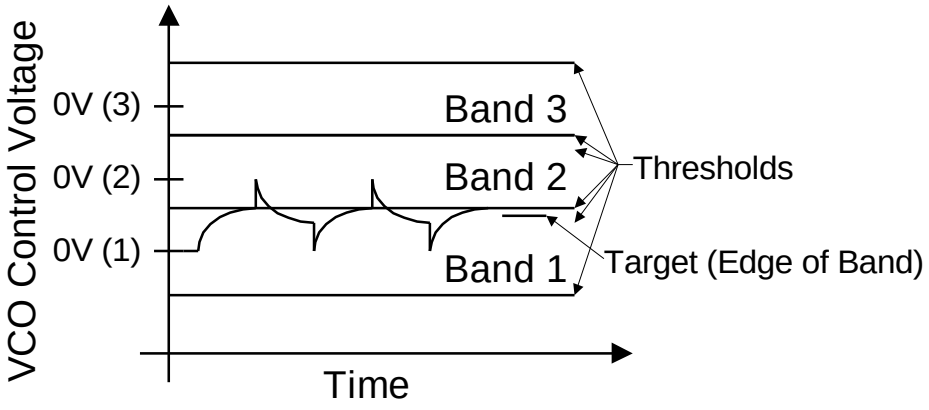

Figure 44 - Overshoot Causing Oscillation Between Frequency Bands

The solution to this stability problem is to force the PLL to always lock away from the edges of the band. This is achieved by providing a frequency overlap for a continuous frequency system and by providing a frequency cushion for a discrete system. In a continuous frequency system the frequency overlap consists of spectrum that is shared by adjacent channels. In a discrete frequency system the frequency cushion is the unusable spectrum at the edges of the discrete bands. This is illustrated in Figure 45.

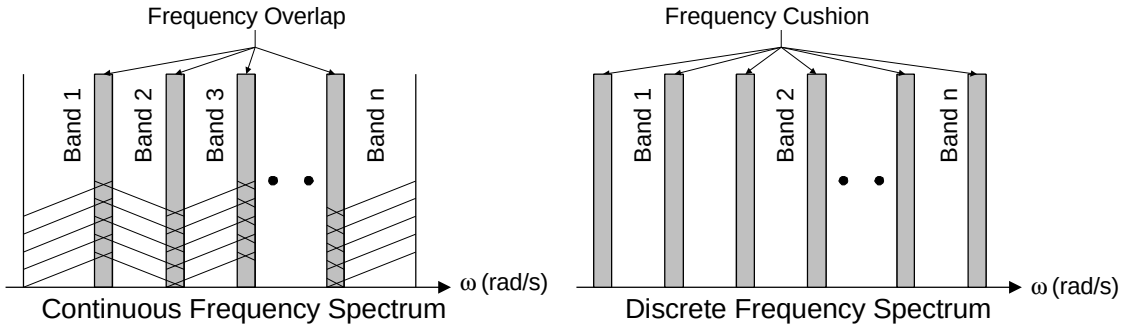

Figure 45 - Frequency Overlap and Cushion Introduced For Stability

The characteristic overshoot of the PLL's VCO control voltage to a frequency step input is used to partly determine the amount of channel overlap or frequency cushion by converting this overshoot voltage into a frequency value. This conversion can be made by knowing the VCO's conversion gain, K_{VCO}. The overshoot is a function of the damping factor, z, and can be determined with the aid of a mathematical model of the PLL in the lock range. The characteristic overshoot of a system with a damping factor of 0.707 is 21% greater then the final value as shown before in Figure 42.

A positive threshold, L^+, and a negative threshold, L^-, can be assumed to determine the required frequency overlap based on the VCO control voltage's overshoot. Without loss of generality consider the case of Figure 46. This example is of a PLL with a damping factor of 0.707. The PLL's channel one has a center frequency , f_{c1}, that corresponds to a voltage of 0V. One can see that the VCO control voltage settles onto a value of $0.83L^+$ in channel one. The peak channel one VCO control voltage reaches a value of $L^+ = 1\text{V}$. The actual overshoot voltage from the final value is the following:

$$\text{Overshoot Voltage} q = L^+(1-0.83) = 0.17L^+ \qquad \textbf{(69)}$$

Observe that in this case the PLL would tend to go to the next band when attempting to synthesize frequencies that require a VCO control voltage greater than $0.83L^+$.

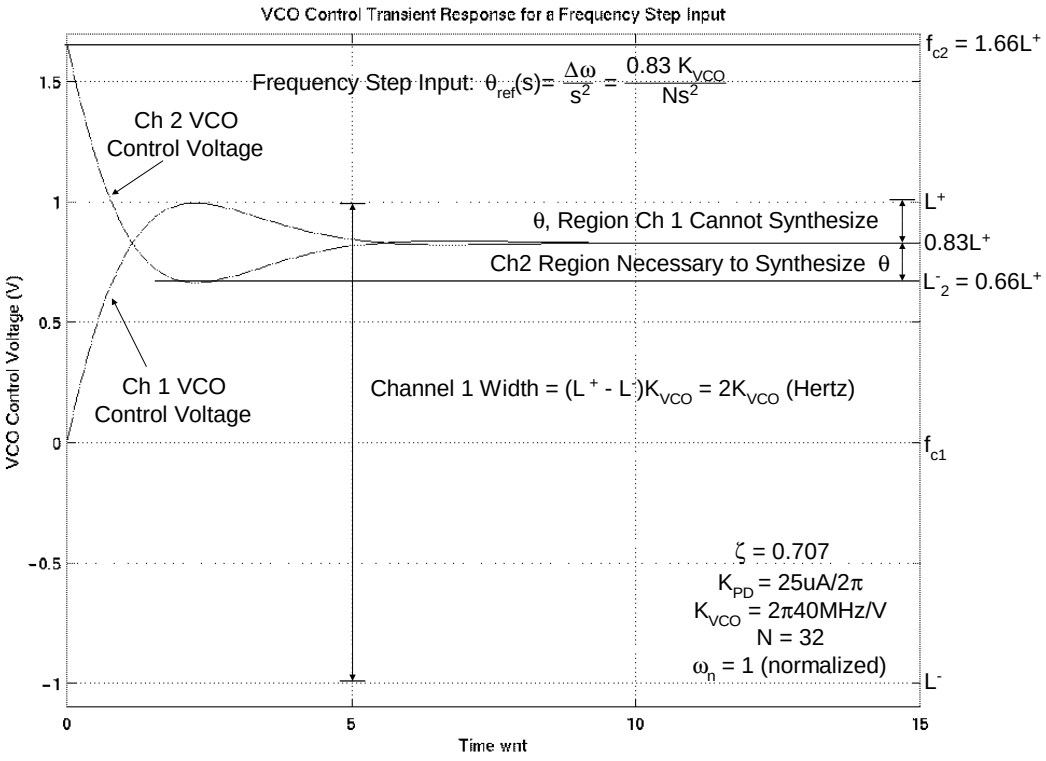

Figure 46 - Determination of Frequency Overlap or Cushion

The frequencies that correspond to the voltage values between $0.83L^+$ and L^+ cannot be synthesized by channel one because of the overshoot. The next higher channel must synthesize these frequencies. Channel two is centered at a higher frequency f_{c2}. Mapping channel two to the voltage range of channel one results in f_{c2} having a positive voltage value. The center frequency of channel two must be placed so that the frequencies that correspond to $0.83L^+$ and L^+ can be synthesized. Knowing that the overshoot q is equal to $0.17L^+$, L^- of the second channel must be placed at $0.66L^+$ in order to synthesize the frequency that corresponds to $0.83L^+$. This implies that the amount of frequency overlap between adjacent channels is equal to the following:

$$\text{Frequency Overlap (Due to Overshoot)} = 2qK_{VCO} = 2(0.17L^{+})K_{VCO} = 0.34L^{+}K_{VCO} \quad \textbf{(70)}$$

This frequency overlap is represented as a percentage of the total channel frequency range by the following:

$$\text{\% Frequency Overlap (Due to Overshoot)} = \frac{\text{Frequency Overlap}}{\text{Channel Frequencies}} = \frac{2qK_{VCO}}{2L^{+}K_{VCO}} = \frac{2(0.17L^{+})K_{VCO}}{2L^{+}K_{VCO}} = 17\% \quad \textbf{(71)}$$

For a discrete frequency system, the frequencies between ±0.83V and ±1V cannot be synthesized. This area is the frequency cushion of the system. The percentage of frequency cushion due to overshoot is equivalent to the following:

$$\text{\% Frequency Cushion (Due to Overshoot)} = \frac{\text{Frequency Cushion}}{\text{Channel Frequencies}} = \frac{2(L^{+} - 0.83L^{+})K_{VCO}}{2L^{+}K_{VCO}} = 17\% \quad \textbf{(72)}$$

However, the above analysis assumes a continuous time system. The charge pump PLL is in fact a discrete time system. A result of this is the ripple of the VCO control voltage due to the charging and discharging of the loop filter by the charge pump. This ripple effectively increases the frequency overlap or cushion in a multi-band PLL design. This ripple will be worse when the input frequency is lowered to close to ten times the loop bandwidth. Here the loop becomes a very strong discrete time system and granularity problems occur[40]. The reason for this is as the input frequency drops, the time the charge pump is charging or discharging the loop filter is increasing. This causes larger ripple. The interaction between the charge pump and the loop filter is illustrated in Figure 47.

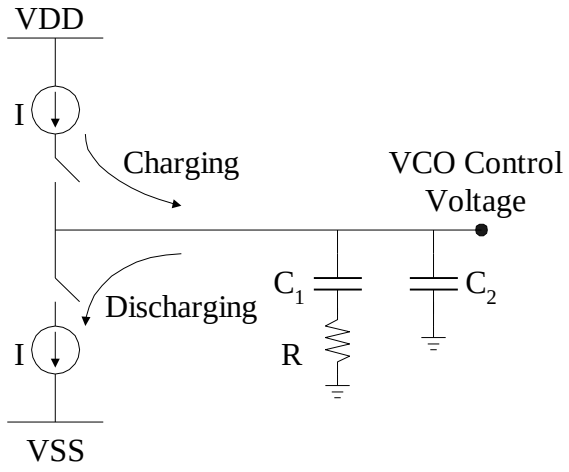

Figure 47 - Charge Pump and Loop Filter Interaction

Here the filter impedance is equal to the following:

$$Z(s)=\frac{\frac{1}{C_2}\left(s+\frac{1}{RC_1}\right)}{s^2+\frac{s(C_1+C_2)}{RC_1C_2}} \qquad \textbf{(73)}$$

The charge pump current is modeled as a step function I/s. This yields the following voltage function.

$$V(s)=I(s)Z(s)=\frac{I}{s}\frac{\frac{1}{C_2}\left(s+\frac{1}{RC_1}\right)}{s^2+\frac{s(C_1+C_2)}{RC_1C_2}} \qquad \textbf{(74)}$$

In the time domain this is the following function.

$$V(t)=I\left(\frac{RC_1^2}{(C_1+C_2)^2}+\frac{t}{C_1+C_2}-\frac{RC_1^2e^{-\frac{C_1+C_2}{RC_1C_2}t}}{(C_1+C_2)^2}\right) \qquad \textbf{(75)}$$

This function is plotted in Figure 48.

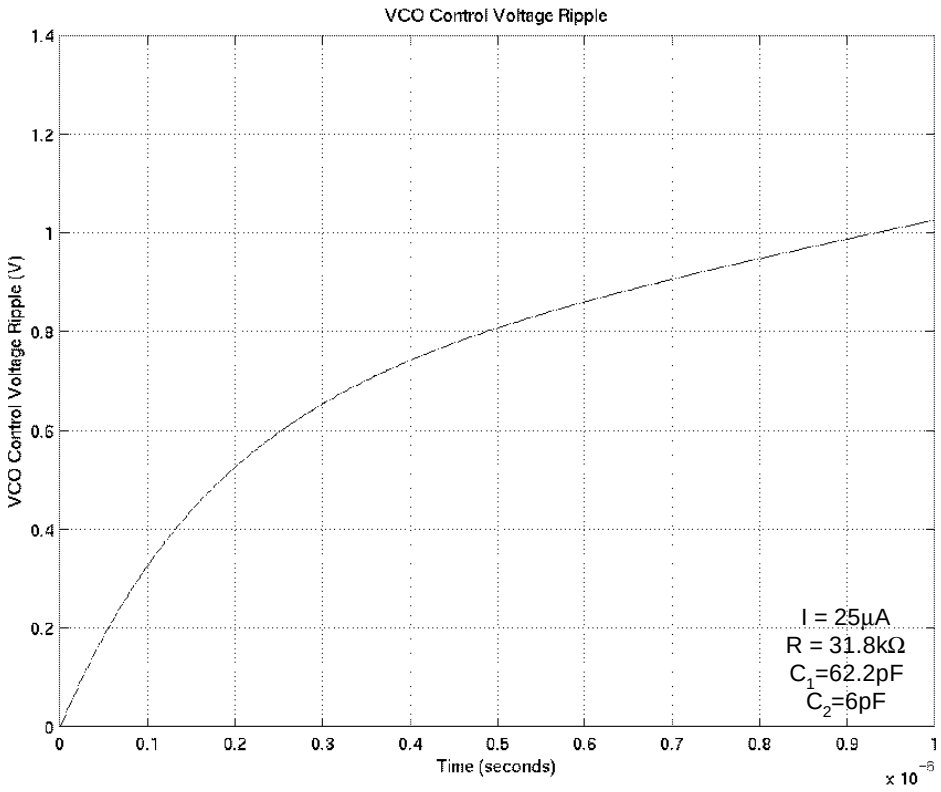

Figure 48 - VCO Control Voltage Ripple Function

It can be observed that for short values of t, which correspond to a high input reference frequency, $v(t)$ is an exponentially rising function. As t increases, with a lower input reference frequency, $v(t)$ becomes more linear with greater amplitude. This results in higher ripple for a low input reference frequency.

The value of overshoot due to the ripple must then be analyzed at the lowest input reference frequency. Simulating an input frequency of thirteen times the loop bandwidth with a behavioral model that correctly models the charge pump yields an overshoot with the following ripple characteristic shown in Figure 49.

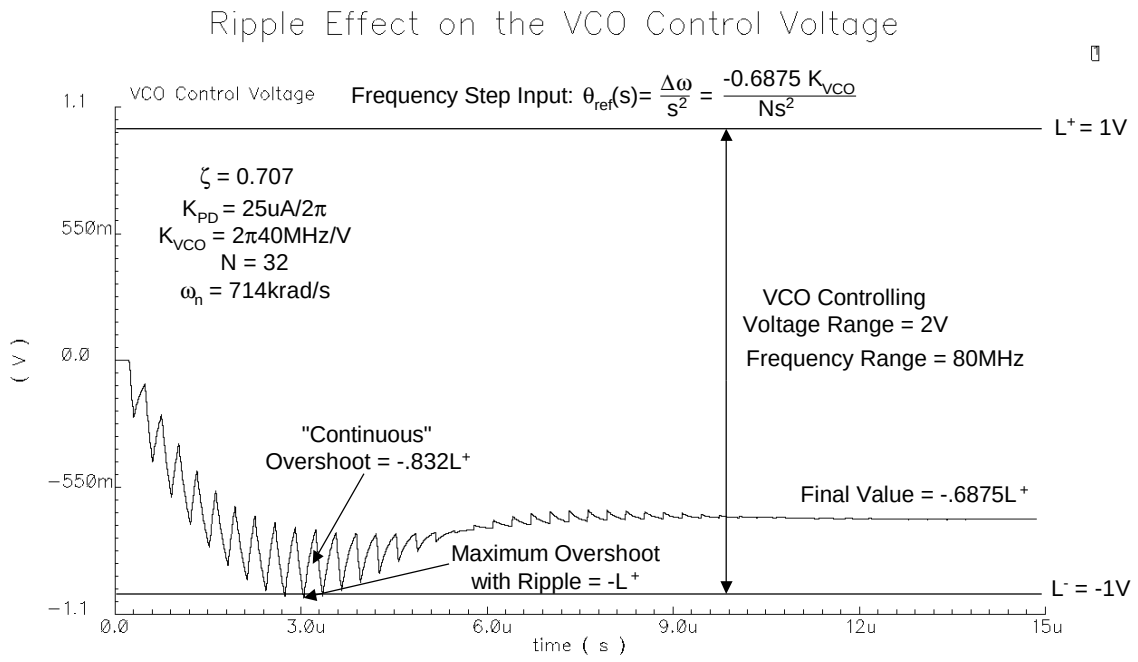

Figure 49 - Effect of Ripple on the VCO Control Voltage

This system settles on a final value of $-0.6875L^+$. This results in a "continuous" overshoot of $-0.832L^+$ for a damping factor of 0.707. However the ripple due to the charge pump PLL pushes the overshoot to $-L^+$. The amount of frequency overlap or cushion due to the ripple can be represented as a percentage of the total channel frequency range by the following:

$$\%\ \text{Frequency Overlap(Due to Ripple)} = \frac{\left|(\text{Maximum Ripple - Continuous Overshoot})\right|K_{VCO}}{\text{Channel Frequencies}} = \frac{\left(L^+ - .832L^+\right)K_{VCO}}{2L^+K_{VCO}} = 8.4\% \qquad \textbf{(76)}$$

One important characteristic of the ripple is that it is not a function of the final value like the characteristic overshoot. Rather, it is a function of the time that the charge pump is charging or discharging the loop filter. The important thing to be observed here is that the ripple will have similar magnitude if it is near the channel edge or in the middle

range of the channel. Therefore, the percentage of frequency overlap due to the VCO control voltage ripple is a strong function of the channel's controlling voltage range or correspondingly the channel's frequency range. A wide frequency channel will have a large controlling voltage range for a given K_{VCO}. A large controlling voltage range means the voltage ripple will not be a significant percentage of the controlling voltage range. However, as the controlling voltage range is decreased, meaning a lower frequency range channel, the ripple becomes a greater percentage of the controlling voltage range. Therefore, it is helpful in knowing the controlling range of the VCO when designing the channels.

In summary, the overlap value is a summation of the continuous overshoot and the ripple as given in the following equation.

$$\%\,\text{Overlap(Total)} = \%\,\text{Continuous Overlap} + \%\,\text{Ripple} \qquad \textbf{(77)}$$

In this equation the percentage due to continuous overlap is only a function of the damping factor. 17% continuous overlap is found for a typical damping factor of 0.707. The percentage due to the ripple is a more complex function. The maximum overlap necessary must be evaluated at the lowest frequency and the percentage is largely a function of the channel voltage width. In the example presented earlier a value of 8.4% was found for an input reference frequency thirteen times the loop bandwidth. This gives a total of 25.4%. If this overlap is not met the PLL will oscillate between bands as shown in Figure 50.

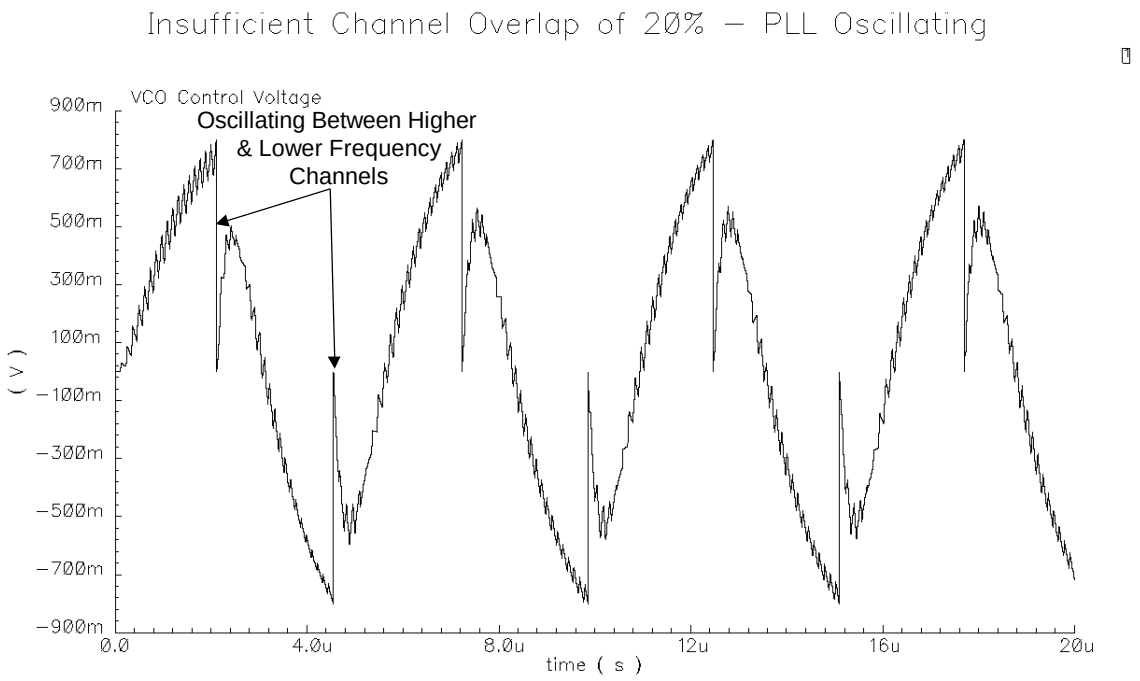

Figure 50 - PLL Oscillating Due to Insufficient Channel Overlap

Here there is only a channel overlap of 20%. As this overlap is increased to 30% it is observed in Figure 51 that the PLL becomes a stable system.

A value of 30% is a good value to start with in the design procedure. This value may be changed due to the application. If extremely low voltage tuning ranges are used or if input reference frequencies near ten times the loop bandwidth are used there may need to be more then 30% overlap due to a large ripple effect. If the input reference frequency is well above ten time the loop bandwidth then the overlap condition may be lowered because the loop approaches more of a continuous time behavior and the ripple is not as evident.

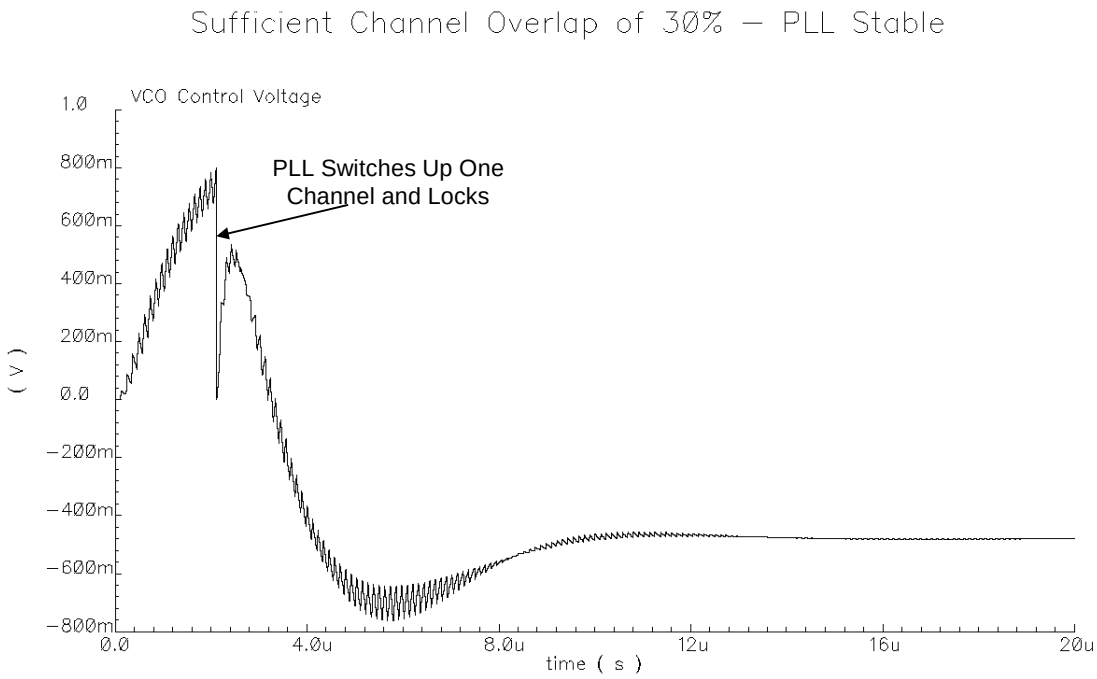

Figure 51 - PLL Locking with Sufficient Channel Overlap

The Multi-Band PLL System Design Methodology

A top-down design procedure is implemented for the multi-band PLL frequency synthesizer as shown in Figure 52. The project is first defined and specifications are decided upon. The specifications are given in Table 6.

Table 6 - Multi-Band PLL Frequency Synthesizer Specifications

Frequency Range	100 – 300MHz
Phase Noise @ 50kHz Offset	< -90dBc/Hz
Lock-In Time	< 15μs
Power Supply	2.7V

A mathematical macromodel is then generated using MATLAB to investigate the PLL's performance in the locked state and to perform stability analysis. This mathematical macromodel aids in defining design parameters such as charge pump current, VCO gain,

loop filter components, and the division ratio. A behavioral macromodel is then generated using SpectreHDL. The behavioral macromodel models the different blocks of the PLL with HDL code. The behavioral macromodel aids in an increased understanding of the loop dynamics and allows the switch control logic to be designed at a behavioral level. The amount of frequency overlap in the channels is determined with the aid of the behavioral macromodel. This macromodel allows for quick design changes without the hassle of transistor level design. The transistor level design is started after the behavioral macromodel is well defined and considered an ideal system. The transistor level designs of each block are performed using CADENCE. The transistor level blocks are substituted into the behavioral macromodel block by block to investigate their performance in the system. The ability to interface transistor level blocks with the behavioral macromodel is very powerful. The non-idealities of the transistor level blocks cause some changes in the system level that are rapidly accommodated with the behavioral macromodel. Layout begins after the transistor level design is completed. The blocks of the PLL are laid out as individual cells. The extracted layout blocks are substituted into the transistor level system block by block in a method similar to what is done with the transistor level and behavioral macromodel. After the layouts are completed a final chip level simulation is run on the prototype chips to verify adequate circuit performance. The final designs are then sent for fabrication.

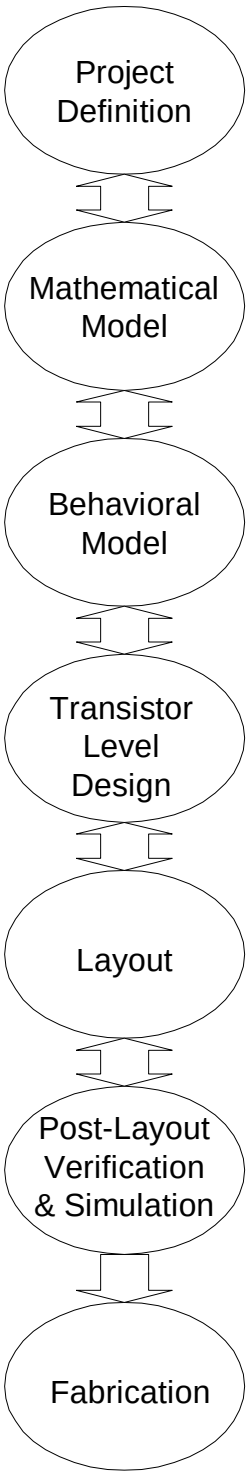

Figure 52 - Multi-Band PLL Frequency Synthesizer Design Flow

Mathematical Design and Modeling

Initial design parameters are computed through a mathematical procedure similar to the one outlined in the previous section. The parameters' effects on loop performance are then analyzed with a mathematical model of the loop.

Mathematical Design Procedure

The design procedure of the multi-band PLL frequency synthesizer is the one described in the previous section with some modifications to handle the switched tuning VCO.

Step 1 Determine VCO Tuning Range

The range of frequencies that the synthesizer must output defines the VCO tuning range. The synthesizer must output between 100 to 300MHz in this design. Therefore, the VCO tuning range is the following.

$$\text{VCO Tuning Range} = 100 - 300\text{MHz} \qquad \textbf{(78)}$$

Step 2 Determine Loop Division Ratio, N

The loop division factor is set to an integer value N in this prototype design. The value of $N = 32$ is chosen such that it is a typical value used in prescalers. Adjusting the input reference frequency changes the output frequency of the synthesizer.

Step 3 Determine Damping Factor, ζ

The damping factor is set to yield an optimally flat frequency response. This results in ζ being equal to the following.

$$\zeta = \frac{1}{\sqrt{2}} \approx 0.707 \qquad \textbf{(79)}$$

Step 4 Determine Natural Frequency, ω_n

The PLL's phase error responds to any stimulus with a dampened oscillation that has a frequency equal to the natural frequency. The natural frequency has a strong effect on

the loop 3dB bandwidth w_{3dB}. In order to insure that the loop's continuous time approximations hold, w_{3dB} must be set less than or equal to a tenth of the lowest input reference frequency. In this design the lowest output frequency will be 100MHz. This means that the lowest input reference frequency will be the following.

$$\text{Lowest Input Reference Frequency} = \frac{100\text{MHz}}{32} = 3.125\text{MHz} \qquad \textbf{(80)}$$

This means that the absolute widest loop bandwidth can be 312.5kHz for the continuous time approximations to hold up. A loop bandwidth 25% lower than this is chosen in the design to allow sufficient margins for process and temperature variations.

$$w_{3dB} = (0.75)(2p)312.5\text{kHz} = 1.47\,Mrad/s \qquad \textbf{(81)}$$

The natural frequency is equal to the following for a damping factor of 0.707.

$$w_n = \frac{w_{3dB}}{2.06} = \frac{1.47\,Mrad/s}{2.06} = 714\,krad/s \qquad \textbf{(82)}$$

Step 5 Determine Frequency Bands and Average VCO Gain, K_{VCO}

This part of the design procedure differs from the earlier design procedure because the wide frequency spectrum has been split up into different frequency bands. The 200MHz frequency spectrum is split into four 65MHz bands of operation. A frequency overlap of approximately 30% or 20MHz between the channels is chosen to avoid oscillation when attempting to acquire lock along the edges of the channels. Assuming a tuning range of approximately 60% of the power supply gives a voltage tuning range of 1.6V. This yields the following average VCO conversion gain.

$$K_{VCO} = \frac{(2p)65\text{MHz}}{1.6\text{V}} = 255\,Mrad/sV \qquad \textbf{(83)}$$

The spectrum allocation is illustrated in Figure 53.

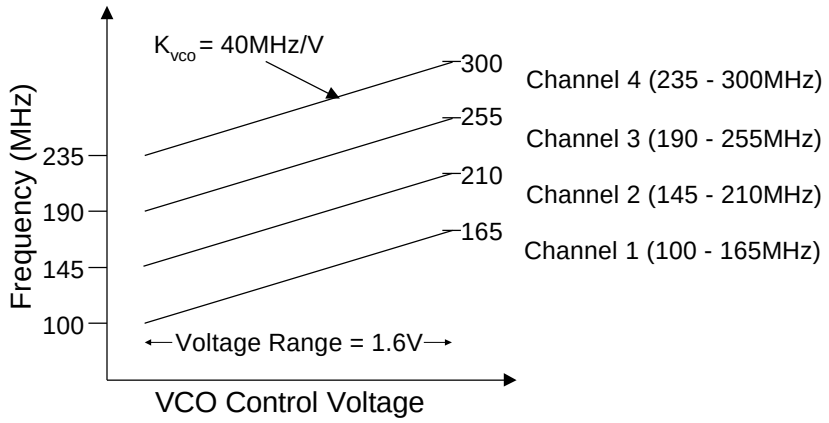

Figure 53 - Multi-Band PLL Frequency Synthesizer Frequency Bands

Step 6 Determine Charge Pump and Loop Filter Capacitor

The charge pump current is set so that a decent loop gain is obtained without producing too large of a capacitor as shown in the following.

$$\text{Set } I = 25mA$$

$$C_1 = \frac{(25mA)\left(255\frac{Mrad}{sV}\right)}{2p(32)\left(714\frac{krad}{s}\right)^2} = 62.2\,pF \qquad \textbf{(84)}$$

Step 7 Determine Other Loop Filter Components

The loop filter resistor is used to set the damping factor of the PLL. The resistor is computed to be the following.

$$R = \frac{2z}{w_n C_1} = \frac{2(0.707)}{\left(714\frac{krad}{s}\right)(62.2\,pF)} = 31.8k\Omega \qquad \textbf{(85)}$$

The secondary loop filter capacitor C_2 is set to less then a tenth of the main loop filter capacitor C_1.

$$C_2 < \frac{C_1}{10} = 6.22\,pF \Rightarrow C_2 = 6\,pF \qquad \textbf{(86)}$$

Now all of the system level loop design parameters have been computed. Table 7 summarizes the system level parameters.

Table 7 - Summary of Multi-Band PLL Frequency Synthesizer System Parameters

Loop Bandwidth	$w_{3dB} = 1.47\,Mrad/s$
Damping Factor	$\zeta = 0.707$
Natural Frequency	$w_n = 714\,krad/s$
VCO Tuning Range	100 – 300MHz
VCO Conversion Gain	$K_{VCO} = 255\,Mrad/sV$
Loop Division Ratio	$N = 32$
Charge Pump Current	$I = 25mA$
Primary Loop Filter Capacitor	$C_1 = 62.2\,pF$
Loop Filter Resistor	$R = 31.8k\Omega$
Secondary Loop Filter Capacitor	$C_2 = 6\,pF$

Mathematical Model

The PLL is a highly non-linear system. However, the PLL can be described with a linear model if the loop is operating in the lock range. The design parameters' effects on the loop performance are analyzed with a mathematical macromodel generated in MATLAB. This mathematical model assumes the PLL is operating only in the lock range. The mathematical model is not valid for other regions of operation because of the non-linearity of the PLL. An illustration of the macromodel is given in Figure 54.

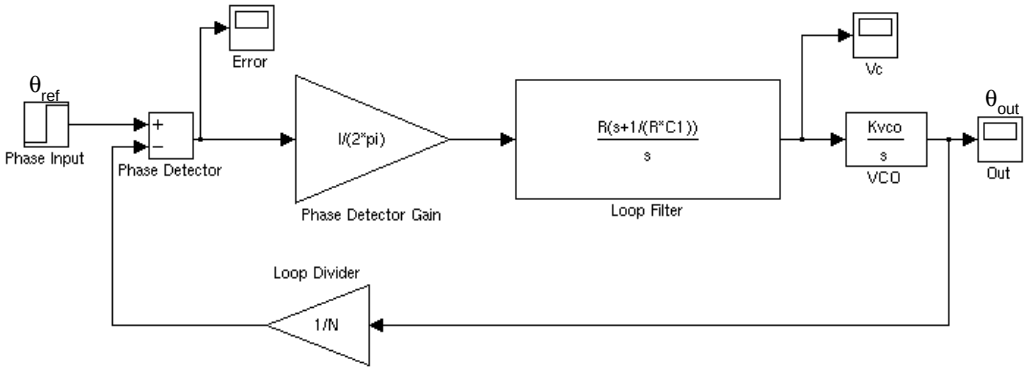

Figure 54 - Mathematical Macromodel of the Multi-Band PLL in the Lock Range

The loop bandwidth is verified with this macromodel as shown in Figure 55.

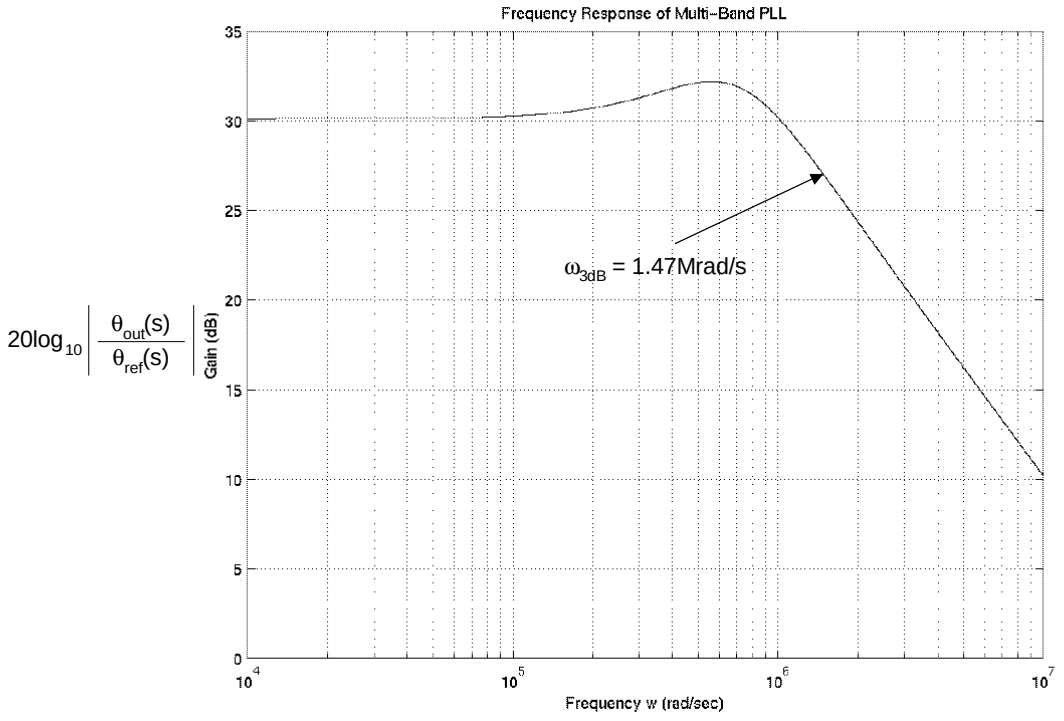

Figure 55 - Frequency Response of the Multi-Band PLL

This wide PLL bandwidth is beneficial to the noise performance of the PLL. The dominant source of noise in integrated PLLs is the VCO. The VCO noise transfer function has a high pass shape. If the loop bandwidth of the PLL is made sufficiently high, the VCO noise contribution can be minimized. The VCO noise transfer function of the multi-band PLL is shown in Figure 56 using the mathematical macromodel.

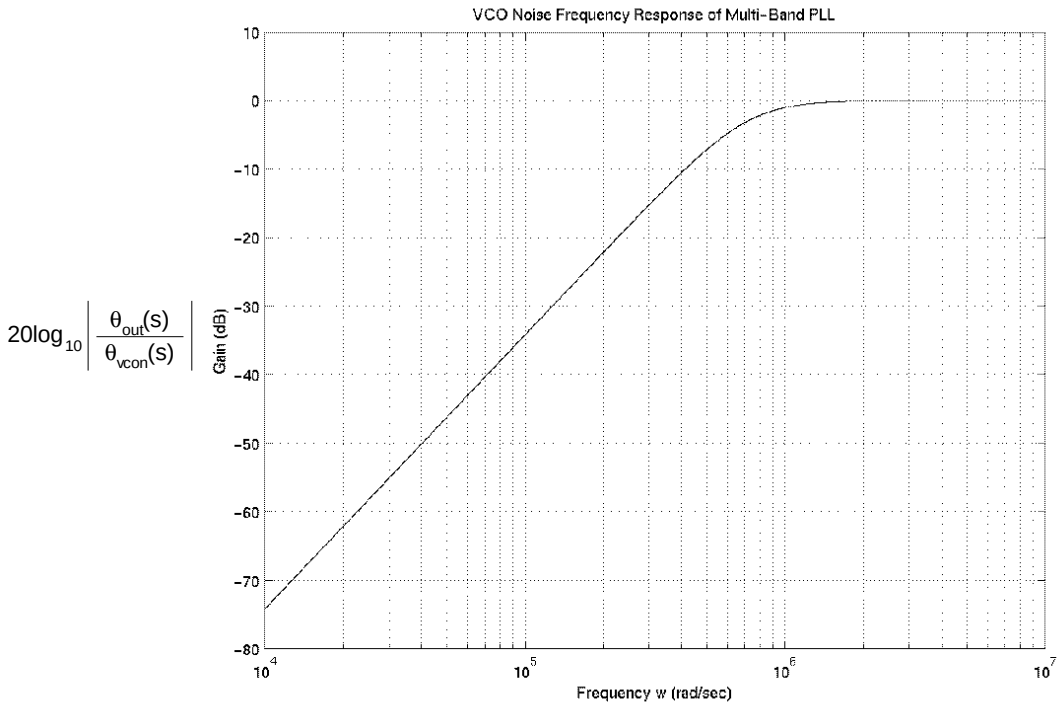

Figure 56 - VCO Phase Noise Frequency Response of the Multi-Band PLL

Another important performance parameter that can be investigated with the mathematical macromodel is the lock-in time. This is the time it takes the PLL to acquire lock assuming it is in the lock range. The lock-in time is shown in Figure 57 as the time it takes the PLL's VCO control voltage to settle within 1% of the final value when a frequency step is input into the system.

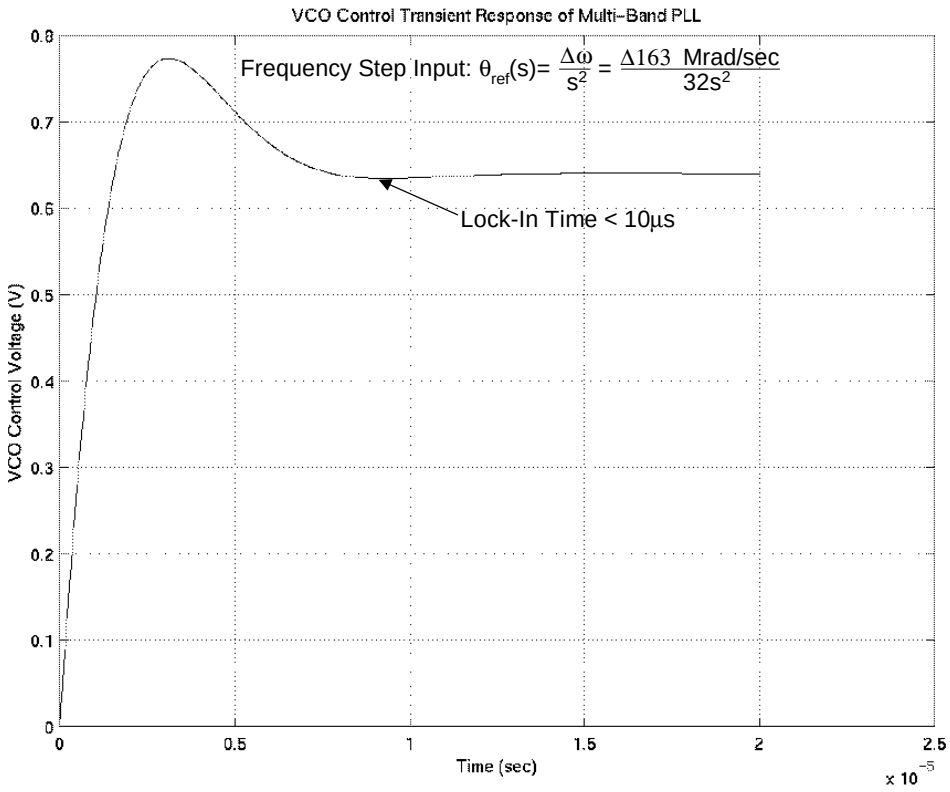

Figure 57 - VCO Control Response to a Frequency Step Showing the Lock-In Time

Behavioral Model

A time-domain behavioral model of the multi-band PLL frequency synthesizer was created to gain an increased understanding of the loop dynamics. This model was realized using Spectre and SpectreHDL. SpectreHDL is a C like programming language that can be used to program behavioral modules of analog or digital circuits. SpectreHDL can also be interfaced with normal Spice or Spectre circuit netlists. This allows for a simulation to mix behavioral code and circuit netlists.

Behavioral modules of all the loop blocks were produced and joined together to make up the behavioral system macromodel. These modules were either SpectreHDL code or

ideal Spectre circuit components. The ideal Spectre components consist of elements such as ideal current and voltage sources, switches, resistors, and capacitors.

The initial behavioral model of the PLL is of a classical charge pump PLL. The model of the phase/frequency detector, VCO, and loop divider consists of behavioral code. The charge pump is modeled as ideal current sources and ideal switches that are controlled by the PFD. The loop filter is modeled as an ideal resistor and two capacitors. The switch control logic for the switched tunable VCO is added as behavioral code to the initial PLL behavioral model to complete the multi-band PLL frequency synthesizer behavioral model. Appendix A shows the actual SpectreHDL code.

This behavioral time-domain model is different then the frequency-domain model produced in MATLAB. Time domain simulations are made with the behavioral model that realistically model the PLL in all regions of operation. This is different from the mathematical model that only simulates the linear model of the PLL in the lock range. The other regions of PLL operation are not visible in the mathematical model because of the non-linearity of the actual PLL system. Events such as cycle slipping that occur when the PLL is undergoing a pull-in process are not visible with the mathematical model. An example of the behavioral model working in the non-lock range is given in Figure 58 and compared to the linear mathematical model response to the same input in Figure 59. Notice specifically the way the VCO control voltage rises to its final value.

These two simulation results show the important differences between the behavioral and linear model. The behavioral model is able to model the PLL in all regions of operation. This is verified by noticing the cycle slips visible in the pull-in process of Figure 58. The same input is applied to the linear model. However, the linear model cannot model this pull-in process because it only models the lock range correctly. There are no cycle slips observed in Figure 59. Also, the behavioral model is an actual discrete time system like the real PLL. This can be seen in the behavioral simulations by the ripple on the

VCO control voltage that comes from the interaction between the charge pump and loop filter. No ripple is observed in the linear model because a continuous time system is assumed. The ripple on the control voltage is an important property that needs to be modeled when considering the design of the channels for the multi-band PLL frequency synthesizer because it adds to the minimum frequency overlap necessary to insure a stable system.

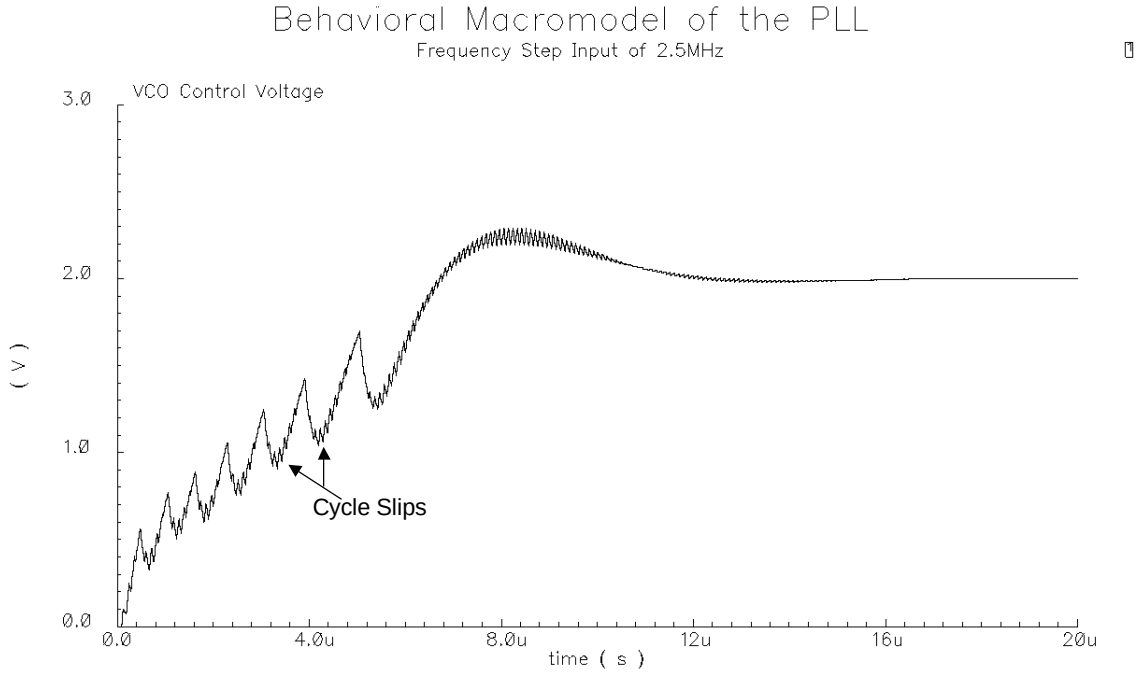

Figure 58 - Behavioral Macromodel of the PLL - Pull-In Process

The behavioral macromodel is extremely useful because many of the circuit simulations can be made without having to do the transistor level design. This allows new ideas to be added to the conventional loop structure with minimal design effort. The behavioral macromodel is very useful in modeling the switched tuning oscillator and the switch control network.

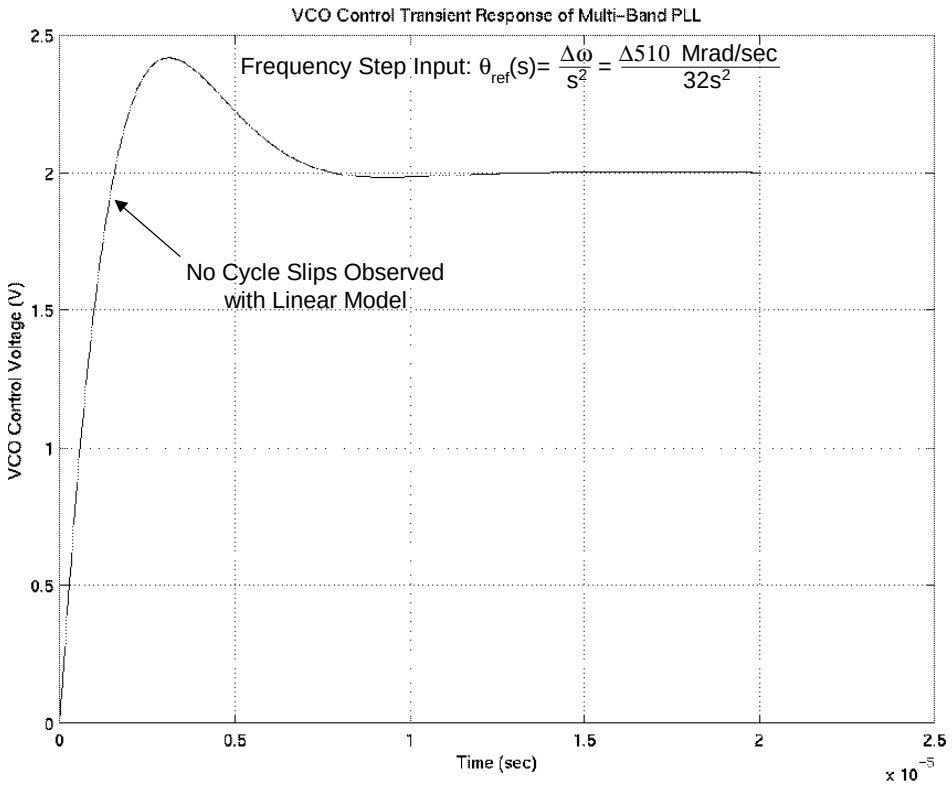

Figure 59 - Linear PLL Model - Pull-In Process (No Cycle Slips)

This switch control mechanism was added to the behavioral macromodel. Figure 60 displays the simulation results with the switch control mechanism added to the behavioral macromodel. This simulation is showing the multi-band PLL acquiring lock to synthesize a 222.5MHz signal. Initially the PLL is synthesizing a 132.5MHz signal. This is the mid-band signal of the first band. The input reference signal is approximately 4.14MHz. The input reference frequency has a frequency step to approximately 6.95MHz at time zero in order to generate 222.5MHz at the output. The acquisition process of the PLL then takes place. The VCO control voltage rises and crosses the positive voltage threshold of 0.8V. The oscillator is then changed to the next higher frequency channel. The VCO control voltage is then grounded to set it oscillating in the mid-band of the second channel. Now the output signal is approximately 177.5MHz.

The VCO control voltage rises again and crosses the positive threshold of 0.8V. The oscillator is then changed to the third channel. The VCO control voltage is then grounded to set it oscillating in the mid-band of the third channel. Now the output signal is approximately 222.5MHz. This is the correct frequency. However, there is still a phase error present in the PLL system. The PLL undergoes some settling to force this phase error to zero and the control voltage locks to synthesize the 222.5MHz signal.

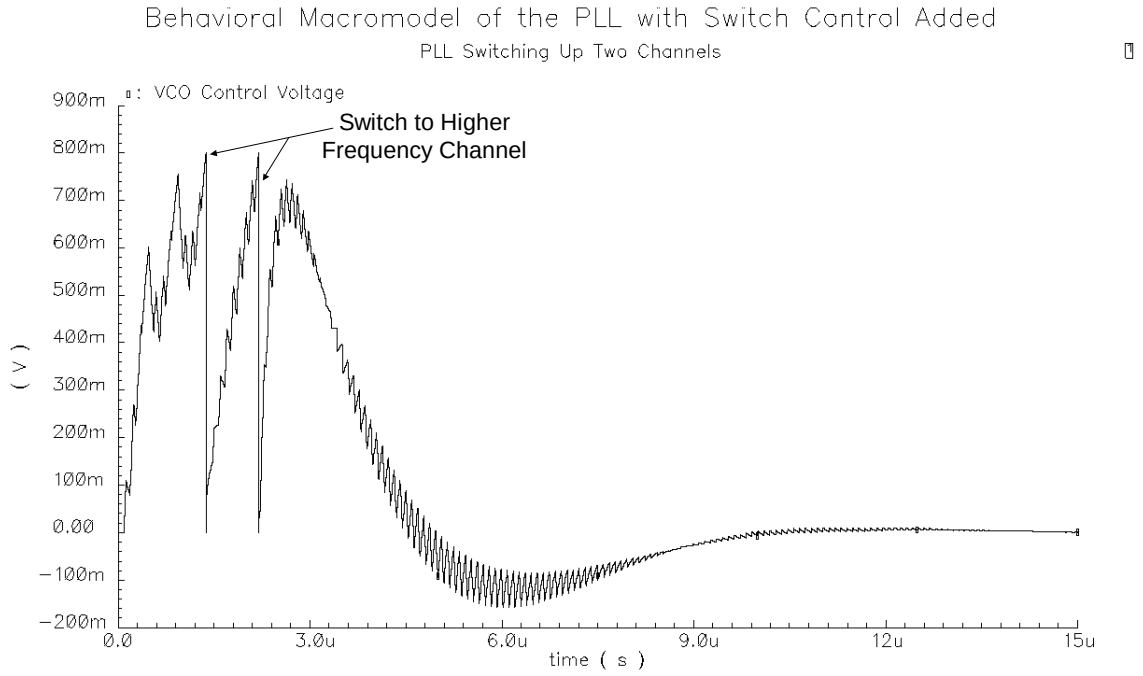

Figure 60 - Behavioral PLL Macromodel with Switch Control Circuitry

Another key advantage to using a behavioral macromodel such as the one discussed is the ability to interface transistor level design with behavioral code. The behavioral macromodel is considered an ideal system. The transistor level blocks will introduce non-idealities into the system. The ability to interface transistor level blocks with an ideal system is very important because it allows one to see the direct effects of that specific block's non-idealities on the loop performance. Design changes can be made

rapidly with the behavioral macromodel to account for the non-idealities of the transistor level blocks.

Transistor Level Block Design

The multi-band PLL frequency synthesizer system is designed using the AMI1.2µ CMOS process through the MOSIS foundry. This is an nwell process. It has double metal and double poly layers. The threshold voltage and transconductance technology parameters are given for this process in Table 8.

Table 8 - AMI1.2µ CMOS Process Technology Parameters

Transistor	V_{T0}	KP
NMOS	0.7194V	69.559µA/V^2
PMOS	-0.8165	21.500µA/V^2

Phase/Frequency Detector

The PFD circuit used is basically the same as the one presented in the previous section, with only a few modifications. The most important modification is that the VCO feedback signal, v_{fb}, is driving the *UP* signal, while the input reference signal, v_{ref}, drives the *DOWN* signal. This connection is reversed in the one presented in the previous section. The reason for this modification is that the designed VCO has a negative conversion gain. To cancel this negative conversion gain the connections are flipped into the PFD as shown in Figure 61.

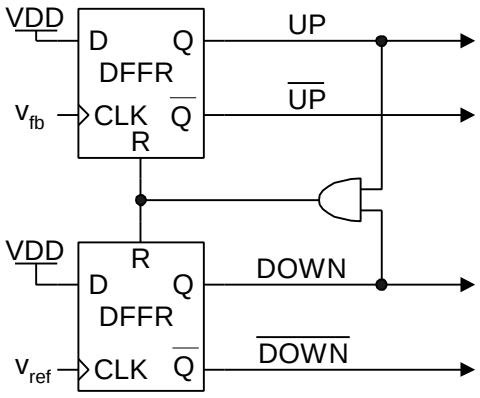

Figure 61 - Multi-Band PLL Phase/Frequency Detector Circuit

The D Flip-Flops used are optimized specifically for operation in the PFD[11]. The schematic is given in Figure 62. The flip-flops are designed with a small number of devices in the signal path to increase speed. The flip-flop has no *D* input because it is designed specifically for a PFD application where the *D* input is always high. The flip-flop's *Q* output goes high on a rising *CLK* edge as long as the *R* input is low. The *Q* output stays high until it is forced low by the *R* signal going high. The *Q* output will remain low as long as the *R* input is high. The *Q* output returns high on the next rising edge of the *CLK* after the *R* input returns low.

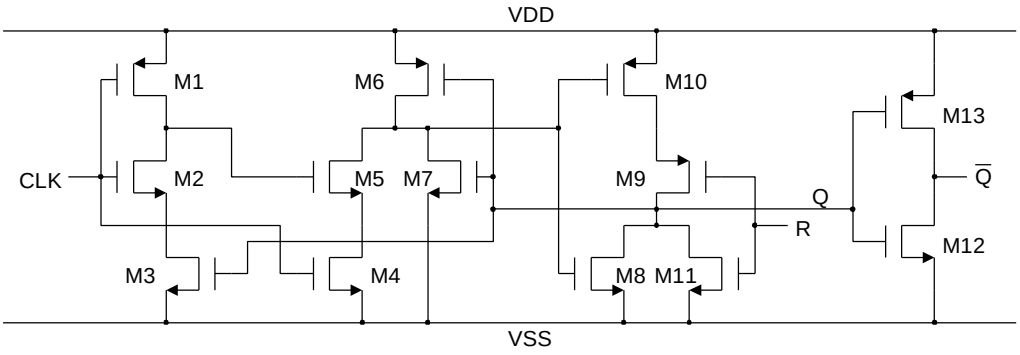

Figure 62 - PFD D Flip-Flop Schematic

The schematic of the AND gate is shown in Figure 63.

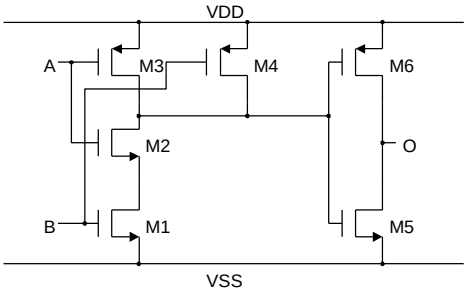

Figure 63 - PFD AND Gate

PFD Design Procedure and Simulation Results

The PFD D flip-flop design flow diagram is shown in Figure 64. This circuit is designed to operate between 1-15MHz to insure that it will operate correctly in the 100-300MHz PLL system.

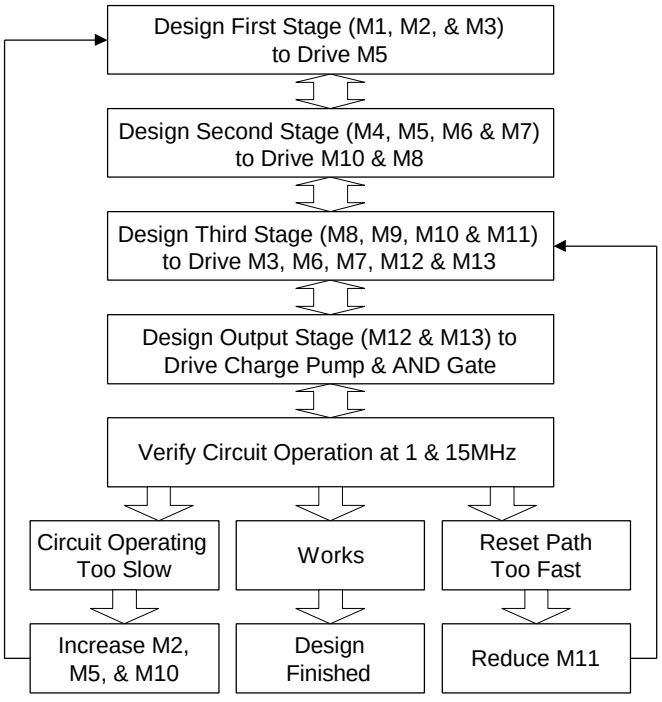

Figure 64 - PFD D Flip-Flop Design Flow Diagram

The first stage consists of transistors M1, M2, and M3. It is designed to drive M5. This first stage only has to drive one transistor gate. Therefore M1, M2, and M3 are made the practical minimum size.

$$\left(\frac{W}{L}\right)_{1,2,3} = \frac{2.4m}{1.2m} \qquad \textbf{(87)}$$

The second stage consists of transistors M4, M5, M6 and M7. It is designed to drive M10 and M8. M4 and M5 are made twice the practical minimum size because they are in series. M6 and M7 are made the practical minimum size.

$$\left(\frac{W}{L}\right)_{4,5} = \frac{4.8m}{1.2m}, \quad \left(\frac{\mathrm{W}}{\mathrm{L}}\right)_{6,7} = \frac{2.4m}{1.2m} \qquad \textbf{(88)}$$

The third stage consists of transistors M8, M9, M10, and M11. It is designed to drive M3, M6, M7, M12, M13, the AND gate, and the charge pump switches. M8 and M10 act as the Q signal path inverter. M9 and M11 operate as the reset inverter. The M8 and M10 inverter is designed for symmetric output drive[48]. This involves matching the effective pull-up resistance of M10 in series with the reset switch M9 to the pull-down resistance of M8. The resistance of the transistors is proportional to the following:

$$R_{N,P} \propto \frac{L_{N,P}}{W_{N,P} KP_{N,P}} \qquad \textbf{(89)}$$

Transistor M9 is set equal to twice the practical minimum length in order to lower its on resistance. Setting R_8 and R_{10} equal yields the following relation between the aspect ratios of M8 and M10.

$$\left(\frac{W}{L}\right)_{10} = \frac{KP_N}{KP_P}\left(\frac{W}{L}\right)_8 = \frac{69.559mA/V^2}{21.5mA/V^2}\left(\frac{W}{L}\right)_8 = 3.24\left(\frac{W}{L}\right)_8 \qquad \textbf{(90)}$$

This ratio is increased to 4 to compensate for the on resistance of M9. Transistor M11 is sized to pull the output of the third stage low when the reset signal goes high.

$$\left(\frac{W}{L}\right)_8 = \frac{2.4m}{1.2m}, \quad \left(\frac{W}{L}\right)_9 = \frac{4.8m}{1.2m}$$
$$\left(\frac{W}{L}\right)_{10} = \frac{9.6m}{1.2m}, \quad \left(\frac{W}{L}\right)_{11} = \frac{12m}{1.2m} \qquad \textbf{(91)}$$

The output inverter stage consists of M12 and M13. It is optimized to switch on the logic levels of the third stage and to drive the charge pump switches.

$$\left(\frac{W}{L}\right)_{12} = \frac{4.8m}{1.2m}, \quad \left(\frac{W}{L}\right)_{13} = \frac{7.2m}{1.2m} \qquad \textbf{(92)}$$

Table 9 summarizes the sizes of the transistors used in the PFD D Flip-Flop.

Table 9 - PFD D Flip-Flop Size Ratios

$(W/L)_{1,2,3,6,7,8}$	$(W/L)_{4,5,9,12}$	$(W/L)_{10}$	$(W/L)_{11}$	$(W/L)_{13}$
2.4µ/1.2µ	4.8µ/1.2µ	9.6µ/1.2µ	12µ/1.2µ	7.2µ/1.2µ

This circuit can fail at high frequencies due to delays in the signal path. Increasing the drive strength of the transistors in the signal path can alleviate this problem. This is accomplished by increasing the aspect ratio of M2, M5, and M10. It is preferable to increase the dimensions in an order from M2 to M5 to M10 so that the input stages are not overloaded.

This circuit can fail at low frequencies due to the reset path being too fast. This could result in the circuit not resetting properly. This also contributes to the PFD dead zone that increases the phase noise or jitter in the output signal as discussed in the previous section. Reducing the aspect ratio of M11 can alleviate this problem. This increases the reset time.

The AND gate consists of a four transistor NAND input stage and an inverter output. The AND gate is designed for symmetric output drive. The inverter output stage is sized the same as M12 and M13 of the D Flip Flop. The input NAND stage can be viewed as 2 PMOS switched in parallel and 2 NMOS switches in series. Setting the pull-up resistance equal to the pull-down resistance yields the following relationship between the input PMOS and NMOS transistors.

$$\left(\frac{W}{L}\right)_P = \frac{KP_N}{4KP_P} = \frac{69.559mA/V^2}{4\left(21.5mA/V^2\right)}\left(\frac{W}{L}\right)_N = 0.81\left(\frac{W}{L}\right)_N \qquad \textbf{(93)}$$

This relationship is rounded to set all the PMOS input transistors equal to the NMOS input transistors. Table 10 summarizes the sizes of the transistors used in the PFD AND gate.

Table 10 - PFD AND Gate Size Ratios

$(W/L)_{1,2,3,4,5}$	$(W/L)_6$
2.4µ/1.2µ	7.2µ/1.2µ

Some simulation results of the PFD are shown in Figure 65. Referring back to Figure 61, there is a 9.375MHz v_{ref} signal and a 6.25MHz v_{fb} signal in this simulation. The v_{ref} signal corresponds to the input reference frequency of the PLL. The v_{fb} signal corresponds to the frequency divided VCO feedback signal. A rising edge on the v_{ref} signal causes the *DOWN* signal to go high first. The *DOWN* signal stays high until a rising edge of v_{fb} causes *UP* to go high. *UP* and *DOWN* are now both high for a short period. This causes the AND gate reset output to go high and force *UP* and *DOWN* low. This cycle is repeated with another rising edge of v_{ref}. The overall effect of this is that with a significantly faster v_{ref} signal the *DOWN* signal is high for a significant period of time. This will force the charge pump to discharge the loop filter and the VCO

control voltage will drop. This will increase the VCO output's frequency and in turn the v_{fb} signal's frequency.

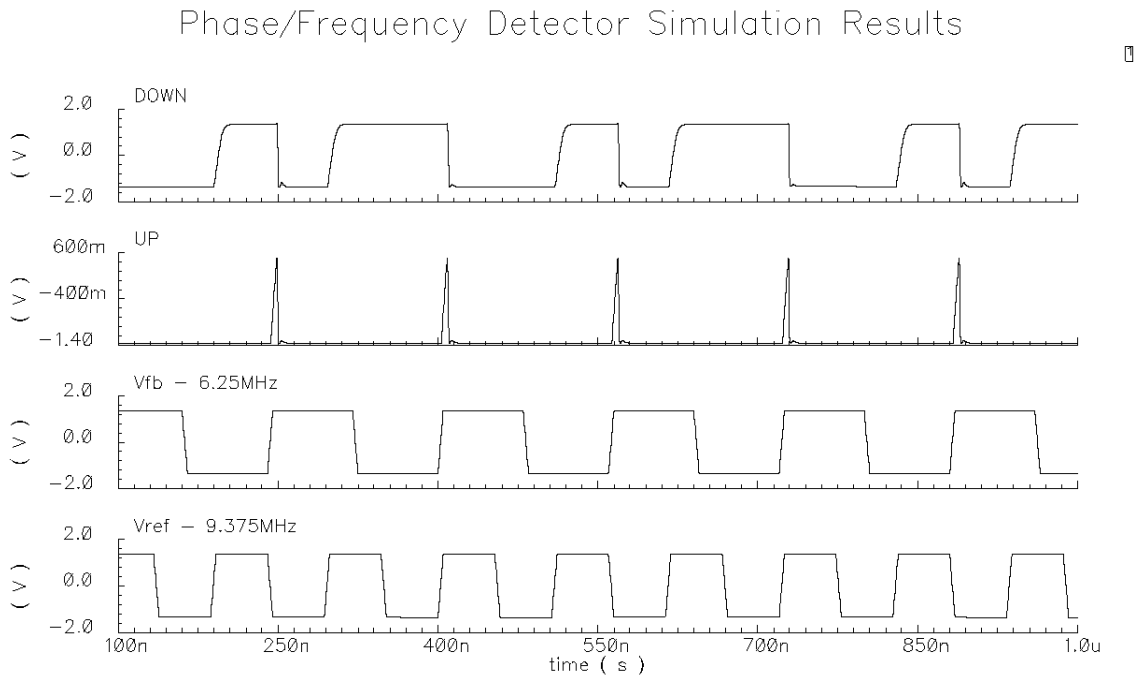

Figure 65 - Phase/Frequency Detector Simulation Results

Charge Pump

The charge pump designed in this system is shown in Figure 66. The circuit consists of a PMOS current mirror (M5 and M6) to mirror I_{UP} into the charge pump. This I_{UP} current either goes into the loop filter or into the ground node depending on the position of the two PMOS switches (M1 and M2). An NMOS current mirror (M7 and M8) is used to mirror I_{DOWN} into the charge pump. This I_{DOWN} current either discharges the loop filter or pulls current from the ground node depending on the position of the two NMOS switches (M3 and M4).

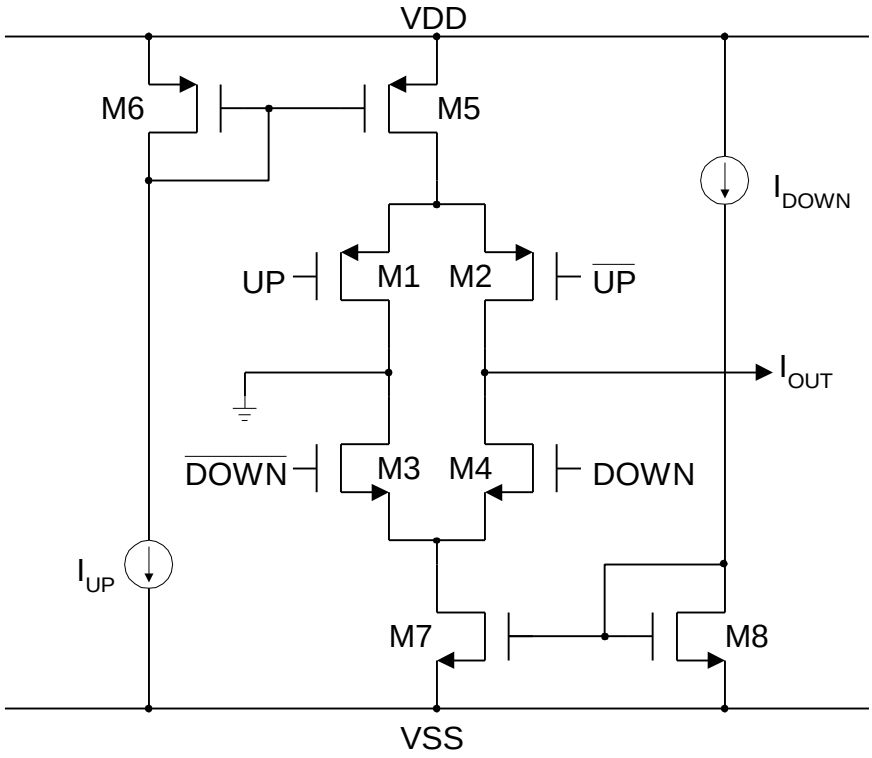

Figure 66 - Charge Pump Schematic

I_{UP} and I_{DOWN} are both set equal to insure a constant phase detector gain. These currents are set to the following value.

$$I_{UP} = I_{DOWN} = 25mA \quad \textbf{(94)}$$

The charge pump must satisfy a certain voltage compliance to generate a relatively constant output current over the output range of the VCO control voltage. The VCO has a tuning range of 1.6V with a 2.7V supply. This implies the following compliance voltage.

$$\text{Charge Pump Voltage Compliance} = 550\text{mV From Each Rail} \quad \textbf{(95)}$$

Charge Pump Design Procedure and Simulation Results

The design procedure for the charge pump is presented. The charge pump sources or sinks 25µA of current over an output voltage range of ±0.8V.

1. Set the proper V_{DSAT} values for transistors M5 and M7 to satisfy the voltage compliance range. The V_{DSAT} for M5 and M7 is set to 0.3V to insure that they do not go out of saturation when the output node swings from ±0.8V. This V_{DSAT} value also allows for a possible 0.25V drop across the switch transistors M1-4. A V_{DSAT} value of 0.3V results in the following minimum sizes for M5, M6, M7, and M8.

$$\left(\frac{W}{L}\right)_{5,6} > \frac{2I_D}{KP_P V_{DSAT}^2} = \frac{2(25mA)}{(21.5mA/V^2)(0.3V)^2} = 25.8$$
$$\left(\frac{W}{L}\right)_{7,8} > \frac{2I_D}{KP_N V_{DSAT}^2} = \frac{2(25mA)}{(69.559mA/V^2)(0.3V)^2} = 7.99 \qquad \textbf{(96)}$$

2. Size the switch transistors M1-4 to insure that the voltage drop across the switches does not exceed 0.25V. In order to meet this requirement a value of 0.15V is used for the calculation. This results in the following minimum sizes for M1-4.

$$\left(\frac{W}{L}\right)_{1,2,3,4} > \frac{I_D}{KP(|V_{GS}| - |V_{TO}|)|V_{DS}|}$$
$$\left(\frac{W}{L}\right)_{1,2} > \frac{25mA}{(21.5mA/V^2)(2.25V - .8165V)(0.15V)} = 5.41 \qquad \textbf{(97)}$$
$$\left(\frac{W}{L}\right)_{3,4} > \frac{25mA}{(69.559mA/V^2)(2.25V - .7194V)(0.15V)} = 1.57$$

The transistor sizes were optimized through computer simulation in Spectre. The final sizes are given in Table 11.

Table 11 - Charge Pump Size Ratios

$(W/L)_{1,2}$	$(W/L)_{3,4}$	$(W/L)_{5.6}$	$(W/L)_{7,8}$
6.6µ/1.2µ	3µ/1.2µ	55.2µ/1.8µ	51.6µ/2.4µ

Some simulation results of the charge pump are shown in Figure 67. In this simulation the *UP* and *DOWN* signals are ±1.35V 200Hz square waves. *UP* and *DOWN* are logic complements. A 10nF capacitor loads the output of the charge pump. The charge

pump positively charges the load capacitor with I_{UP} when UP is high and negatively charges the load capacitor with I_{DOWN} when $DOWN$ is high. The output current will vary slightly with the output voltage level due to channel length modulation effects. The average output current is measured from the voltage slope over the ±0.8V region of interest for the multi-band PLL system. When UP is high the charge pump sources 24.0µA of current into the loop filter. The charge pump sinks –25.0µA of current from the loop filter when $DOWN$ is high.

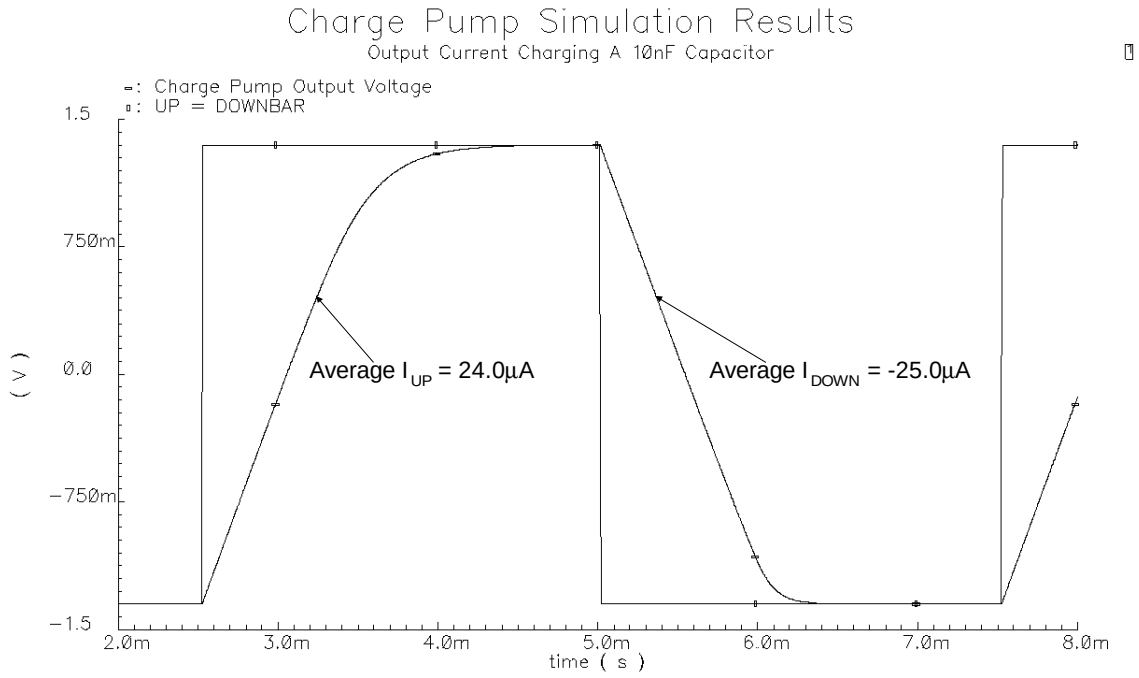

Figure 67 - Charge Pump Simulation Results

Loop Filter

The loop filter is fully integrated on chip by using poly2 – poly1 capacitors and a poly1 resistor as shown in Figure 68. The key issue here is the silicon area associated with the filter components.

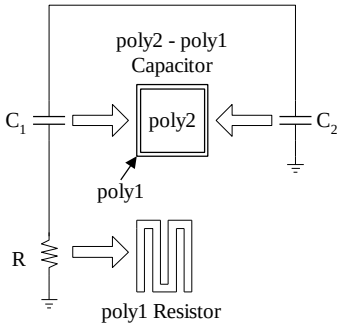

Figure 68 - Fully Integrated Loop Filter

The capacitance per area parameter for poly2 – poly1 capacitors is 611aF/μm^2. This yields the following area for the two capacitors.

$$C_1 \text{ Area} = \frac{62.2\,pF}{611\,aF/mm^2} = 101.8\times10^3\,mm^2 \Rightarrow 320mm\times320mm$$
$$C_2 \text{ Area} = \frac{6\,pF}{611\,aF/mm^2} = 9.82\times10^3\,mm^2 \Rightarrow 100mm\times100mm \quad \textbf{(98)}$$

A picture of the loop filter capacitors is shown in Figure 69.

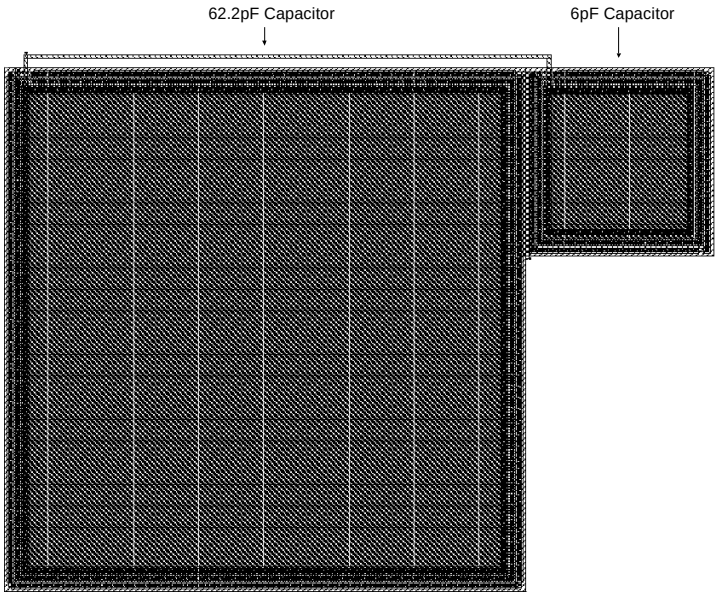

Figure 69 - Loop Filter Capacitors

The poly1 resistor also occupies significant area. However, the resistor area is not on the same scale as the capacitor area. The sheet resistance for poly1 is 29 ohms/square and the poly1 contact resistance is 36.2 ohms. The resistor required for the loop filter is 31.8kO. Placing several contacts in parallel at both ends of the resistor allows the contact resistance to be effectively neglected in computing the number of squares. Neglecting the contact resistance results in the following number of squares for the resistor.

$$\#\,\text{squares} = \frac{31.8k\Omega}{29\,ohms/square} = 1097\ \text{squares} \qquad \textbf{(99)}$$

This results in a resistor of 1316µm long using minimum poly1 width of 1.2µm. A picture of the loop filter resistor is shown in Figure 70.

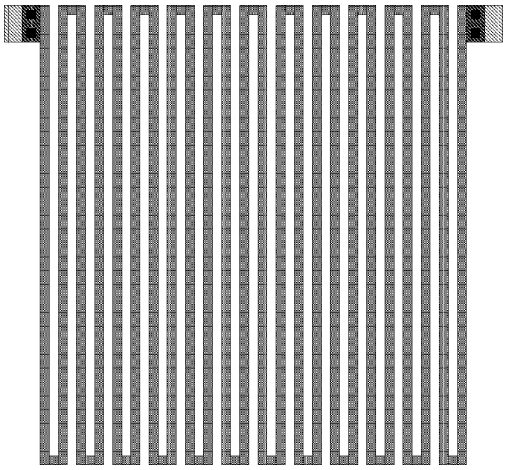

Figure 70 - Loop Filter 31.8kO Resistor Layout

The frequency response of the layout extracted loop filter is shown in Figure 71. The filter has a pole at zero and a zero at approximately 80.5kHz. The capacitor C_2 in the loop filter causes the high frequency second pole.

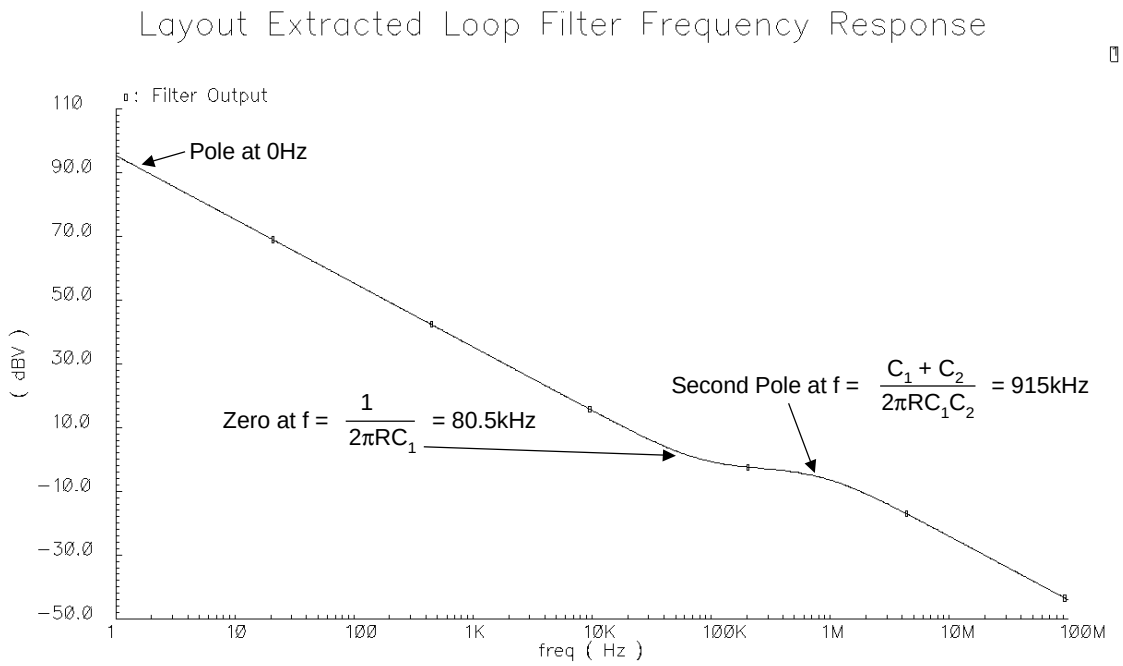

Figure 71 - Layout Extracted Frequency Response

Switched Tuning VCO

The switched tuning VCO designed in this system is shown in Figure 72. The VCO is a three-stage ring VCO. The inverter stages are loaded with one continuously tuned capacitor, C_C, and three discretely tuned capacitors, C_{D1-3}.

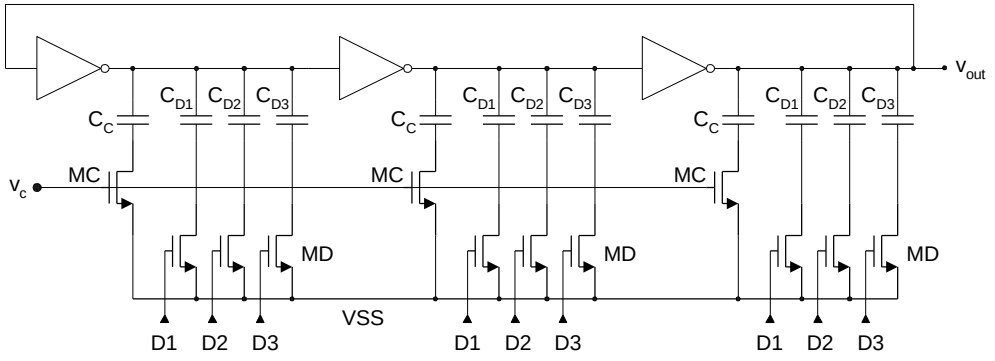

Figure 72 - Switched Tuning VCO

The VCO inverter stages consist of single-ended CMOS inverters shown in Figure 73.

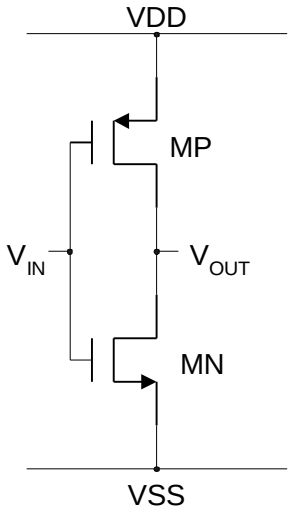

Figure 73 - CMOS Inverter Delay Cell

The model shown in Figure 74 can be used to analyze the ring oscillator. The output capacitors are lumped into one output capacitance C_O.

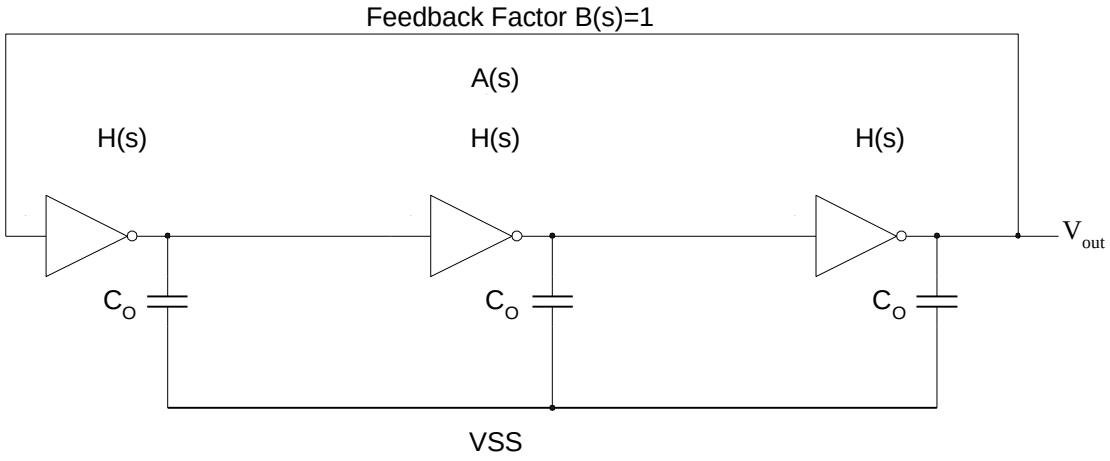

Figure 74 - Ring Oscillator Model

The individual inverter stages have the following transfer function.

$$H(s) = -\frac{gm_P + gm_N}{go_P + go_N + sC_O} = -\frac{K}{1+sT}$$
$$K = \frac{gm_P + gm_N}{go_P + go_N}, \quad T = \frac{C_O}{go_P + go_N} \qquad \textbf{(100)}$$

Here K is the DC gain and T is the inverse of the 3-dB bandwidth. This results in the following open loop transfer function $A(s)$.

$$A(s) = [H(s)]^3 \qquad \textbf{(101)}$$

The oscillator's closed loop transfer function is the following:

$$\text{Closed Loop Transfer Function} = \frac{A(s)}{1 - A(s)B(s)} = \frac{A(s)}{1 - A(s)} \qquad \textbf{(102)}$$

The Barkhausen criteria for constant amplitude oscillation is the following[49].

1. The phase of the loop gain should be zero at the frequency of oscillation.
2. The magnitude of the loop gain should be unity at the frequency of oscillation.

The loop gain must be equal to the following in order for the circuit to oscillate.

$$A(s)\big|_{w_{osc}} = 1 \qquad \textbf{(103)}$$

This implies the following for the individual stages.

$$A(s)\big|_{w_{osc}} = [H(s)]^3\big|_{w_{osc}} = -\frac{K^3}{(1+sT)^3}\bigg|_{w_{osc}} = 1 \qquad \textbf{(104)}$$

The following equality can be solved for K and T.

$$(1 + jw_{osc}T)^3 + K^3 = 0$$
$$3w_{osc}^2T^2 - K^3 = 1, \quad w_{osc}^2T^2 = 3w_{osc}T \qquad \textbf{(105)}$$
$$K = 2, \quad T = \frac{\sqrt{3}}{w_{osc}} \Rightarrow w_{osc} = \frac{\sqrt{3}}{T}$$

The frequency of oscillation is the square root of three times the inverter stage's 3-dB bandwidth. Notice also that this implies that the inverter's DC gain must be exactly two for constant amplitude oscillation. However, this exact value cannot be designed for. Therefore, the inverters should be designed for a gain greater than two and the amplitude will be controlled by a limiter. In this case the power supplies are the limiter. The following equations can be used to achieve a desired frequency of oscillation.

$$w_{osc} = \frac{\sqrt{3}}{T} = \frac{\sqrt{3}(go_P + go_N)}{C_O} \qquad \textbf{(106)}$$

$$K = \frac{gm_P + gm_N}{go_P + go_N} \geq 2 \qquad \textbf{(107)}$$

The previous analysis assumes small-signal operation of the transistors. The oscillator is actually a large signal oscillator because the output signal swings rail-to-rail. This large signal operation allows the oscillator to be analyzed using propagation delays.

The VCO output signal propagates through the ring oscillator each half period with an inversion. If the output of the third stage is low, the signal will propagate through the three inverters before the output of the third stage goes high. Each inverter has a propagation delay t_p. The time it takes for the output signal to go high is equal to the sum of the propagation delays of the three inverter stages. This time is equal to one half period of oscillation, $\frac{T}{2}$, as shown in the following:

$$\frac{T}{2} = nt_p \qquad \textbf{(108)}$$

The VCO's angular frequency of oscillation, w_{osc}, is derived from (108) to be the following. Here n is the number of inverting stages.

$$w_{osc} = \frac{p}{nt_p} = \frac{p}{3t_p} \qquad \textbf{(109)}$$

The propagation delay is the average of the rise time, t_{pLH}, and the fall time, t_{pHL}, as shown in the following:

$$t_p \approx \frac{t_{pLH} + t_{pHL}}{2} \qquad \textbf{(110)}$$

The fall time, t_{pHL}, is mostly a function of the NMOS transistor in the inverter cell and the total output capacitance, C_O, as shown in the following[50].

$$t_{pHL} = \frac{C_O}{\left(\frac{W}{L}\right)_N KP_N \left(VDD - V_{TN}\right)} \left[\frac{2V_{TN}}{VDD - V_{TN}} + \ln\left(\frac{4\left(VDD - V_{TN}\right)}{VDD} - 1 \right) \right] \qquad \textbf{(111)}$$

The rise time, t_{pLH}, is mostly a function of the PMOS transistor in the inverter cell and the total output capacitance, C_O, as shown in the following[50].

$$t_{pLH} = \frac{C_O}{\left(\frac{W}{L}\right)_P KP_P \left(VDD - \left|V_{TP}\right|\right)} \left[\frac{2\left|V_{TP}\right|}{VDD - \left|V_{TP}\right|} + \ln\left(\frac{4\left(VDD - \left|V_{TP}\right|\right)}{VDD} - 1 \right) \right] \qquad \textbf{(112)}$$

Equations (106), (107), (111), and (112) can be used to design the inverter stages for a desired frequency response. These equations yield initial values that are optimized through simulations.

Changing the propagation delay of the inverter cells is used to tune the VCO's output frequency. It can be observed from the following equations that the propagation delay is proportional to the load capacitance C_O. This load capacitance is the summation of any loading capacitance, C_{TUNE}, intentionally placed at the output of the inverting cells and the parasitic capacitances associated with the output node of the inverting cell and the input node of the next inverting cell. The capacitors that make up C_O are given in the following equation where the subscript 1 indicates the inverting cell and the subscript 2 indicates the next inverting cell.

$$\begin{aligned} C_O &= C_{TUNE} + C_{gdN1} + C_{gdP1} + C_{dbN1} + C_{dbP1} + C_{gsN2} + C_{gsP2} \\ &+ C_{gbN2} + C_{gbP2} + C_{gdN2} + C_{gdP2} \approx C_{TUNE} + C_{gsN2} + C_{gsP2} \end{aligned} \qquad \textbf{(113)}$$

The output capacitance is simplified because the C_{gs} of the next inverter stage dominates the parasitic capacitance.

Changing the propagation delay, and in turn the frequency of oscillation, is achieved through capacitive tuning. Capacitive tuning loads the inverter stages with an RC network as shown in Figure 75.

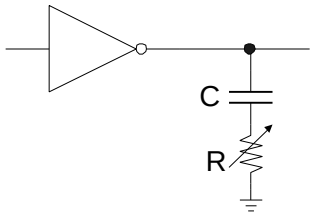

Figure 75 - Capacitive Tuning

The effective value of capacitance, C_{eff}, that the inverter sees at the output is equal to the following:

$$C_{eff} = \frac{C}{1 + sCR} \qquad \textbf{(114)}$$

This means that the effective capacitance is small for high values of R and the propagation delay will be relatively low. This makes sense because as R becomes large, the inverter simply sees an open circuit output with little capacitance. As R approaches zero, C_{eff} approaches C and the propagation delay will increase. This makes sense because if R is zero the inverter simply sees a capacitor shorted to ground.

Capacitive tuning is implemented in the switched tuning VCO with capacitors C_C and the NMOS active resistors MC. The capacitor C_C is the capacitor in (114) for the above oscillator analysis. This capacitor is the tuning capacitor and should be made as large as possible compared to the parasitic capacitances of the inverter transistors in order to have a wide tuning range. The active resistor's resistance is tuned with the

VCO controlling voltage v_c. The frequency bands of operation are changed by discretely switching in the capacitors C_D with the NMOS switches MD. Switching in the discrete capacitors increases the tuning range of the oscillator. However, the VCO gain, K_{VCO}, drops from the high frequency channel when there are no discrete capacitors to the low frequency channel when all the discrete channels are switched in because the value of the tuning capacitance is now a smaller percentage of the total capacitance.

Switched Tuning VCO Design Procedure and Simulation Results

The switched tuning VCO design flow diagram is shown in Figure 76. This circuit is designed to operate over a minimum frequency range of 100-300MHz.

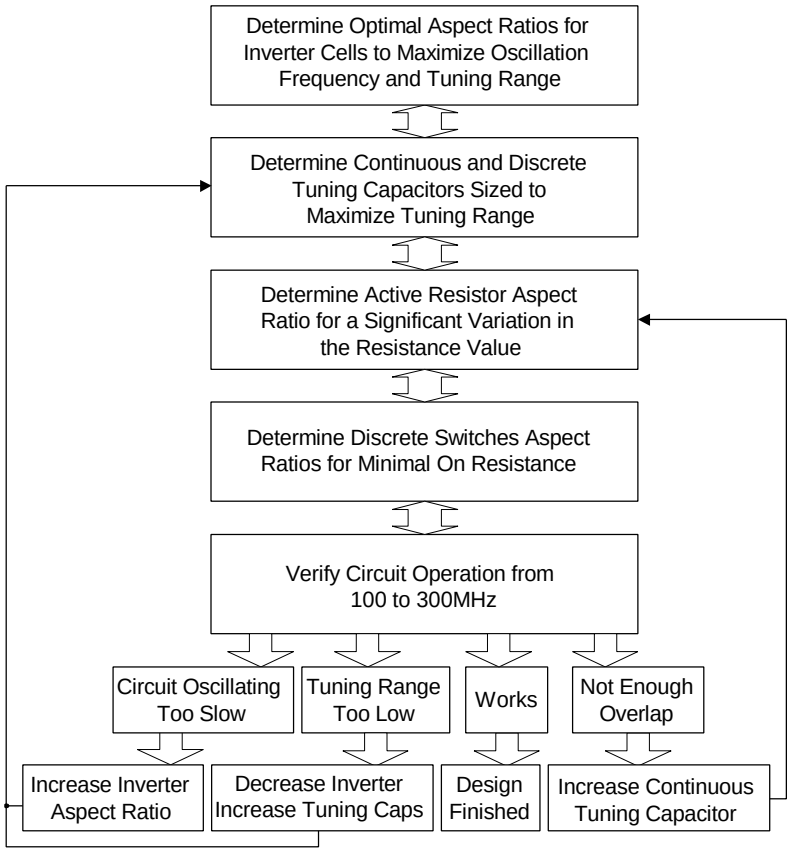

Figure 76 - Switched Tuning VCO Design Flow Diagram

The inverter aspect ratios are designed to yield a maximum oscillation frequency of 300MHz and a wide tuning range. Equations (106) and (113) are used to initially determine the inverter aspect ratios for 300MHz operation. At this maximum frequency C_{TUNE} is the minimum tuning capacitance. It is assumed to be 40fF. Equation (106) is simplified with (113) to yield the following.

$$w_{osc} = \frac{\sqrt{3}\left(go_P + go_N\right)}{C_O} = \frac{\frac{\sqrt{3}}{2}\left(l_N KP_N \left(\frac{W}{L}\right)_N \left(V_{GS} - V_{TN}\right)^2 + l_P KP_P \left(\frac{W}{L}\right)_P \left(\left|V_{GS}\right| - \left|V_{TP}\right|\right)^2 \right)}{\frac{2}{3} C_{ox}\left(W_N L_N + W_P L_P\right) + C_{TUNE}} \quad \textbf{(115)}$$

Minimum length transistors should be used in order to achieve maximum oscillation frequency with minimum area. This allows equation (115) to be simplified to the following.

$$w_{osc} = \frac{3\sqrt{3}\left(l_N KP_N W_N \left(V_{GS} - V_{TN}\right)^2 + l_P KP_P W_P \left(\left|V_{GS}\right| - \left|V_{TP}\right|\right)^2 \right)}{4C_{ox} L^2 \left(W_N + W_P\right) + LC_{TUNE}} \quad \textbf{(116)}$$

The minimum length l parameters were determined through computer simulation to be the following.

$$l_N = 0.111\text{V}^{-1}, \quad l_P = 0.300\text{V}^{-1} \quad \textbf{(117)}$$

The V_{GS} values are assumed to be 1.35V because of large signal operation. Substituting the technology parameters into equation (116) yields the following.

$$w_{osc} = \frac{16.0\times10^{-6} W_N + 9.55\times W_P}{6.05\times10^{-15}\left(W_N + W_P\right) + 48\times10^{-21}} \quad \textbf{(118)}$$

Increasing the transistor widths increases the oscillation frequency until the denominator width term becomes much larger than the lowest tunable capacitance term. However, increasing the transistors' widths will lower the tuning range because the parasitic

capacitance becomes comparable to the tuning capacitance even when the tuning capacitance is not minimal. Thus, changing the effective value of the tuning capacitance has less of an effect on the total inverter load capacitance. The PMOS transistor degrades the maximum frequency versus tuning range tradeoff because it only contributes 37.4% to the maximum frequency, while contributing 50% of the parasitic capacitance. The PMOS transistor width is set to be the following relation with the NMOS in order to allow the PMOS to contribute 50% to the maximum frequency.

$$W_P = \frac{16.0\times10^{-6}}{9.55\times10^{-6}} W_N = 1.68 W_N \qquad \textbf{(119)}$$

Substituting equation (119) into equation (118) and solving for 300MHz operation yields the following initial values for W_N and W_P.

$$\text{Initial } W_N = 61.8m, \quad \text{Initial } W_P = 103.8m \qquad \textbf{(120)}$$

These inverter aspect ratios must also satisfy the DC gain given in equation (107). Equation (107) can be simplified to yield the following.

$$K = \frac{gm_P + gm_N}{go_P + go_N} = \frac{2\left(\sqrt{KP_N W_N} + \sqrt{KP_P W_N}\right)}{\sqrt{KP_N W_N \left(V_{GS} - V_{TN}\right)^2}\left(l_N + l_P\right)} = 13.3 \geq 2 \qquad \textbf{(121)}$$

The circuit will oscillate because it has a gain greater than two. The initial values were optimized through simulation to yield the following aspect ratios.

$$\left(\frac{W}{L}\right)_N = \frac{60m}{1.2m}, \quad \left(\frac{W}{L}\right)_P = \frac{88.8m}{1.2m} \qquad \textbf{(122)}$$

The values of the tuning capacitors, C_C, are chosen to be large enough to be significantly greater than the parasitics, but not too big to significantly limit the maximum frequency of oscillation. The continuous tuning capacitors, C_C, are chosen larger than the discrete tuning capacitors, C_D in order to maximize the tuning range.

The following capacitor values are chosen to cover the frequency range from 100 – 300MHz.

$$C_C = 600\,fF, \qquad \mathrm{C_D} = 300\,fF \tag{123}$$

The active resistor's aspect ratio is determined to provide a significant variation in the resistance in order to vary the loading capacitance of the inverter cell. Making the $\left(\frac{W}{L}\right)_C$ of the active resistor MC greater increases the variation in the resistance and thus results in a larger tuning effect. However, a larger $\left(\frac{W}{L}\right)_C$ also produces more parasitic capacitance and lowers the maximum output frequency. This is because the C_{db} and C_{gd} of the active resistor add to the total capacitance the inverter stages have to charge. The aspect ratio of MC is chosen to provide a significant variation in the resistance and to not significantly limit the maximum frequency of oscillation. The resistance of the active resistor is approximated by the following formula.

$$R_{DS} = \frac{1}{KP_N\left(\frac{W}{L}\right)(V_{GS} - V_{TO})} \tag{124}$$

As the VCO control voltage varies from –0.8V to 0.8V the resistance varies from the GO range when the transistor is cut-off to approximately $10k\Omega(L/W)_C$. This $\left(\frac{W}{L}\right)_C$ can be increased to provide minimal resistance when v_c is equal to 0.8V. However, this increases C_{db} and C_{gd}. The aspect ratio is chosen to be the following to yield a minimum resistance of approximately 500O.

$$\left(\frac{W}{L}\right)_C = \frac{26.4m}{1.2m} \tag{125}$$

The other NMOS switches, MD, are designed such that their on resistance is minimal and that their parasitic capacitance is not significant. The parasitic capacitors C_{db} and C_{gd} reduce the maximum frequency of oscillation. Again, the resistance is approximated by equation (124). The transistor is on when the controlling voltage, $D1-D3$, is equal to 1.35V. This provides an on resistance of approximately $7.26k\Omega(L/W)_D$. This $\left(\frac{W}{L}\right)_D$ can be increased to provide minimal on resistance. However, this increases C_{db} and C_{gd}. The aspect ratio is chosen to be the following to yield an on resistance of approximately 500O.

$$\left(\frac{W}{L}\right)_D = \frac{16.8m}{1.2m} \qquad \textbf{(126)}$$

Table 12 summarizes the transistor sizes and capacitor values used in the switched tuning VCO design.

Table 12 - Switched Tuning VCO Transistor Sizes and Capacitor Values

$(W/L)_N$	$(W/L)_P$	$(W/L)_C$	$(W/L)_D$	C_C	C_D
60µ/1.2µ	88.8µ/1.2µ	26.4µ/1.2µ	16.8µ/1.2µ	600fF	300fF

The circuit oscillates too slow if the inverter propagation delay is too long. Increasing the aspect ratios of the inverter transistors reduces the inverter propagation delay because the delay is inversely proportional to the inverter transistor aspect ratios. Care should be taken not too increase the inverters too large as this increases the parasitic capacitance at the output node and thus reduces the tuning range.

The circuit's tuning range becomes low when the parasitic capacitance of the inverter transistors becomes comparable to the tuning capacitance. Reducing the inverter aspect

ratios increases the tuning range because it reduces the parasitic capacitance. However, the maximum frequency of oscillation is lowered due to a larger propagation delay. Increasing the tuning capacitor's size will increase the tuning range because the inverters will see a higher range of capacitance at the output node. This does not affect the maximum frequency too much because these capacitors are not seen when the active resistors are a large value.

The overlap between frequency bands becomes low when the parasitic and discrete capacitance becomes comparable in size to the continuous tuned capacitors C_C. The continuous tuned capacitors should be increased in order to increase the frequency overlap between frequency bands.

A near maximum buffered VCO output frequency is shown in Figure 77. The VCO oscillates at 340MHz when the continuous VCO control voltage, v_c, is at -0.8V and the three digital control signals, $D1 - D3$, are all low.

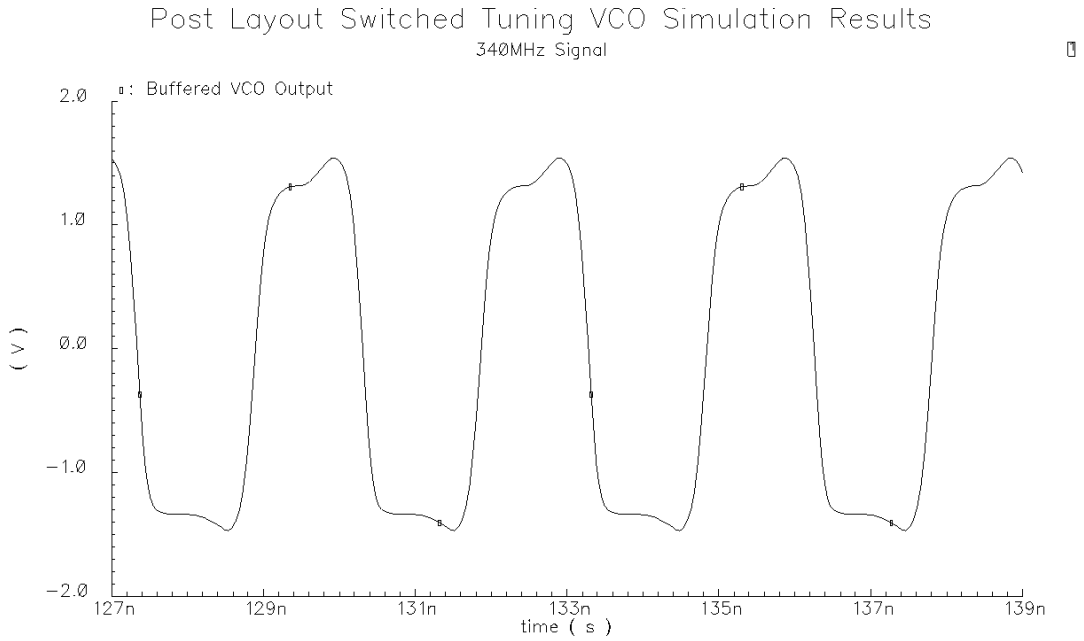

Figure 77 - Switched Tuning VCO Output Signal

The switched tuning VCO's frequency response and phase noise performance over the different bands of operation is given in Table 13. The transfer curves of the switched tuning VCO are shown in Figure 78. The frequency bands of the actual designed VCO are not as ideal as the ones in the design calculations. However, they do cover the entire frequency range with enough spectrum overlap to provide a stable system. The SpectreRF simulated phase noise values seem quite optimistic. While these phase noise absolute values may not be correct, it is assumed that the relative values are correct and design optimization was performed based on the changes in the phase noise values. The phase noise performance of the VCO is optimal at the edges of the bands where the VCO conversion gain is the lowest. The worst VCO phase noise performance occurs in the mid-band range where the VCO conversion gain is highest.

Table 13 - Switched Tuning VCO Frequency Response

Band	Description	Frequency Range (MHz)	Phase Noise @ 50kHz Offset (dBc/Hz)
1	All Switches Closed	99.8 – 146.8	-91.77 ? -103.7
2	2 Switches Closed	121.1 – 185.2	-89.32 ? -102
3	1 Switch Closed	148.2 – 246.5	-86.01 ? -99.75
4	All Switches Open	191.4 – 341.8	-82.63 ? -96.67

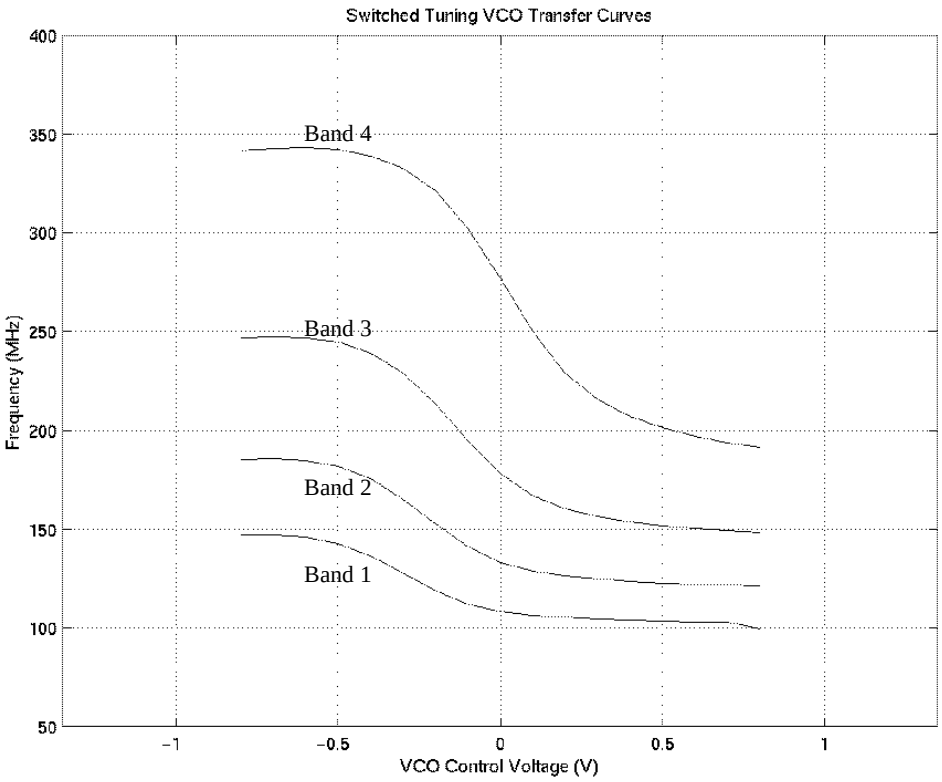

Figure 78 - Switched Tuning VCO Transfer Curves

VCO Switch Control System

The VCO switch control system is shown in Figure 79. The switch control network detects when the VCO control voltage crosses a positive threshold, *VREFP* , or negative threshold, *VREFN* , and changes the VCO channel by switching in or out different tuning loads. The VCO control voltage is then grounded to set the VCO in the middle of the next channel and to reset the system.

The two comparators are used to detect when the VCO control voltage crosses the *VREFP* or *VREFN* threshold. This provides a rising edge on the *UP* or *DOWN* signal. The OR combination of the *UP* and *DOWN* signals is used as the *CLK* for a state machine that changes the switch control signals accordingly. This *CLK* signal is

also fed back to close a switch to ground the VCO control voltage to reset the tuning system and insure loop stability. When the VCO control voltage has returned within the thresholds sufficiently the switch to ground is opened and the *UP* or *DOWN* signals return low. Comparators with hysteresis are used to avoid unnecessary switching due to ripple in the VCO control voltage.

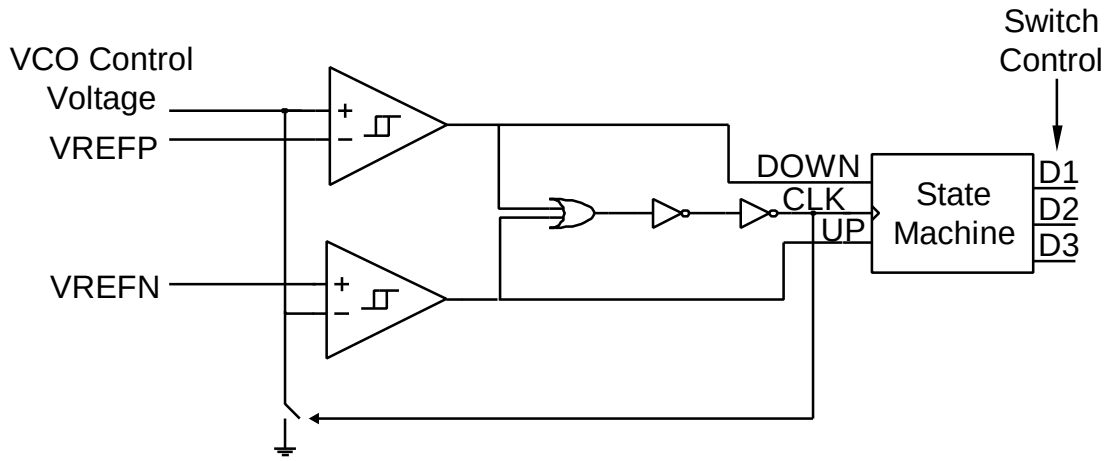

Figure 79 - VCO Switch Control System

Switch Control State Machine Design Procedure and Simulation Results

The switch control state machine is designed by first forming the state diagram and then synthesizing it into a sequential logic circuit. The state diagram for the state machine is given in Figure 80. State A corresponds to the lowest frequency band 1. All of the VCO control signals $D1-D3$ are high. This means that all of the discrete tuning capacitors are loading each inverter cells of the VCO. State B corresponds to frequency band 2. The VCO control signals $D1$ and $D2$ are high and $D3$ is low. This means that two of the discrete tuning capacitors are loading each inverter cell of the VCO. State C corresponds to frequency band 3. The VCO control signals $D1$ is high and $D2$ and $D3$ are low. This means that one of the discrete tuning capacitors is loading each inverter cell of the VCO. State D corresponds to frequency band 4. The VCO control signals $D1-D3$ are low. This means that none of the discrete tuning capacitors are loading

each inverter cell of the VCO. This state diagram is synthesized into the synchronous logic circuit shown in Figure 81.

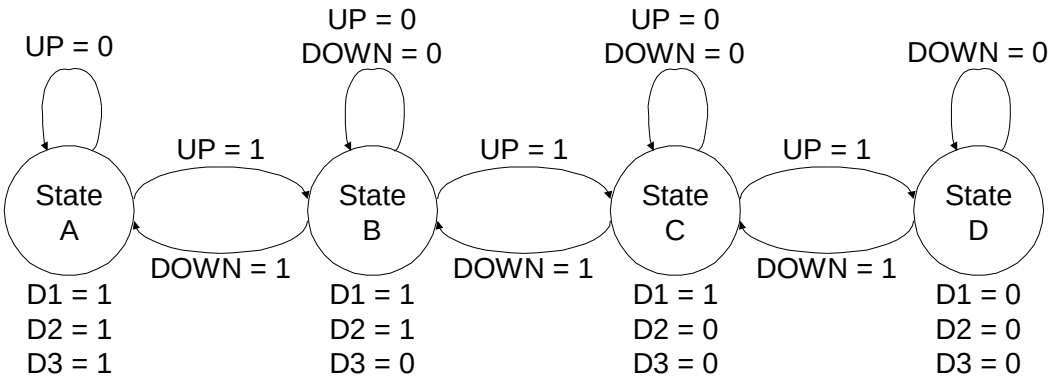

Figure 80 - Switch Control State Diagram

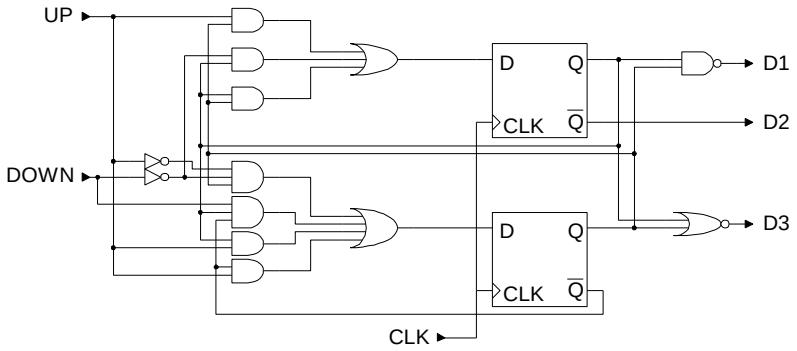

Figure 81 - Switch Control State Machine

Some simulation results of the state machine circuit are shown in Figure 82. This simulation shows the state machine circuit cycling from the initial state A when the $D1-D3$ outputs are high to state D when the $D1-D3$ outputs are low because the UP signal is high and the circuit is clocked 3 times. UP then goes low and $DOWN$ becomes high. The circuit then cycles from state D to state A because the $DOWN$ signal is high and the circuit is clocked 3 times.

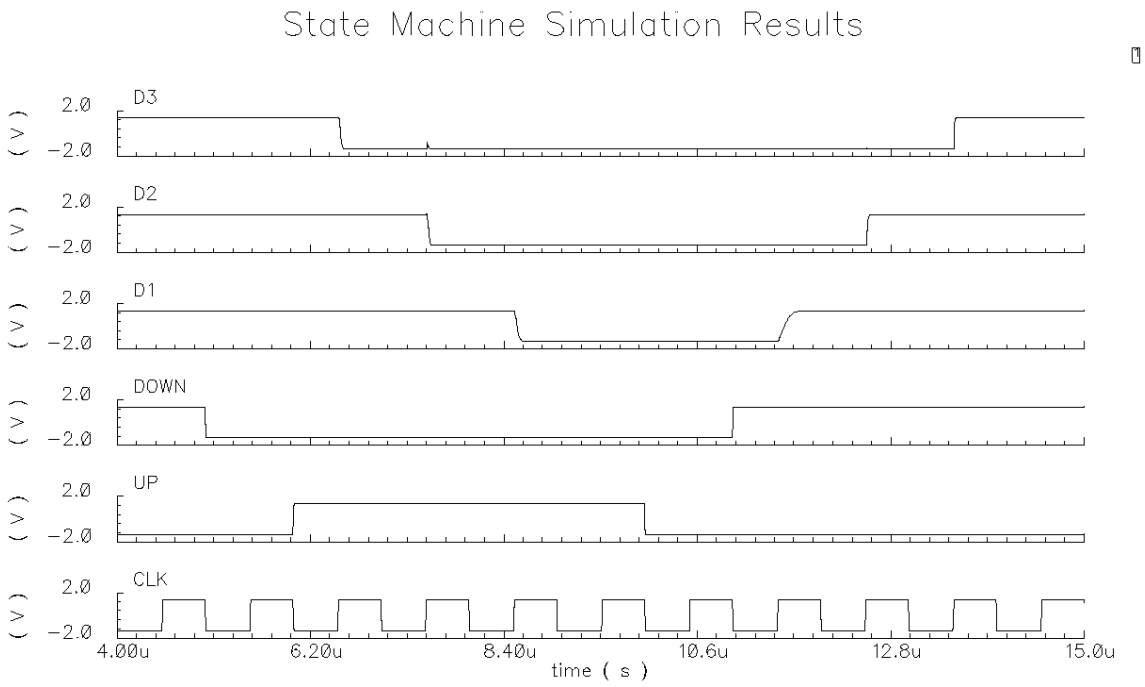

Figure 82 - Switch Control State Machine Simulation Results

Switch Control Comparators with Hysterisis Design Procedure and Simulation Results

The comparators with hysterisis used in the switch control system are shown in Figure 83 and Figure 84[39,48,51,52]. Due to the low power supply of 2.7V, an NMOS comparator is used to compare the VCO control voltage, v_c, with the 0.8V *VREFP* signal and a PMOS comparator is used to compare v_c with the −0.8V *VREFN* signal. Two comparators are designed to insure that the transistor with the threshold voltage input does not always operate in cutoff due to $|V_{GS}|$ being less than $|V_T|$.

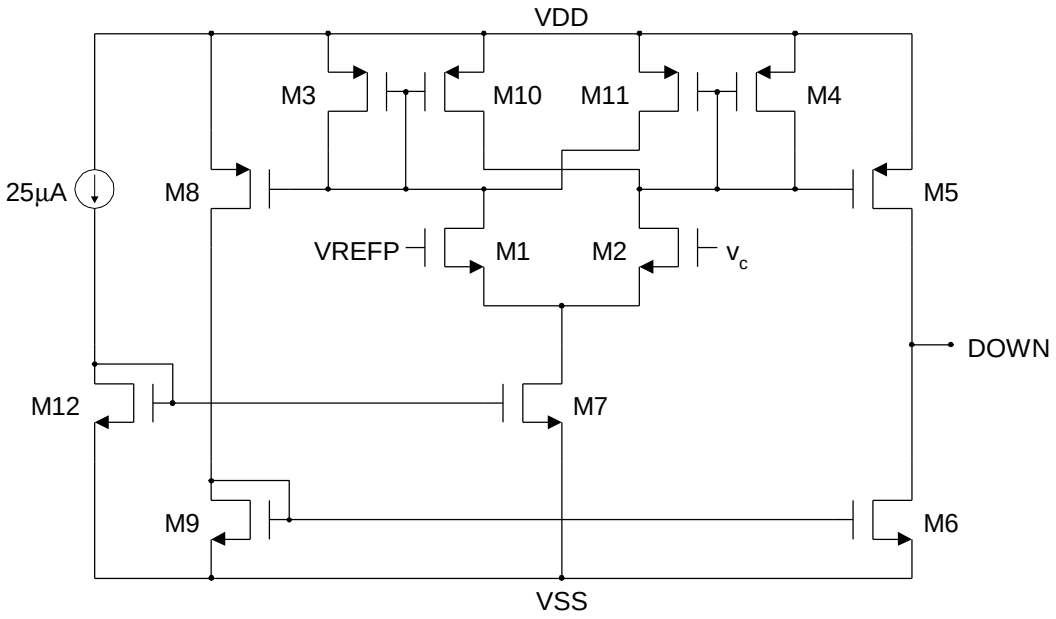

Figure 83 - Positive Threshold NMOS Comparator

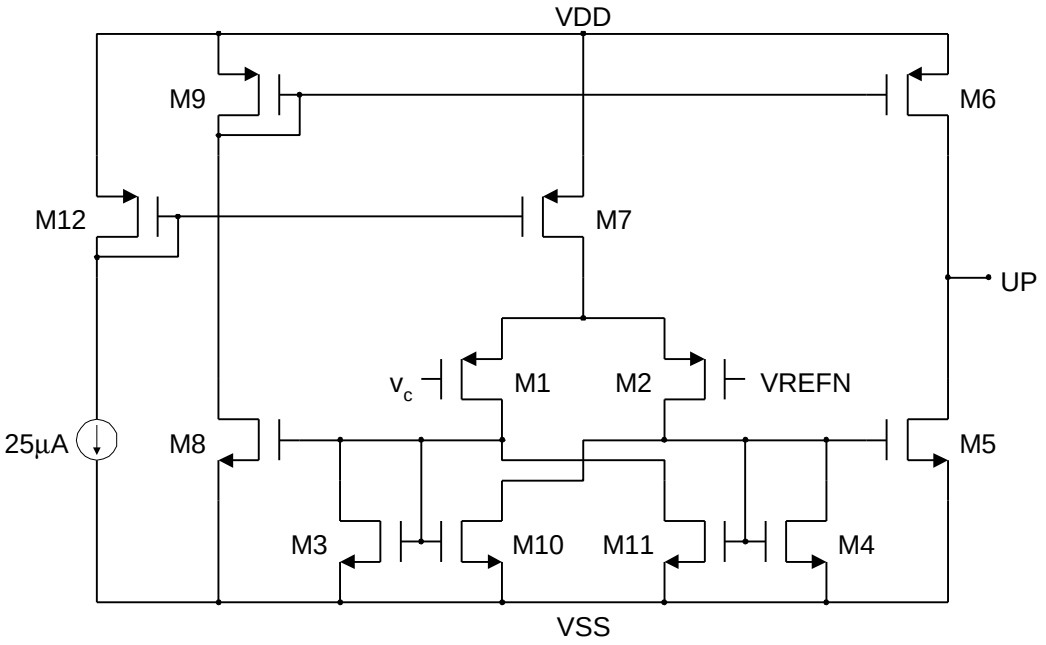

Figure 84 - Negative Threshold PMOS Comparator

The comparators consist of a differential input stage formed by M1-M2. M7 is the tail current source. The differential input stage is loaded with the cross-coupled transistors M3-M4 and M10-M11. There are two feedback paths associated with this circuit. Negative current feedback is achieved by the common source node of M1-M2[51,52]. Positive voltage-shunt feedback is formed by M10-M11[51,52]. Hysterisis is formed when the positive feedback is greater then the negative feedback. This is achieved under the following condition[39].

$$\left(\frac{W}{L}\right)_{10,11} \Big/ \left(\frac{W}{L}\right)_{3,4} > 1 \qquad \textbf{(127)}$$

This hysterisis is illustrated in Figure 85 that displays the transfer characteristic of the NMOS comparator.

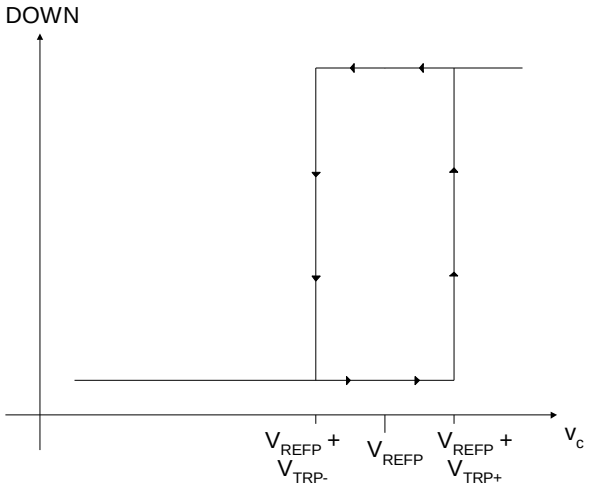

Figure 85 - Transfer Characteristic of a Comparator with Hysterisis

When hysterisis occurs the rising input signal, v_c, must pass the *VREFP* signal by V_{TRP+} before the output switches from low to high. When v_c is falling it must be lower than the *VREFP* signal by V_{TRP-} before the output switches from high to low. The trip points

are a function of the positive feedback factor, $\left(\frac{W}{L}\right)_{10} \Big/ \left(\frac{W}{L}\right)_{3}$, and the tail current I_{TAIL} as given in the following expressions[51,52].

$$V_{TRP+} = \sqrt{\frac{2I_{TAIL}}{KP\left(\frac{W}{L}\right)_1\left(1+\left(\frac{W}{L}\right)_{10} \Big/ \left(\frac{W}{L}\right)_3\right)}} \bullet \left(\sqrt{\frac{\left(\frac{W}{L}\right)_{10}}{\left(\frac{W}{L}\right)_3}} - 1\right)$$

$$V_{TRP-} = \sqrt{\frac{2I_{TAIL}}{KP\left(\frac{W}{L}\right)_1\left(1+\left(\frac{W}{L}\right)_{10} \Big/ \left(\frac{W}{L}\right)_3\right)}} \bullet \left(1 - \sqrt{\frac{\left(\frac{W}{L}\right)_{10}}{\left(\frac{W}{L}\right)_3}}\right) \qquad \textbf{(128)}$$

Based on the value of the ripple on the VCO control voltage, the trip points are set at a minimum of 100mV from the reference voltage. In the design of the comparators a feedback factor of 8 is chosen for the NMOS comparator and a feedback factor of 40 is used for the PMOS comparator in order to achieve the desired hysterisis. This results in the following relationship between M3-M4 and M10-M11.

$$\left(\frac{W}{L}\right)_{10,11N} = 8\left(\frac{W}{L}\right)_{3,4N}, \quad \left(\frac{W}{L}\right)_{10,11P} = 40\left(\frac{W}{L}\right)_{3,4P} \qquad \textbf{(129)}$$

A significant gain is needed for the comparators to switch hard. Therefore, a large gain is assigned to the M3-M6 and M4-M5 mirror stage. A gain of 24 is chosen for the NMOS comparator and a gain of 110 is chosen for the PMOS comparator. This results in the following relationship between M3-M4 and M5-M8.

$$\left(\frac{W}{L}\right)_{5,8N} = 24\left(\frac{W}{L}\right)_{3,4N}, \quad \left(\frac{W}{L}\right)_{5,8P} = 110\left(\frac{W}{L}\right)_{3,4P} \qquad \textbf{(130)}$$

A ratio of 16 is used in the NMOS differential pair to achieve the desired gain and a ratio of 37 is used in the PMOS differential pair.

$$\left(\frac{W}{L}\right)_{1,2N} = 16, \quad \left(\frac{\mathrm{W}}{\mathrm{L}}\right)_{1,2P} = 37 \qquad \textbf{(131)}$$

The tail current transistor M7 is sized to stay in saturation with a compliance voltage of 400mV from the power rail. This results in the following minimum values for M7.

$$\left(\frac{W}{L}\right)_{7N} > \frac{2I_{TAIL}}{KP_N V_{DSAT}^2} = \frac{2(25mA)}{(69.559mA/V^2)(0.4V)^2} = 4.5$$
$$\left(\frac{W}{L}\right)_{7P} > \frac{2I_{TAIL}}{KP_P V_{DSAT}^2} = \frac{2(25mA)}{(21.5mA/V^2)(0.4V)^2} = 14.5 \qquad \textbf{(132)}$$

A summary of the transistor sizes for the two comparators is given in Table 14.

Table 14 - Comparators with Hysterisis Transistor Sizes

Type	$(W/L)_{1,2}$	$(W/L)_{3,4}$	$(W/L)_{10,11}$	$(W/L)_{5,8}$	$(W/L)_{6,9}$	$(W/L)_{7,12}$
NMOS	48µ/3µ	3µ/1.2µ	24µ/1.2µ	72µ/1.2µ	24µ/1.2µ	90µ/12µ
PMOS	44.4µ/1.2µ	2.4µ/24µ	4.8µ/1.2µ	13.2µ/1.2µ	24µ/1.2µ	90µ/2.4µ

The simulated transfer characteristic for the NMOS comparator is given in Figure 86. The *VREFP* value is set to 0.8V and applied to the negative input. The VCO control voltage is swept from the negative rail to the positive rail and then back to the negative rail. The positive trip point, V_{TRP+}, is found to be 945mV. The negative trip point, V_{TRP-} is found to be 656mV. This exceeds the desired ripple margin of 100mV from the threshold.

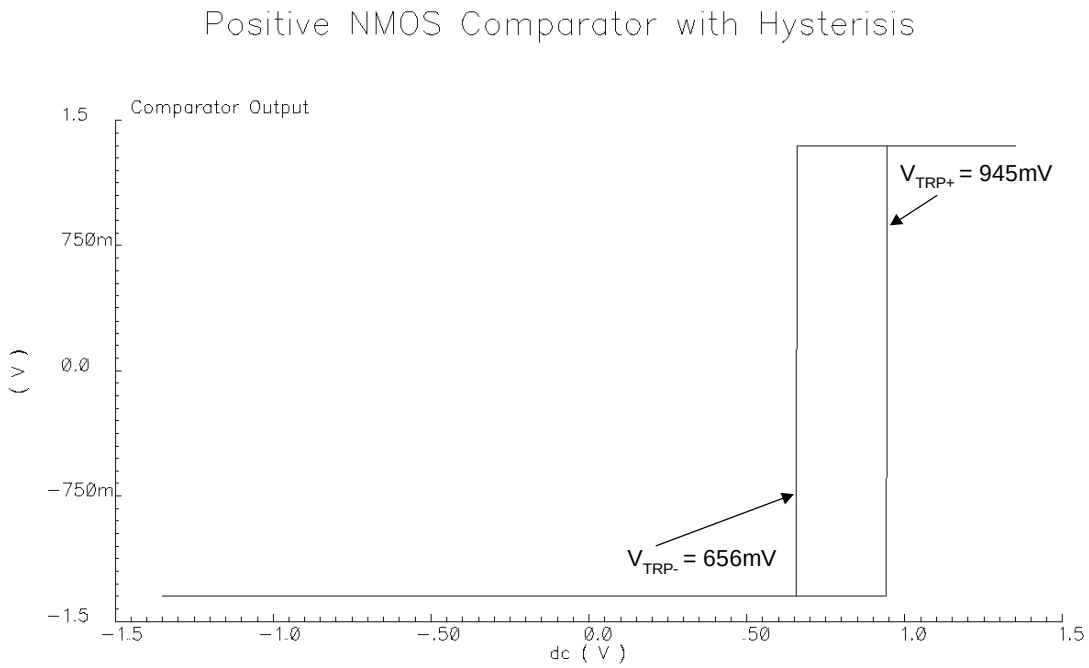

Figure 86 - NMOS Comparator with Hysterisis Transfer Characteristic

The simulated transfer characteristic for the PMOS comparator is given in Figure 87. The *VREFN* value is set to -0.8V and applied to the positive input. The VCO control voltage is swept from the positive rail to the negative rail and then back to the positive rail. The negative trip point, V_{TRP-}, is found to be –1.05V. The positive trip point, V_{TRP+} is found to be -550mV. This exceeds the desired ripple margin of 100mV from the threshold.

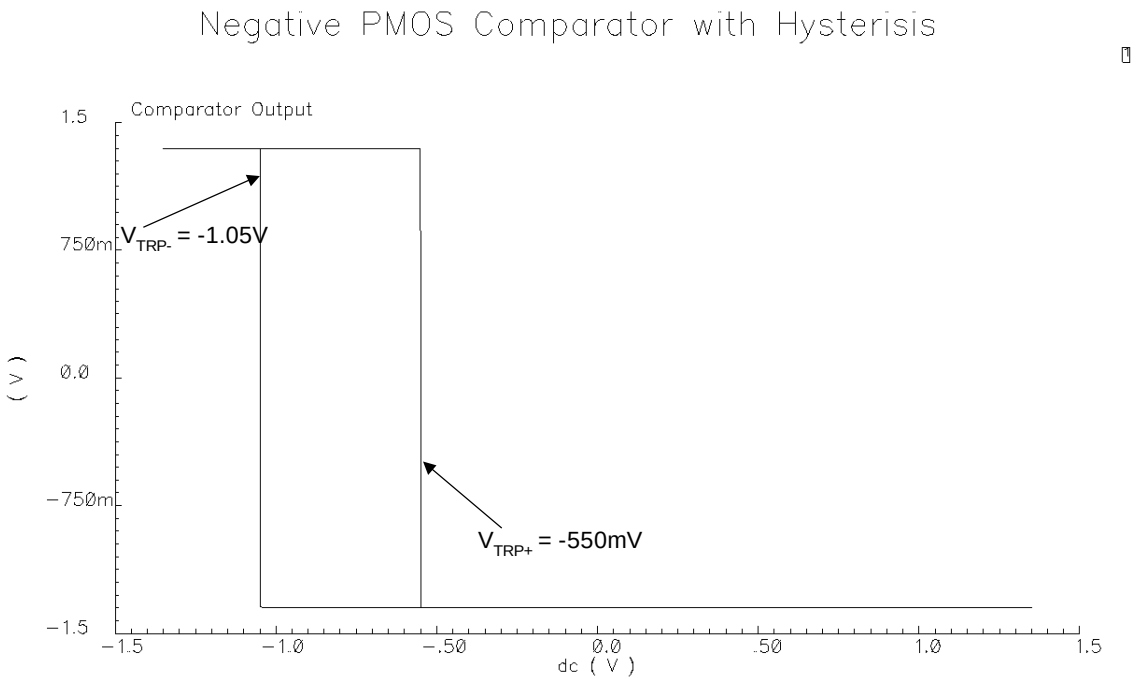

Figure 87 - PMOS Comparator with Hysterisis Transfer Characteristic

Loop Divider

The multi-band PLL frequency synthesizer has a fixed division ratio of $N = 32$. The loop divider consists of five cascaded divide-by-two circuits as shown in Figure 88. The divide-by-two circuits are implemented with D Flip-Flops that have the $\overline{Q}$ outputs fed back into the D inputs. The CLK signal is the input signal and the Q signal is the divide-by-two output.

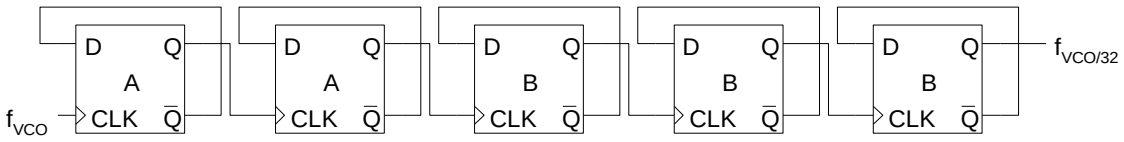

Figure 88 - Loop Divider Schematic

The schematic of the flip-flops that are used in the loop divider is shown in Figure 89[26]. These are dynamic flip-flops that operate at very high frequencies. The loop divider is the second most difficult circuit to design in the PLL after the VCO. The first flip-flop is especially difficult to design because it must operate at the same frequencies as the VCO.

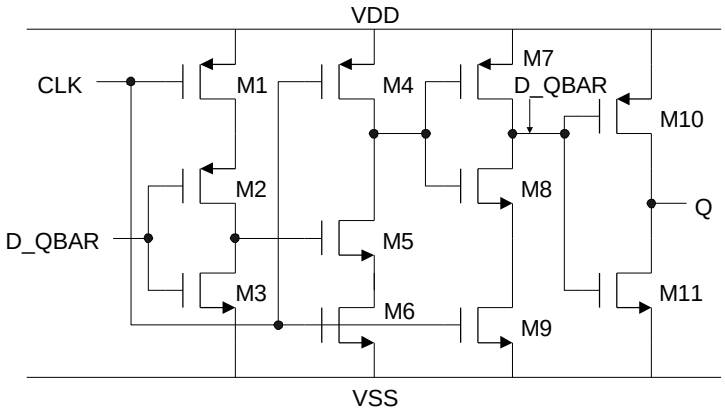

Figure 89 - Dynamic D Flip-Flop Schematic

The dynamic flip-flop used as a divide-by-2 can be looked at as the circuit shown in Figure 90. It is basically three clocked inverters cascaded with an output inverter. The first inverter operates when the clock is low, while the second and third inverters operate when the clock is high. This staggering of the clock control signals produces an output frequency half of the clock frequency.

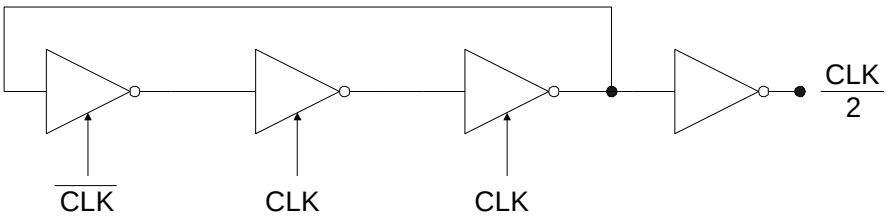

Figure 90 - Dynamic Divide-by-2 D Flip-Flop

Loop Divider Design Procedure and Simulation Results

The design of the loop divider is nontrivial due to the high frequency of operation of the dynamic flip-flops and the wide range of operation. The circuit is designed such that it is fast enough to operate at the highest frequency, but not too fast as to work improperly at the lower frequencies due to the early discharge of some nodes. This requires not all the flip-flops to have the same transistor sizes. The first two flip-flops are optimized for high speed, while the last three are optimized for mid to low frequency operation. In discussing the design of the flip-flop's transistors the subscript A refers to the first two flip-flops and B refers to the last three. The design procedure of the flip-flops is similar to the design procedure of the VCO where the circuit is designed and optimized through computer simulation while understanding the basic operation of the circuit. The loop divider D flip-flop design flow diagram is shown in Figure 91. The loop divider must operate from 100-300MHz.

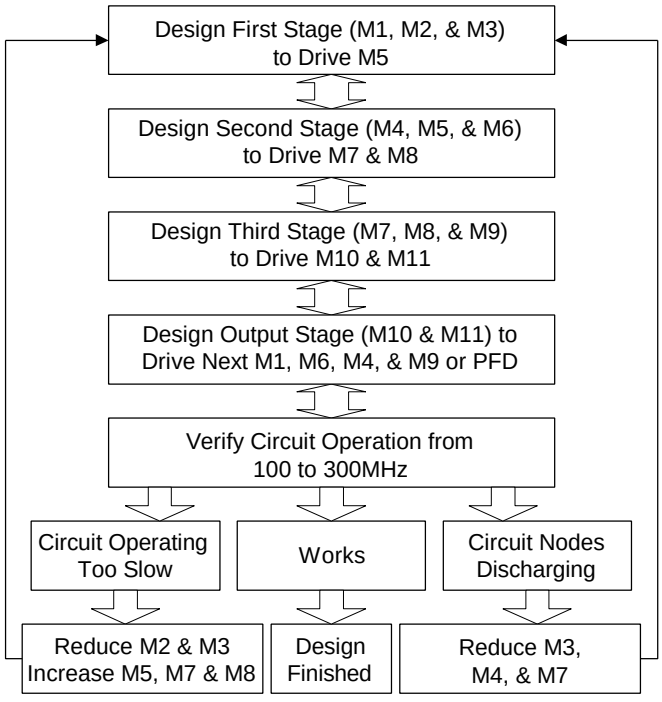

Figure 91 - Loop Divider D Flip-Flop Design Flow Diagram

The first stage of the flip-flop consists of M1, M2, and M3. This stage is active when the clock signal is low. M1 acts as a switch to VDD which is used to power the M2-M3 inverter. This inverter must drive the following parasitic capacitors in a minimum of four times the maximum CLK frequency in order to switch M5.

$$C_{parasitic1} = C_{gd2} + C_{db2} + C_{gd3} + C_{db3} + C_{gd5} + C_{gs5} + C_{gb5} \approx C_{gs5} \quad \textbf{(133)}$$

This parasitic capacitance is assumed to be 50fF. A switching current of approximately 1mA is needed to charge the parasitic capacitors in approximately 135ps to switch M5. This insures the flip-flop will operate at the maximum CLK of 300MHz. This implies the following aspect ratio for M3.

$$\left(\frac{W}{L}\right)_3 = \frac{2I}{KP_N\left(VDD - VSS - V_{TN}\right)^2} = \frac{2(1mA)}{(69.559\,mA/V^2)(2.7V - .7194V)^2} = 7.33 \Rightarrow \frac{9.6m}{1.2m} \quad \textbf{(134)}$$

M2 is designed for symmetric output drive. This implies the following aspect ratio for M2.

$$\left(\frac{W}{L}\right)_2 = \frac{KP_N}{KP_P}\left(\frac{W}{L}\right)_1 = \frac{69.559\,mA/V^2}{21.5\,mA/V^2}\left(\frac{9.6m}{1.2m}\right) \approx 3\left(\frac{9.6m}{1.2m}\right) \Rightarrow \frac{28.8m}{1.2m} \quad \textbf{(135)}$$

M1 is sized so that it can supply enough current fast enough to power the inverter when the clock goes low. The charge time is not as critical in the cascaded stages so M1 is made smaller in the B cell.

$$\left(\frac{W}{L}\right)_{1A} = \frac{16.8m}{1.2m}, \quad \left(\frac{\mathrm{W}}{\mathrm{L}}\right)_{1B} = \frac{4.8m}{1.2m} \quad \textbf{(136)}$$

The second stage of the flip-flop consists of M4, M5, and M6. This stage is active when the clock is high. M4 precharges the output of this stage to VDD when the clock is low. When the clock goes high M6 supplies power to M5 which acts as an inverter. If the

gate of M5 is high the output will get pulled low. If the gate of M5 is low the output will stay high due to precharging by M4. M5 must drive the following parasitic capacitors in a minimum of four times the maximum CLK frequency in order to switch M7 and M8.

$$C_{parasitic2} = C_{gd5} + C_{db5} + C_{gd4} + C_{db4} + C_{gs7} + C_{gd7} + C_{gb7} + C_{gs8} + C_{gd8} + C_{gb8} \approx C_{gs7} + C_{gs8} \quad \textbf{(137)}$$

This parasitic capacitance is assumed to be 100fF. A switching current of approximately 2.5mA is needed to charge the parasitic capacitors in approximately 108ps to switch M7 and M8. This insures the flip-flop will operate at the maximum CLK frequency of 300MHz. This implies the following aspect ratio for M5.

$$\left(\frac{W}{L}\right)_5 = \frac{2I}{KP_N\left(VDD - VSS - V_{TN}\right)^2} = \frac{2(2.5mA)}{(69.559\,mA/V^2)(2.7V - .7194V)^2} = 18.3 \Rightarrow \frac{21.6m}{1.2m} \quad \textbf{(138)}$$

M4 and M6 are sized so that they can charge their drain nodes quickly. The charge times are not as critical in the cascaded stages so M4 and M6 are made smaller in the B cell.

$$\left(\frac{W}{L}\right)_{4A} = \frac{43.2m}{1.2m}, \quad \left(\frac{\mathrm{W}}{\mathrm{L}}\right)_{4B} = \frac{16.8m}{1.2m}$$
$$\left(\frac{W}{L}\right)_{6A} = \frac{33m}{1.2m}, \quad \left(\frac{\mathrm{W}}{\mathrm{L}}\right)_{6B} = \frac{31.2m}{1.2m} \quad \textbf{(139)}$$

The third stage of the flip-flop consists of M7, M8, and M9. This stage is active when the clock is high. M9 acts as a switch to VSS which is used to power the M7-M8 inverter. This inverter must drive the following parasitic capacitor in a minimum of four times the maximum CLK frequency in order to switch M10, M11, M2, and M3.

$$C_{parasitic3} = C_{gd7} + C_{db7} + C_{gd8} + C_{db8} + C_{gs10} + C_{gd10} + C_{gb10} + C_{gs11} + C_{gd11} + C_{gb11} + C_{gs2} + C_{gd2} + C_{gb2} + C_{gs3} + C_{gd3} + C_{gb3} \approx C_{gs10} + C_{gs11} + C_{gs2} + C_{gs3} \quad \textbf{(140)}$$

This parasitic capacitance is assumed to be 100fF. A switching current of approximately 2mA is needed to charge the parasitic capacitors in approximately 135ps for the high frequency flip-flops. Approximately 1mA switching current is required to charge the parasitic capacitors in approximately 270ps for the lower frequency flip-flops. This implies the following aspect ratio for M8.

$$\left(\frac{W}{L}\right)_8 = \frac{2I}{KP_N\left(VDD - VSS - V_{TN}\right)^2} \Rightarrow$$
$$\left(\frac{W}{L}\right)_{8A} = \frac{16.8m}{1.2m}, \quad \left(\frac{W}{L}\right)_{8B} = \frac{9.6m}{1.2m} \qquad \textbf{(141)}$$

M7 is designed for symmetric output drive. This implies the following aspect ratio for M7.

$$\left(\frac{W}{L}\right)_7 = \frac{KP_N}{KP_P}\left(\frac{W}{L}\right)_8 = \frac{69.559\,mA/V^2}{21.5\,mA/V^2}\left(\frac{W}{L}\right)_8 \approx 3\left(\frac{W}{L}\right)_8$$
$$\left(\frac{W}{L}\right)_{7A} = \frac{40.8m}{1.2m}, \quad \left(\frac{W}{L}\right)_{7B} = \frac{28.2m}{1.2m} \qquad \textbf{(142)}$$

M9 is sized so that it can supply enough current fast enough to power the inverter when the clock goes low. The charge time is not as critical in the cascaded stages so M9 is made smaller in the B cell.

$$\left(\frac{W}{L}\right)_{9A} = \frac{24m}{1.2m}, \quad \left(\frac{\mathrm{W}}{\mathrm{L}}\right)_{9B} = \frac{12m}{1.2m} \qquad \textbf{(143)}$$

The output inverter stage consists of M10 and M11. This inverter must drive the following parasitic capacitors in a minimum of four times the maximum *CLK* frequency in order to switch M1, M4, M6, and M9 or the PFD input transistors.

$$C_{parasiticO} = C_{gd10} + C_{db10} + C_{gd11} + C_{db11} + C_{gs1} +$$
$$C_{gd1} + C_{gb1} + C_{gs4} + C_{gd4} + C_{gb4} + C_{gs6} + C_{gd6} +$$
$$C_{gb6} + C_{gs9} + C_{gd9} + C_{gb9} \approx C_{gs1} + C_{gs4} + C_{gs6} + C_{gs9} \qquad \textbf{(144)}$$

This parasitic capacitance is assumed to be 100fF. A switching current of approximately 2mA is needed in order to drive the parasitic capacitors in approximately 135ps. This implies the following aspect ratio for M11.

$$\left(\frac{W}{L}\right)_{11} = \frac{2I}{KP_N\left(VDD - VSS - V_{TN}\right)^2} = \frac{2(2mA)}{(69.559\,mA/V^2)(2.7V - .7194V)^2} \approx 15 \qquad \textbf{(145)}$$

The NMOS transistor M11 in the first two stages is made slightly larger to aid in driving the following stages.

$$\left(\frac{W}{L}\right)_{11A} = \frac{19.2m}{1.2m}, \quad \left(\frac{W}{L}\right)_{11B} = \frac{16.8m}{1.2m} \qquad \textbf{(146)}$$

M10 is designed for symmetric output drive. This implies the following aspect ratio for M10.

$$\left(\frac{W}{L}\right)_{10} = \frac{KP_N}{KP_P}\left(\frac{W}{L}\right)_{11} = \frac{69.559\,mA/V^2}{21.5\,mA/V^2}\left(\frac{W}{L}\right)_{11} \approx 3\left(\frac{W}{L}\right)_{11} \Rightarrow \frac{50.4m}{1.2m} \qquad \textbf{(147)}$$

Table 15 summarizes the transistor sizes for the dynamic flip-flops.

Table 15 - Dynamic Flip-Flop Transistor Sizes

Flip-Flop	$(W/L)_1$	$(W/L)_2$	$(W/L)_3$	$(W/L)_4$
A	16.8µ/1.2µ	28.8µ/1.2µ	9.6µ/1.2µ	43.2µ/1.2µ
B	4.8µ/1.2µ	28.8µ/1.2µ	9.6µ/1.2µ	16.8µ/1.2µ
Flip-Flop	$(W/L)_5$	$(W/L)_6$	$(W/L)_7$	$(W/L)_8$
A	21.6µ/1.2µ	33µ/1.2µ	40.8µ/1.2µ	16.8µ/1.2µ
B	21.6µ/1.2µ	31.2µ/1.2µ	28.2µ/1.2µ	9.6µ/1.2µ

Flip-Flop	$(W/L)_9$	$(W/L)_{10}$	$(W/L)_{11}$
A	24µ/1.2µ	50.4µ/1.2µ	19.2µ/1.2µ
B	12µ/1.2µ	50.4µ/1.2µ	16.8µ/1.2µ

This circuit can fail at high frequencies due to delays in the signal path. Optimizing the drive ratios of stages one through three can alleviate this problem. M2 and M3 can be made slightly smaller because they drive only M5. M5 can be increased to drive M7 and

M8 faster. M7 and M8 can be increased to drive the output stage faster. The sizes should be adjusted in the mentioned order to achieve optimal frequency performance.

This circuit can fail at low frequencies due to the discharge of the stages' output nodes. Increasing the output resistance of the stages alleviates this problem. Reducing M3, M4, and M7 accomplishes this.

Figure 92 shows the simulation of the loop divider operating at 300MHz.

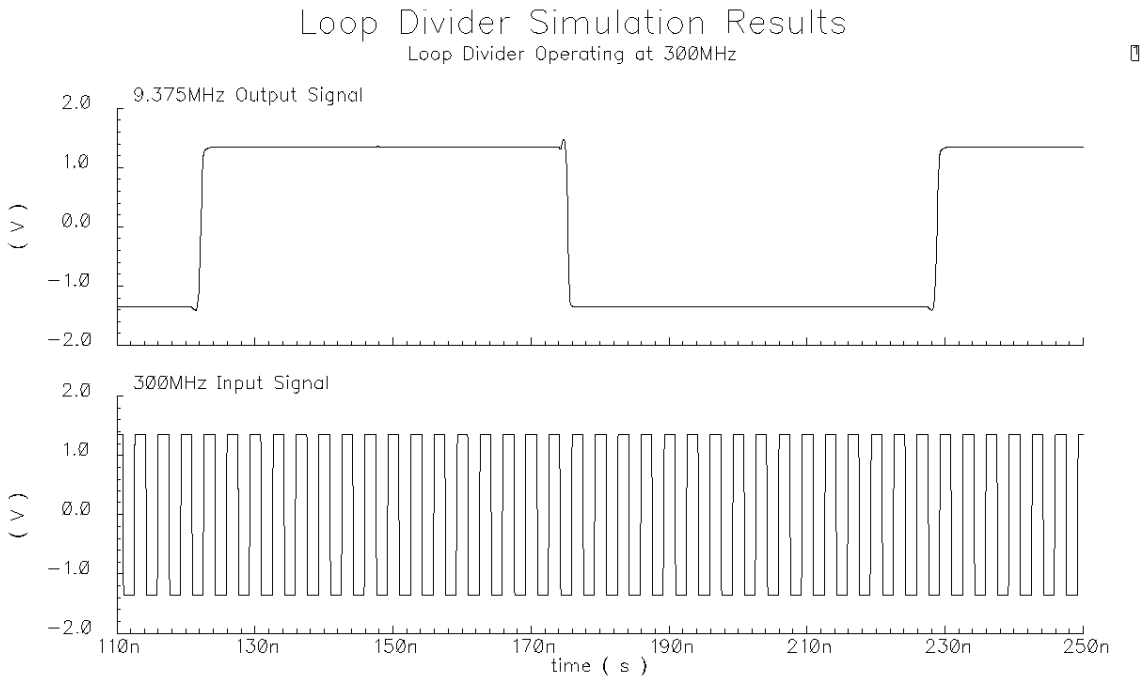

Figure 92 - Loop Divider Simulation Results

Multi-Band PLL System Simulation Results

The transistor level building blocks are combined to form the multi-band PLL system. System level simulations are done to verify the functionality of the multi-band PLL system. The performance of the multi-band PLL system is illustrated through 5 case studies. These case studies range from synthesizing a signal in-band to more complex

situations such as synthesizing an edge-of-band signal or a signal that falls in the channel overlap. The multi-band PLL is initially operating in the multi-band region of band 4 at a frequency of 280MHz for all cases. Table 16 summarizes the setup for each case.

Table 16 - Multi-Band PLL Frequency Synthesizer Case Studies

Case	Initial Frequency	Final Frequency	? f	Simulation Type	Acquisition Time
A	280MHz	310MHz	30MHz	Mid-Band	5µs
B	280MHz	190MHz	-90MHz	Mid-Band (Band Change)	13µs
C	280MHz	100MHz	-180MHz	Lowest Edge-of-Band	18µs
D	280MHz	340MHz	60MHz	Highest Edge-of Band	19µs
E	280MHz	160MHz	-120MHz	Overlap	14µs

Case A

The first system level simulation presented shows the PLL synthesizing a 310MHz signal. This illustrates a situation where a mid-band frequency in the current band is being synthesized. Figure 93 shows the VCO control signals. All three digital inputs are initially low which means the PLL is in the correct band of operation. The initial output is approximately 280MHz. The VCO control voltage then settles to synthesize 310MHz without triggering the switch control mechanism. The acquisition time is approximately 5µs. This acquisition time is low because the frequency change is within the lock range. Figure 94 shows the 310MHz output signal and its frequency spectrum.

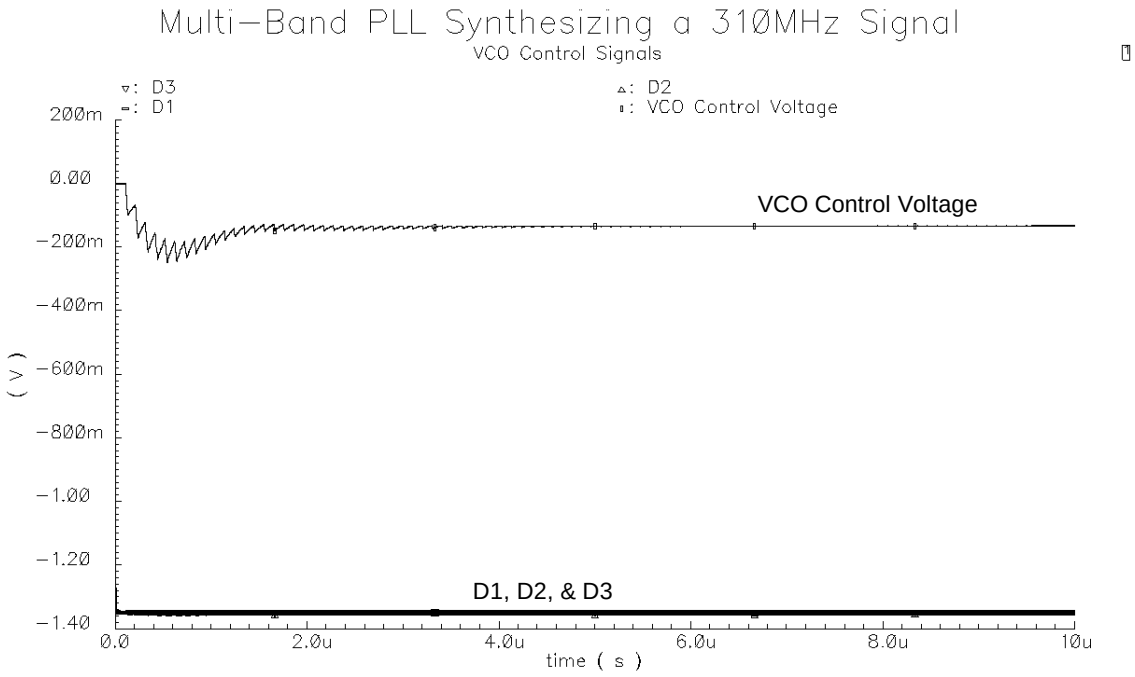

Figure 93 - VCO Control Signals for Multi-Band PLL 310MHz Output

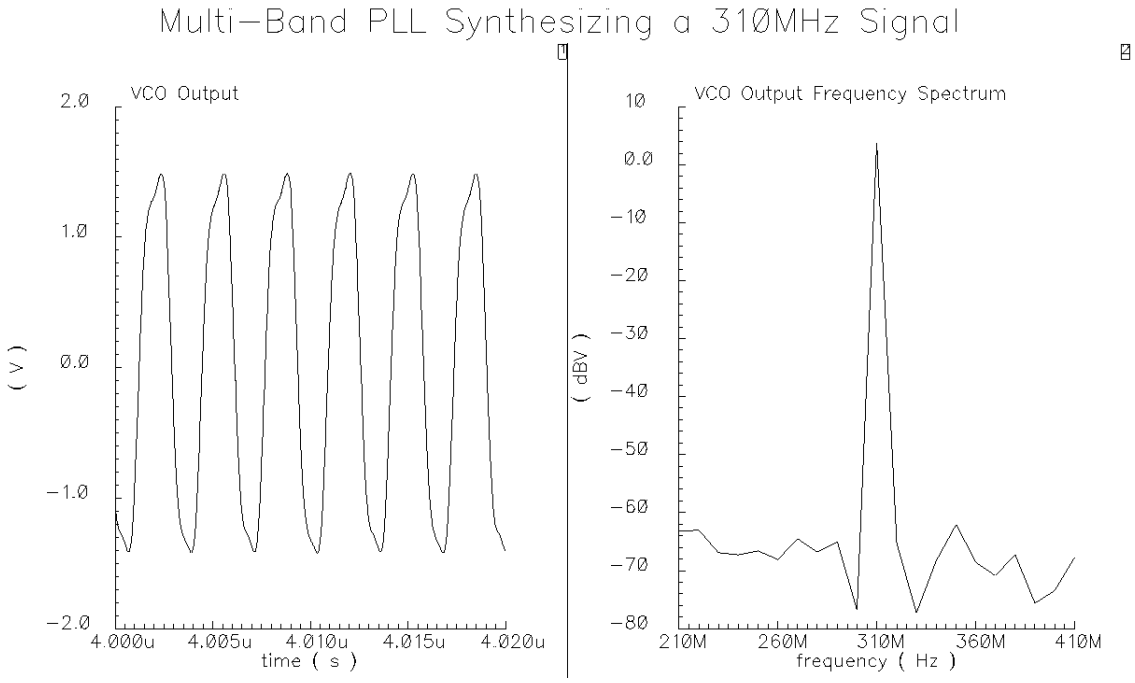

Figure 94 - 310MHz Multi-Band PLL Output Signal

Case B

The second system level simulation presented shows the PLL synthesizing a 190MHz signal. This illustrates a situation where a mid-band frequency out of the current band is being synthesized. Figure 95 shows the VCO control signals. All three digital inputs are initially low which means the PLL is not in the correct band of operation. The initial output is approximately 280MHz. The VCO control voltage rises and triggers the switch control mechanism. The digital control signal *D*1 then goes high and the VCO control voltage is grounded. The PLL is now in the correct band of operation. The VCO control voltage then settles to synthesize 190MHz. The acquisition time is approximately 13µs. This acquisition time is longer because the frequency change is outside the lock range and the acquisition process becomes a pull-in process. Figure 96 shows the 190MHz output signal and its frequency spectrum.

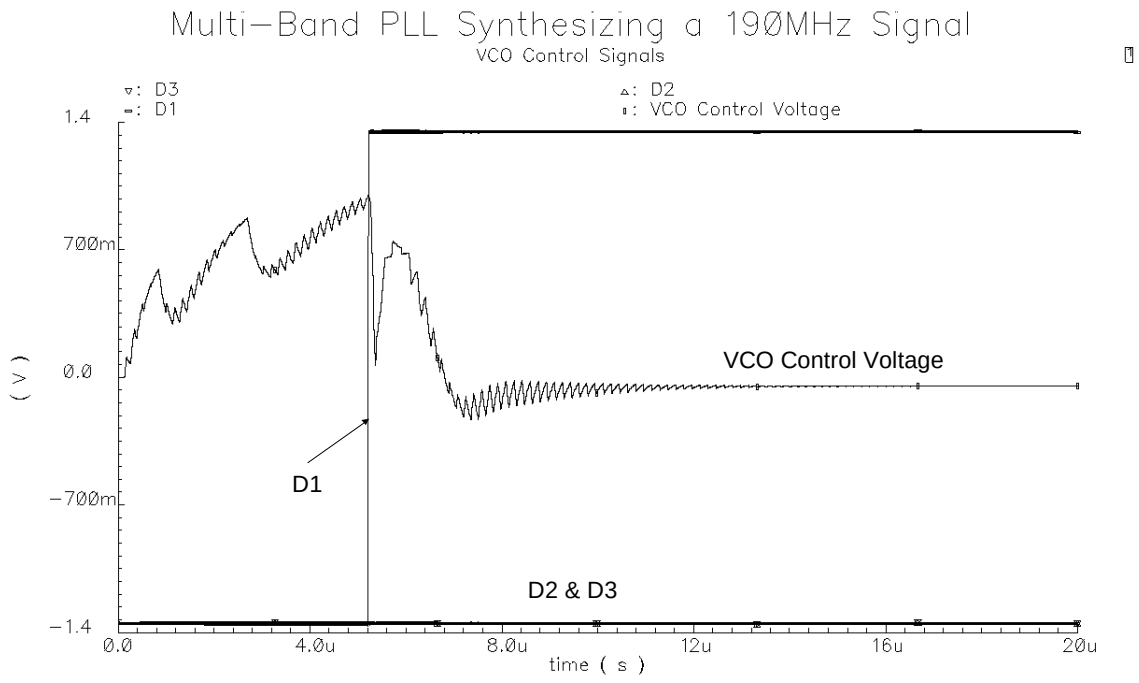

Figure 95 - VCO Control Signals for Multi-Band PLL 190MHz Output

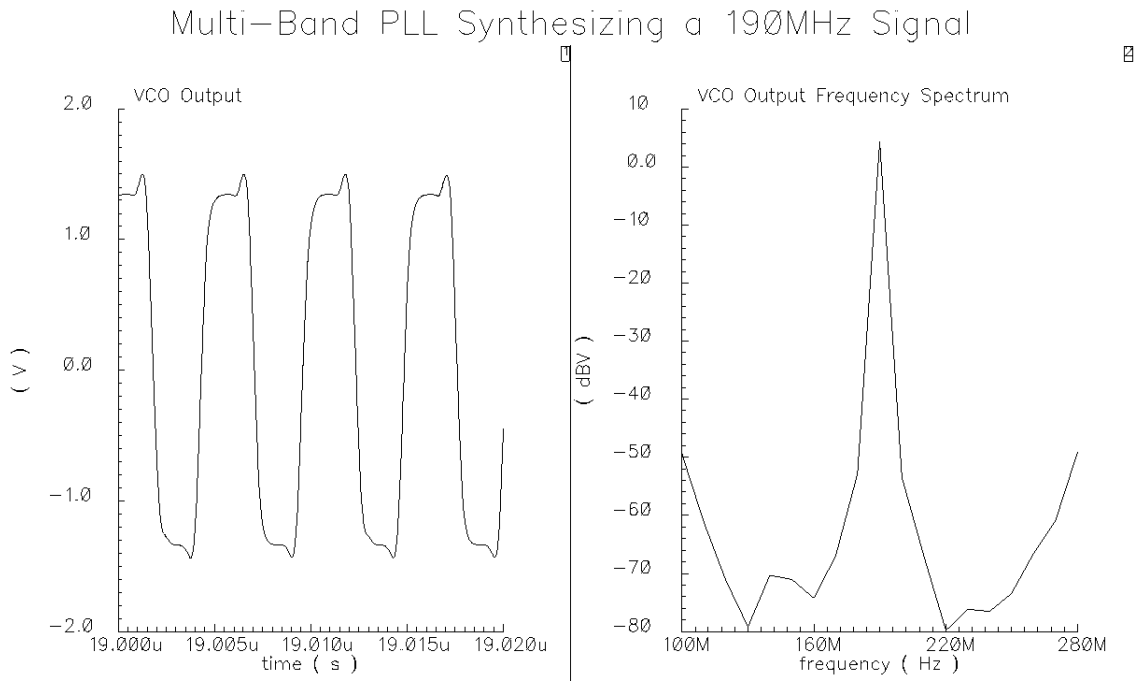

Figure 96 - 190MHz Multi-Band PLL Output Signal

Case C

The third system level simulation presented shows the PLL synthesizing a 100MHz signal. This illustrates a situation where close to the lowest edge-of-band frequency is being synthesized. Figure 97 shows the VCO control signals. All three digital inputs are initially low which means the PLL is not in the correct band of operation. The initial output is approximately 280MHz. The VCO control voltage rises and triggers the switch control mechanism. The digital control signal $D1$ then goes high and the VCO control voltage is grounded. The PLL is still not in the correct band of operation. The VCO control voltage rises and triggers the switch control mechanism. The digital control signal $D2$ then goes high and the VCO control voltage is grounded. The PLL is still not in the correct band of operation. The VCO control voltage rises and triggers the switch control mechanism. The digital control signal $D3$ then goes high and the VCO control voltage is grounded. The PLL is now in the correct band of operation. The VCO control voltage then settles to synthesize 100MHz. The acquisition time is approximately 18µs.

This acquisition time is longer because the frequency change is outside the lock range and the acquisition process becomes a pull-in process. Figure 98 shows the 100MHz output signal and its frequency spectrum.

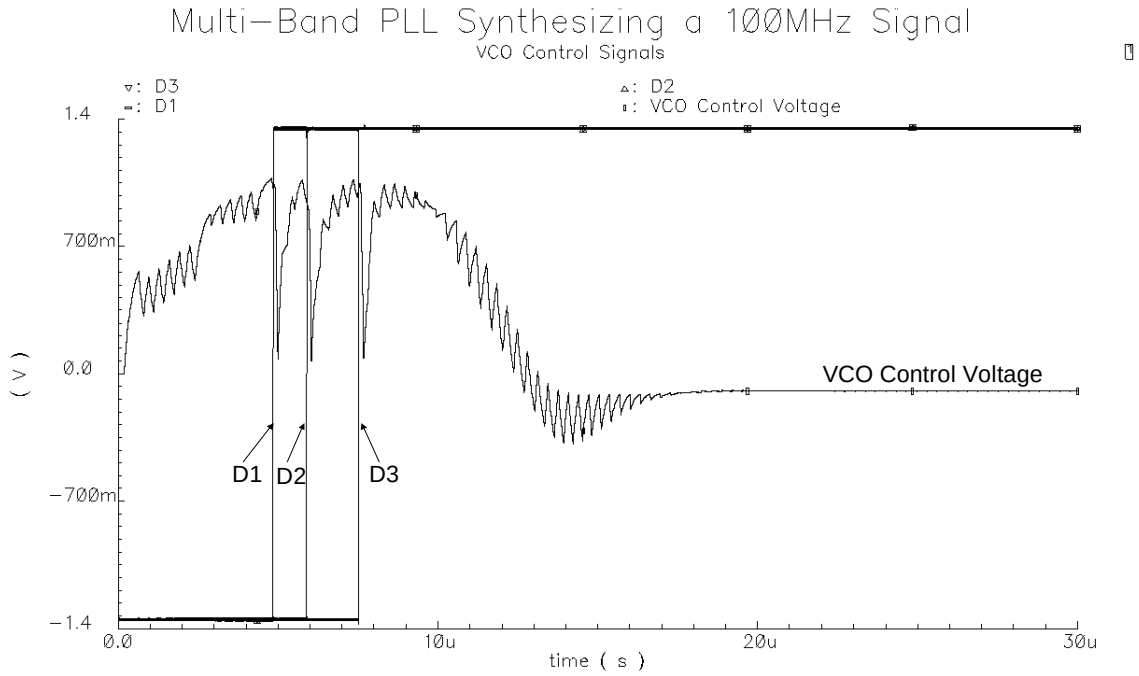

Figure 97 - VCO Control Signals for Multi-Band PLL 100MHz Output

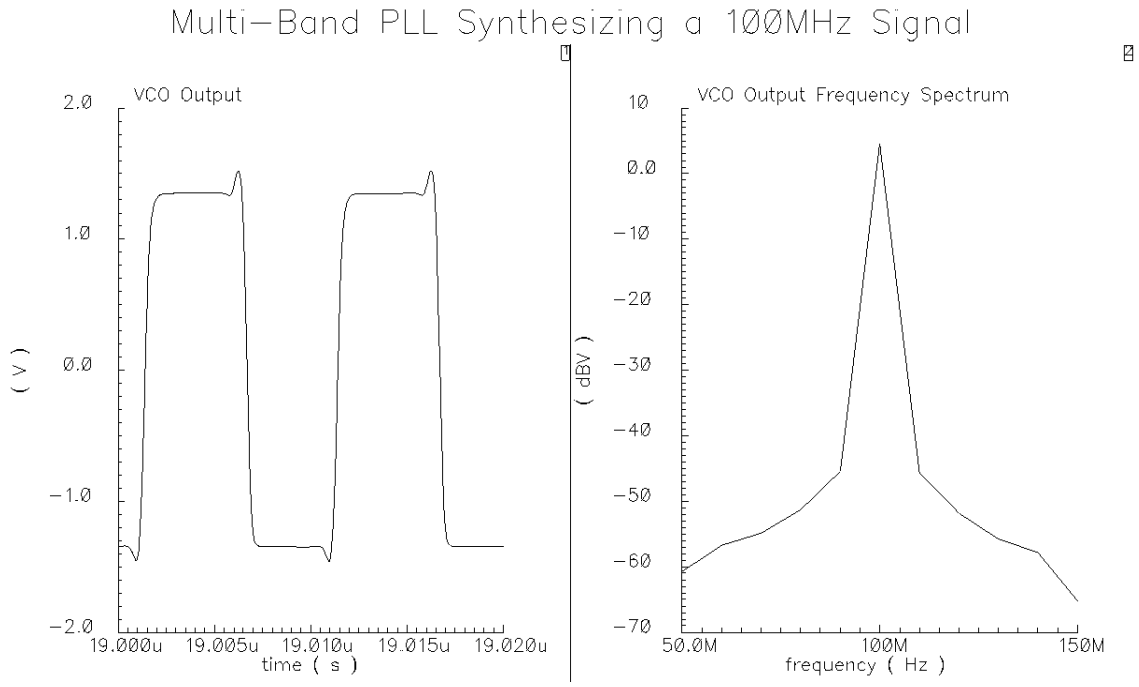

Figure 98 - 100MHz Multi-Band PLL Output Signal

Case D

The fourth system level simulation presented shows the PLL synthesizing a 340MHz signal. This illustrates a situation where close to the highest edge-of-band frequency is being synthesized. Figure 99 shows the VCO control signals. All three digital inputs are initially low which means the PLL is in the correct band of operation. The initial output is approximately 280MHz. Even though the PLL is in the correct band of operation, the VCO control voltage still drops low enough to trigger the switch control mechanism several times because the frequency that is attempted to synthesize is on the edge of the synthesizer's performance. This unnecessary triggering of the switch control mechanism does not change the band of operation because the state machine is in the highest state. The VCO control voltage finally settles to synthesize 340MHz. The acquisition time is approximately 19µs. This acquisition time is longer because the frequency change is outside the lock range and the acquisition process becomes a pull-in process. Figure 100 shows the 340MHz output signal and its frequency spectrum.

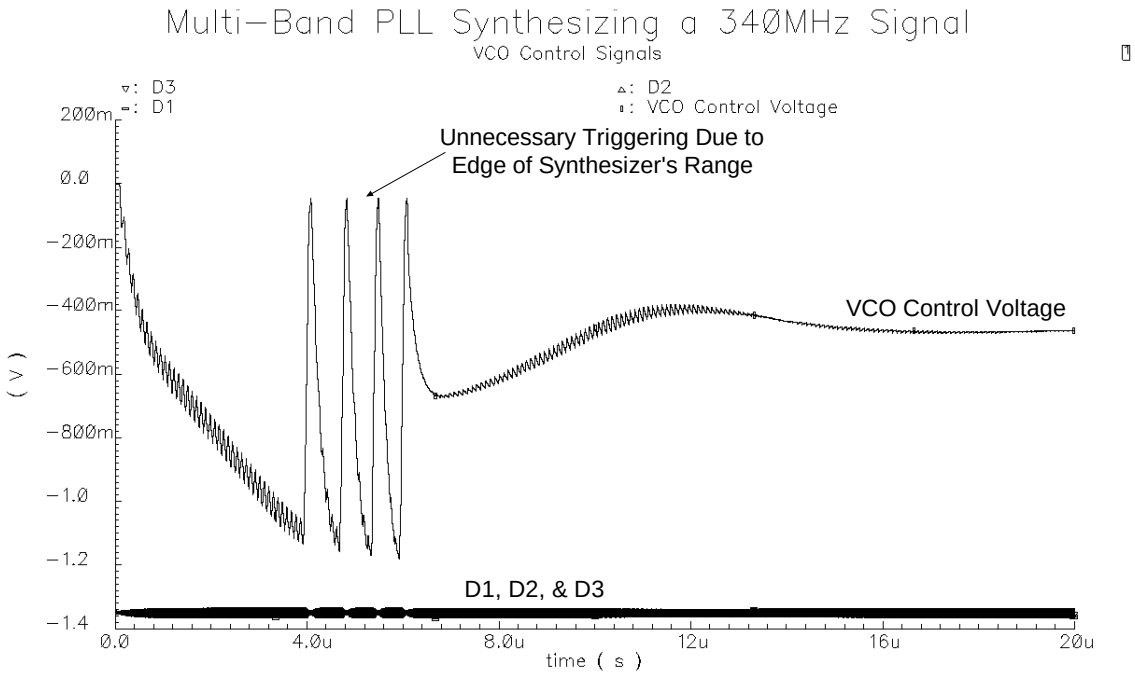

Figure 99 - VCO Control Signals for the Multi-Band PLL 340MHz Output

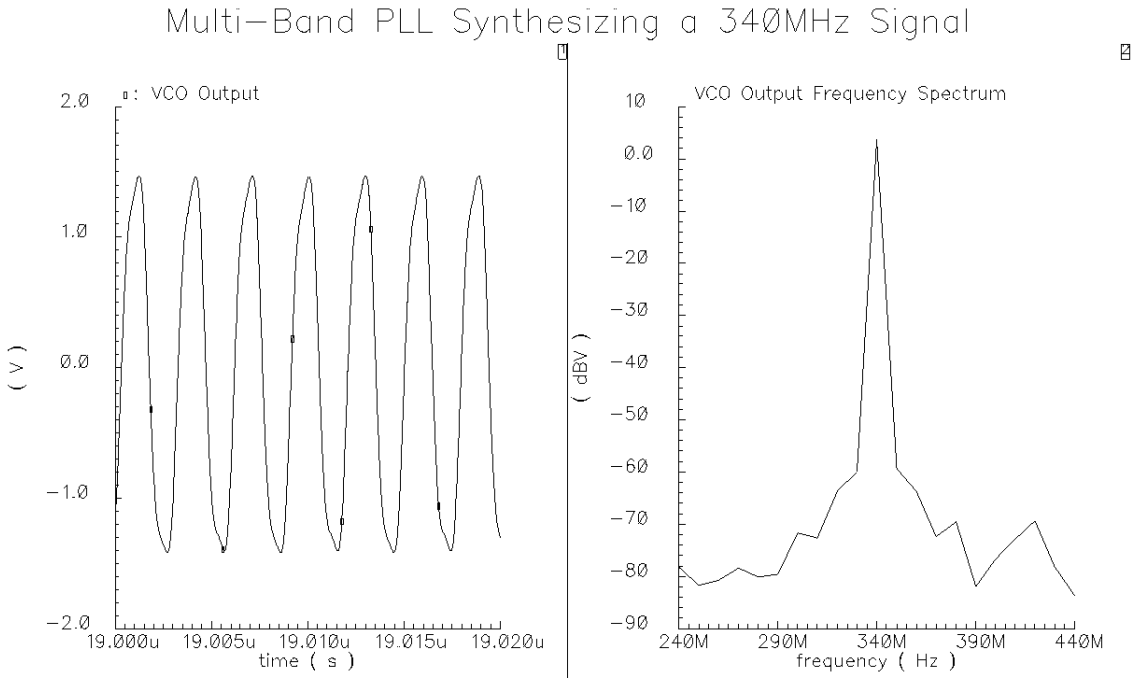

Figure 100 - 340MHz Multi-Band PLL Output Signal

Case E

The fifth system level simulation presented shows the PLL synthesizing a 160MHz signal. This illustrates a situation where a frequency that lies in the overlap between two channels is being synthesized. Figure 101 shows the VCO control signals. All three digital inputs are initially low which means the PLL is not in the correct band of operation. The initial output is approximately 280MHz. The VCO control voltage rises and triggers the switch control mechanism. The digital control signal *D*1 then goes high and the VCO control voltage is grounded. The PLL is now in the correct band of operation. The VCO control voltage then settles to synthesize 160MHz. The acquisition time is approximately 14µs. This acquisition process is a pull-in process. Figure 102 shows the 160MHz output signal and its frequency spectrum.

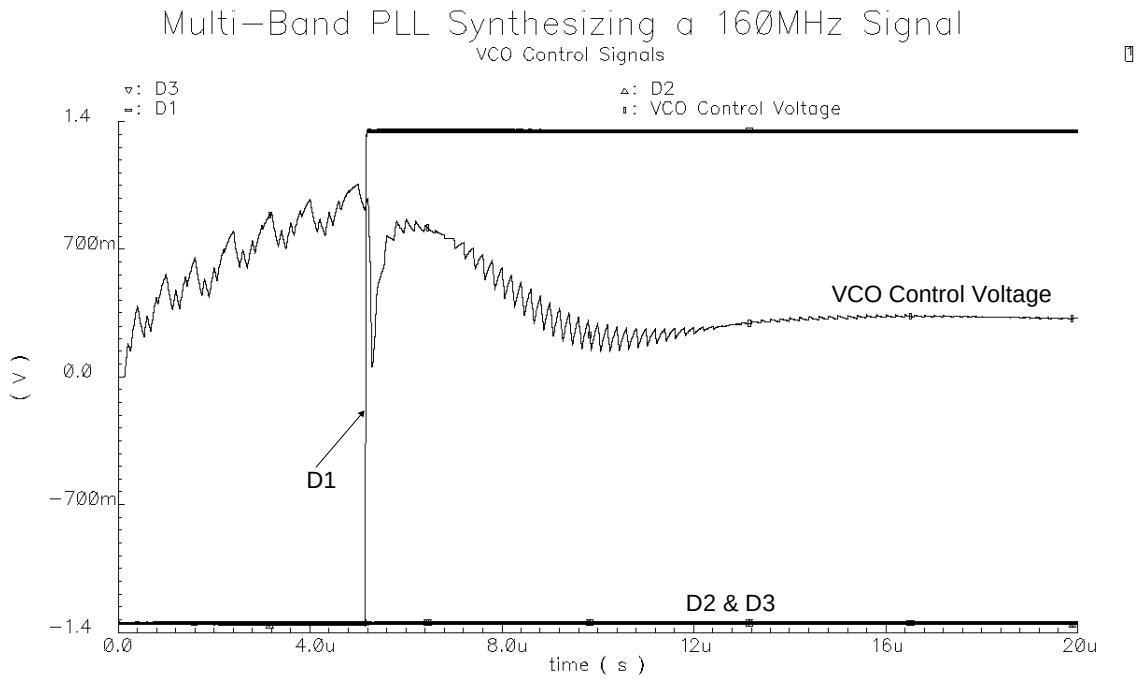

Figure 101 - VCO Control Signals for Multi-Band PLL 160MHz Output

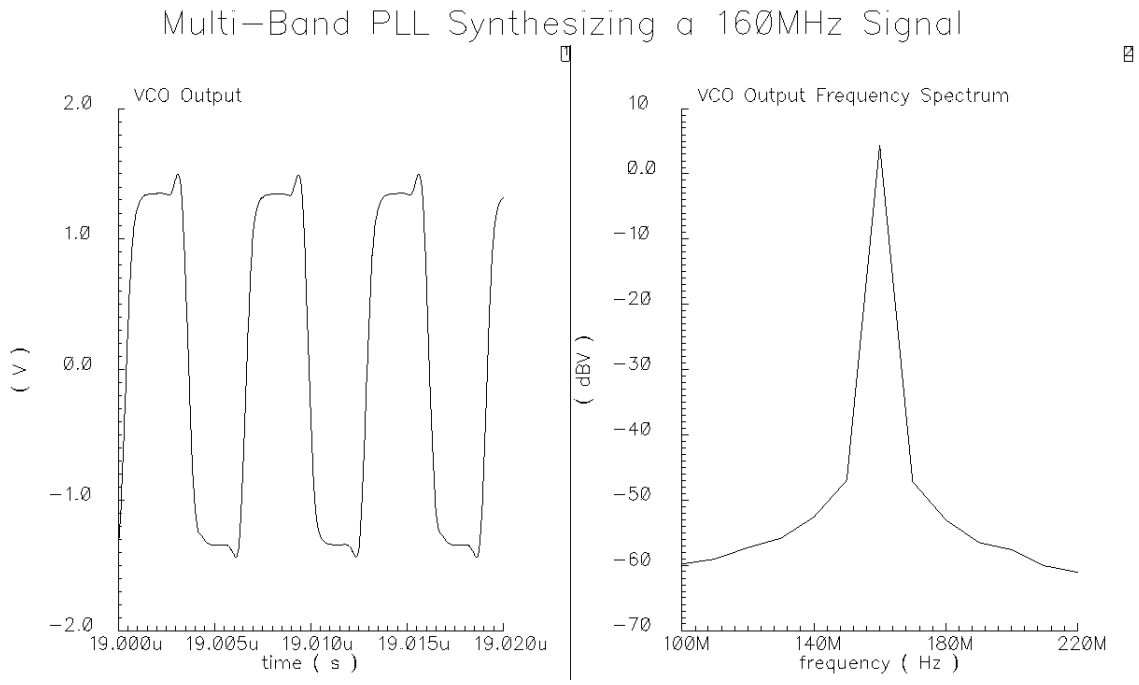

Figure 102 - 160MHz Multi-Band PLL Output Signal

Classic Digital PLL Design and Simulation Results

A classic digital phase-locked loop was designed for comparison with the multi-band phase-locked loop system. This PLL contains a single-band voltage-controlled oscillator that is only tuned continuously. The PLL also does not have any switch control system or discrete capacitors. The other PLL blocks are the same ones used in the multi-band design.

The main difference between the performance of the two PLLs is due to the different VCOs. Figure 103 shows the VCO used in the classic digital PLL.

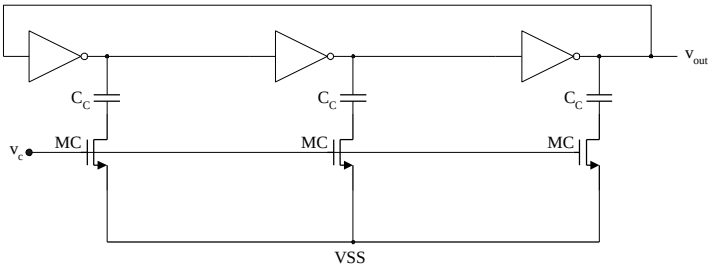

Figure 103 - Classic Digital PLL VCO

This VCO is the same one used in the multi-band PLL except the discrete capacitors and switch transistors have been removed. The same transistor aspect ratios and capacitor sizes have been used. This VCO has a tuning range of 229.8-385 MHz. Figure 104 shows the VCO transfer curve.

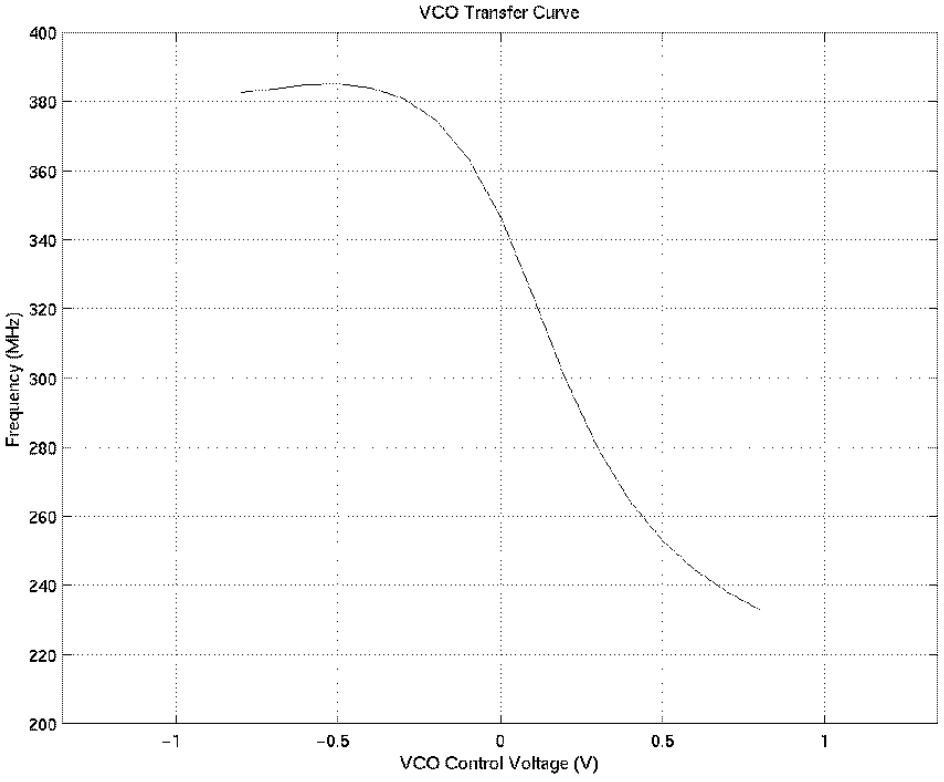

Figure 104 - Classic Digital PLL VCO Transfer Curve

This VCO has a higher maximum frequency due to less parasitic capacitance associated with the routing of the discrete capacitors. It has a conversion gain of –97MHz/V. This is higher than any of the switched-tuned VCO channel's conversion gains. The simulated phase noise performance of this VCO ranges from –83.74 to –93.6dBc/Hz at a 50kHz offset. Referring to Table 13, this is comparable to the switched tuning VCO's band 4 simulated phase noise performance of –82.63 to –96.67dBc/Hz at a 50kHz offset. Band 4 of the switched tuning VCO has a conversion gain of –94.75MHz/V. The other switched tuning oscillator frequency bands have lower conversion gains. This results in better simulated phase noise performance than the classic digital PLL VCO.

The performance of the classic digital PLL is illustrated through 3 case studies. These case studies include synthesizing the edge of range frequencies and a mid-range frequency. Table 17 shows the setup for each case.

Table 17 - Classic Digital PLL Frequency Synthesizer Case Studies

Case	Initial Frequency	Final Frequency	? f	Simulation Type	Acquisition Time
A	350MHz	380MHz	30MHz	Near Maximum Frequency	10µs
B	350MHz	230MHz	-120MHz	Near Minimum Frequency	14µs
C	350MHz	260MHz	-90MHz	Mid-Band	5µs

Case A

The classic digital PLL was simulated to synthesize a 380MHz signal. This is close to the maximum frequency that the classic digital PLL can synthesize. Figure 105 shows the VCO control voltage as the PLL acquires lock. Initially the PLL is outputting a 350MHz signal. The loop dynamics take over and the VCO control voltage drops to synthesize the 380MHz signal. The acquisition time is approximately 10µs. The reason for the length of the acquisition time is that the PLL is operating in a region where the

VCO gain has decreased due to non-linearity in the gain. Figure 106 shows the 380MHz output and frequency spectrum.

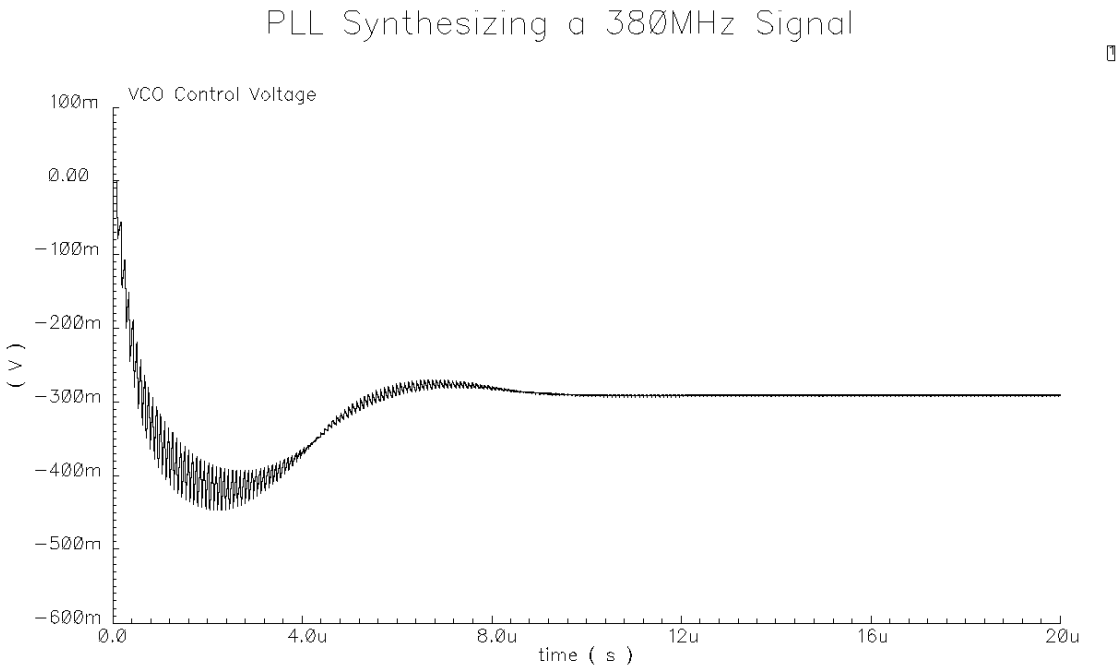

Figure 105 - VCO Control Voltage for Classic Digital PLL 380MHz Output

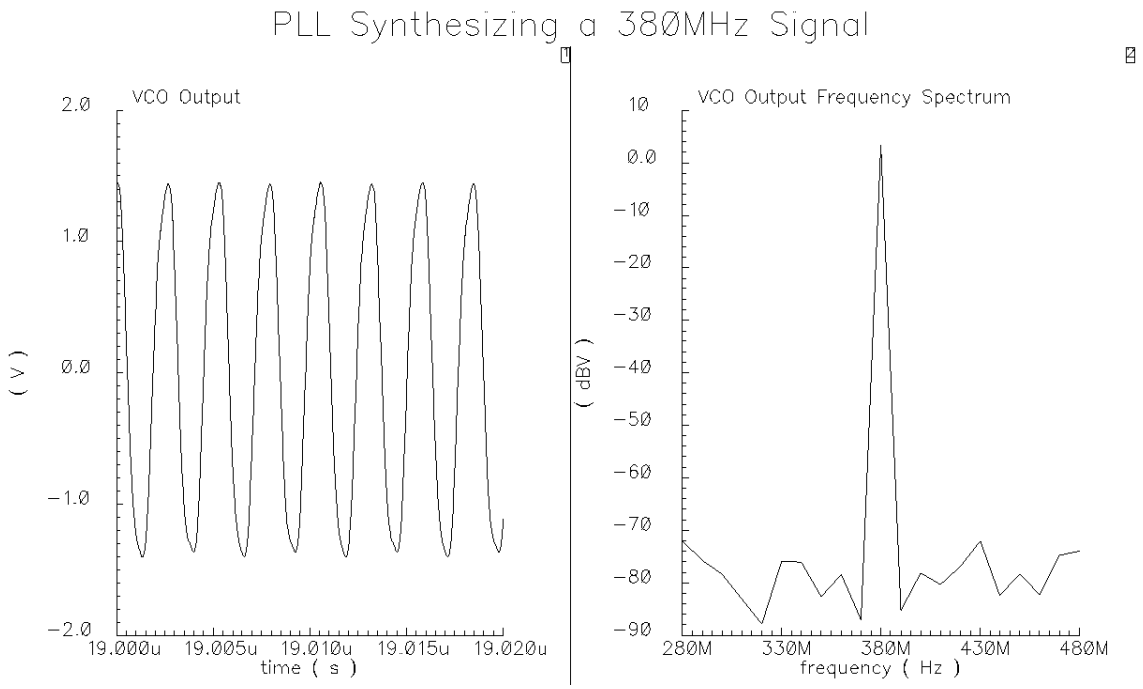

Figure 106 - 380MHz Classic Digital PLL Output Signal

Case B

The classic digital PLL was simulated to synthesize a 230MHz signal. This is close to the minimum frequency that the classic digital PLL can synthesize. Figure 107 shows the VCO control voltage as the PLL acquires lock. Initially the PLL is outputting a 350MHz signal. The loop dynamics take over and the VCO control voltage rises to synthesize the 230MHz signal. The acquisition time is approximately 14µs. The length of the acquisition time is due to the frequency change being outside of the lock range. The acquisition process is a pull-in process. Figure 108 shows the 230MHz output and frequency spectrum.

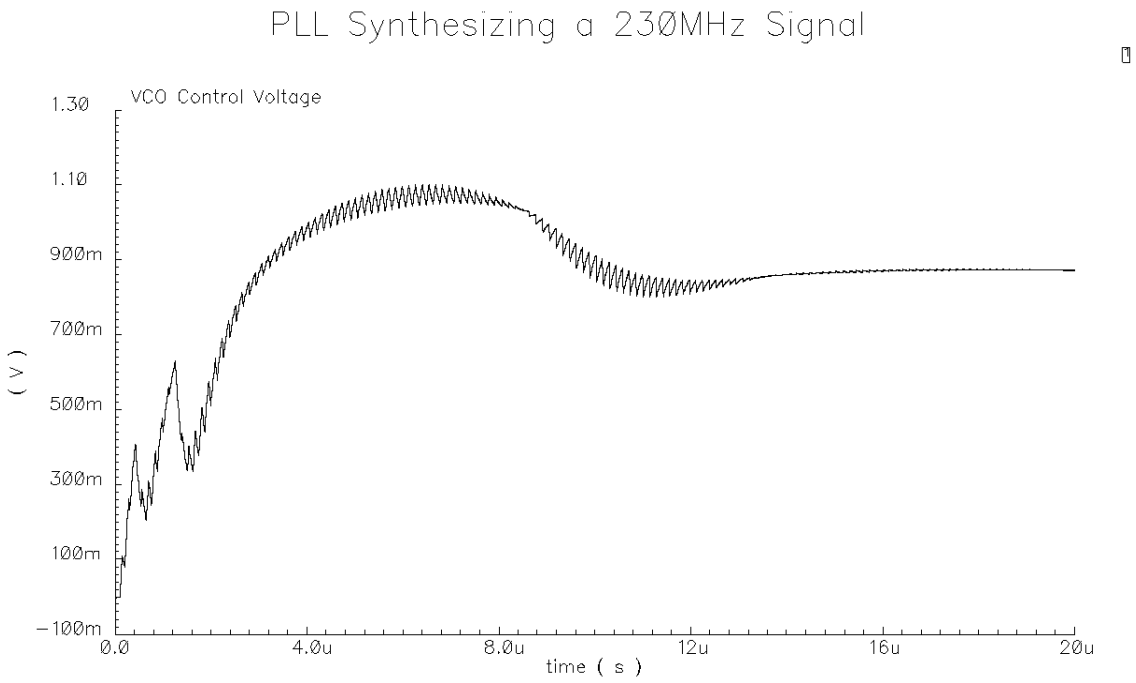

Figure 107 - VCO Control Voltage for Classic Digital PLL 230MHz Output

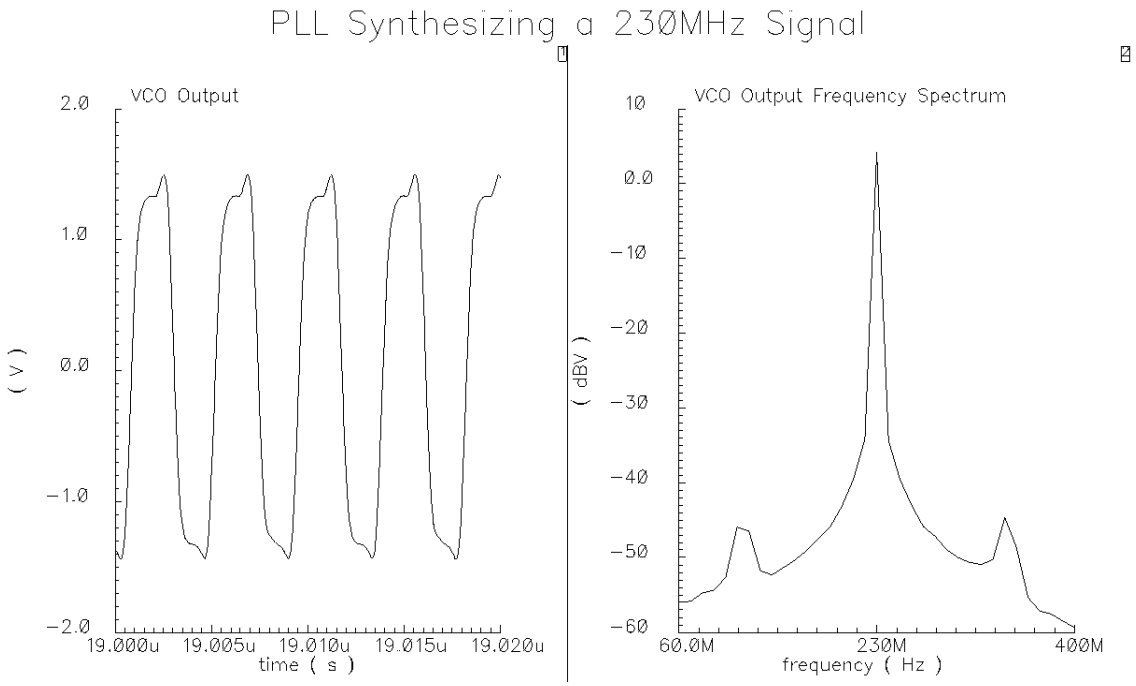

Figure 108 - 230MHz Classic Digital PLL Output Signal

Case C

The classic digital PLL was simulated to synthesize a 260MHz signal. This is a mid-range frequency. Figure 109 shows the VCO control voltage as the PLL acquires lock. Initially the PLL is outputting a 350MHz signal. The loop dynamics take over and the VCO control voltage rises to synthesize the 260MHz signal. The acquisition time is approximately 5µs. The acquisition time is short due to the frequency change being inside the lock range. Figure 110 shows the 260MHz output and frequency spectrum.

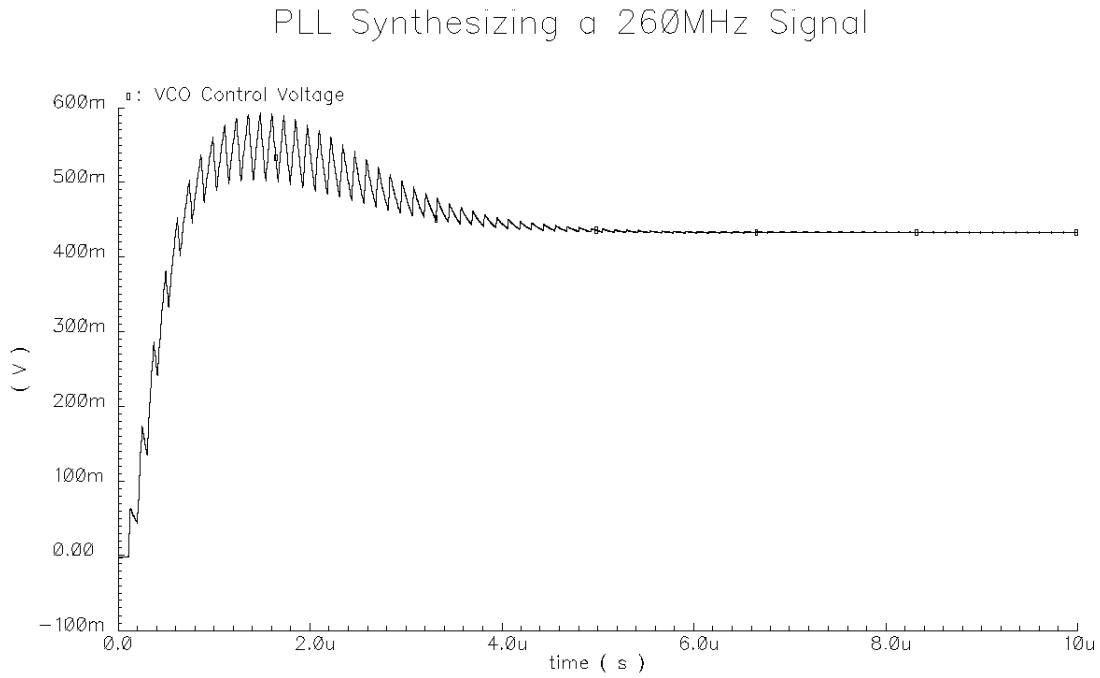

Figure 109 - VCO Control Voltage for Classic Digital PLL 260MHz Output

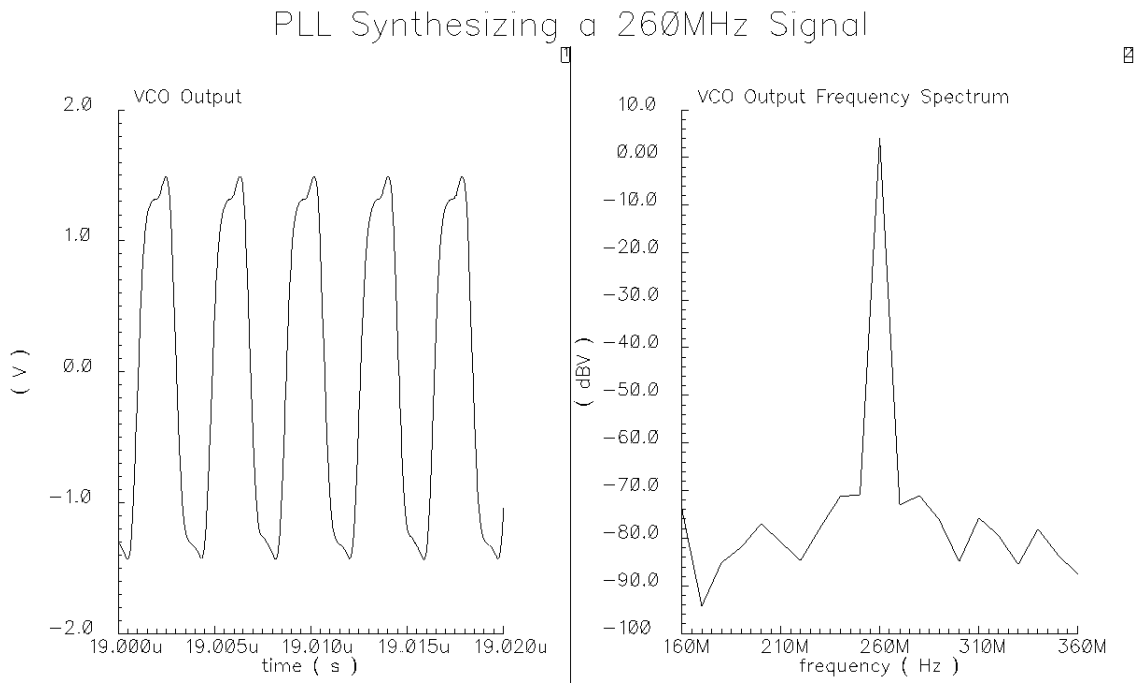

Figure 110 - 260MHz Classic Digital PLL Output Signal

Table 18 provides a comparison between the multi-band PLL and the classic digital PLL. The multi-band PLL achieved a 60% wider tuning range than the classic digital PLL. The multi-band PLL was able to achieve a wider tuning range while maintaining a lower VCO conversion gain. This allowed the switched tuning oscillator to have better phase noise performance than the oscillator that was used in the classic digital PLL. The phase noise of the PLL systems was unable to be simulated due to the high transistor count. This comparison is made through experimental results. The acquisition time depends on the region that the PLL operates in and is a strong function of the VCO conversion gain. Case A of the multi-band PLL and the classic PLL can be used to compare the acquisition time for a frequency step of 30MHz. The multi-band PLL has an acquisition time of 5µs and the classic digital PLL has an acquisition time of 10µs. However, the reason for the classic digital PLL to have a slow acquisition is because it is operating near the edge of the synthesizer's range in a region where the VCO gain is low. Case E of the multi-band PLL and case B of the classic digital PLL can be used to

compare the acquisition time for a frequency step of –120MHz. Both synthesizers have an acquisition time of 14µs. This is a pull-in process for both synthesizers, with the multi-band PLL switching down one band. Case B of the multi-band PLL and case C of the classic digital PLL can be used to compare the acquisition time for a frequency step of –90MHz. The multi-band PLL has an acquisition time of 14µs and the classic digital PLL has an acquisition time of 5µs. This is a pull-in process for the multi-band PLL and the PLL switches bands. The acquisition time is much lower for the classic digital PLL because the frequency step is within the lock range due to the large VCO conversion gain of the PLL.

Table 18 - Comparison of Multi-Band PLL and Classic Digital PLL Systems

PLL System	Frequency Range (MHz)	VCO Phase Noise (dBc/Hz @ 50kHz)	PLL System Phase Noise	Acquisition Time (µs)
Multi-Band	100 ? 340	-82.63 ? -103.7	Determined Experimentally	5 ? 19
Classic	230 ? 380	-83.74 ? -93.6	Determined Experimentally	5 ? 14

EXPERIMENTAL RESULTS

In this section the experimental results for the multi-band PLL building blocks, the multi-band PLL frequency synthesizer system, and the classic digital PLL frequency synthesizer are presented. These results are compared with mathematical and Spectre simulation results where applicable. A comparison is made between the multi-band and the classic digital PLL frequency synthesizer.

Building Block Verification

The prototype chip shown in Figure 111 contains the following multi-band PLL frequency synthesizer building blocks:

1. Phase/Frequency Detector
2. Charge Pump
3. Switched Tuning VCO
4. Switch Control State Machine
5. Comparators with Hysterisis
6. Loop Divider

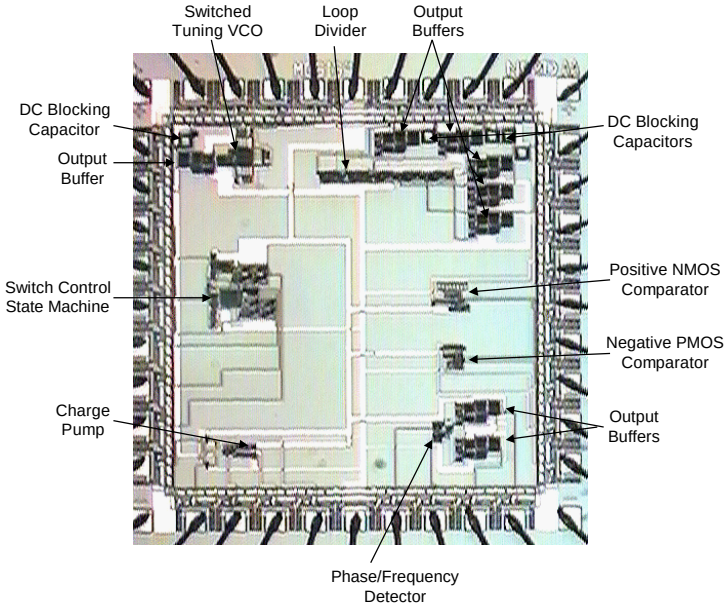

Figure 111 - Multi-Band PLL Building Blocks Prototype Chip

The characterization of these blocks outside the PLL systems provides information that is used to solve any problems encountered in the systems.

Phase/Frequency Detector

The functionality of the phase/frequency detector was verified on a high frequency test board shown in Figure 112. BNC Connectors are used on the test board for high frequency input and output signals. The test board is double-sided with a large ground plane on both sides for optimal high frequency performance. Low frequency and power signals are brought on to the board through headers. All of the multi-band PLL building blocks can be tested on the test board. Potentiometers and resistors are used to generate bias currents and reference voltage for other building blocks.

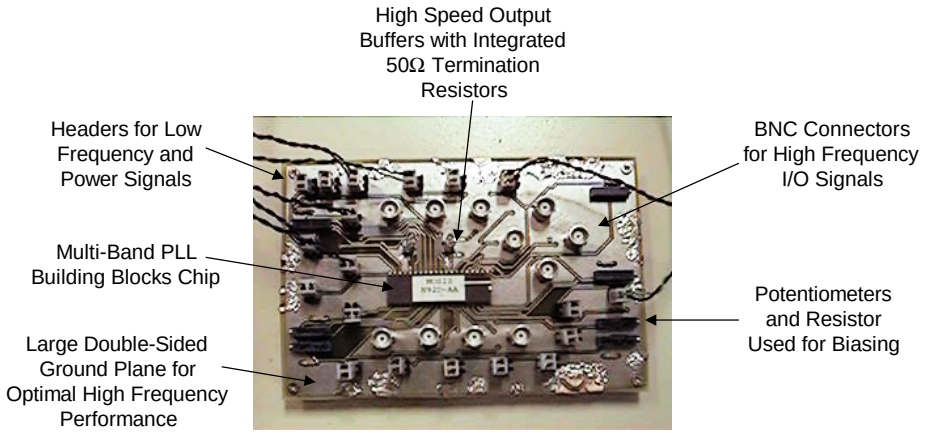

Figure 112 - Multi-Band PLL Building Blocks Test Board

A schematic diagram of the PFD is shown in Figure 61. A ±1.35V 9.375MHz square wave signal is applied to the v_{ref} input. A ±1.35V 6.25MHz square wave signal is applied to the v_{fb} input. The buffered outputs of the PFD are loaded with approximately 10pF from the HP1661CS Logic Analyzer/Oscilloscope used to measure the signals and also pin and board capacitance associated with driving the output signals outside of the chip.

The experimental results for the phase/frequency detector are shown in Figure 113. These experimental results reproduce the PFD simulation results presented in the previous section in Figure 65. A HP1661CS Logic Analyzer/Oscilloscope is used to obtain the results. After initial settling, a rising edge on the v_{ref} signal causes the *DOWN* signal to go high. The *DOWN* signal stays high until a rising edge of v_{fb} causes *UP* to go high. *UP* and *DOWN* are now both high for a short period. This causes the AND gate reset output to go high and forces *UP* and *DOWN* low. This cycle is repeated with another rising edge of v_{ref}. The overall effect of this is that with a significantly faster signal v_{ref}, the *DOWN* signal is high for a significant period of time. When the PFD is placed in the PLL system, these conditions will force the charge pump to discharge the loop filter and the VCO control voltage will drop. This will increase the VCO output's frequency and in turn the v_{fb} signal's frequency.

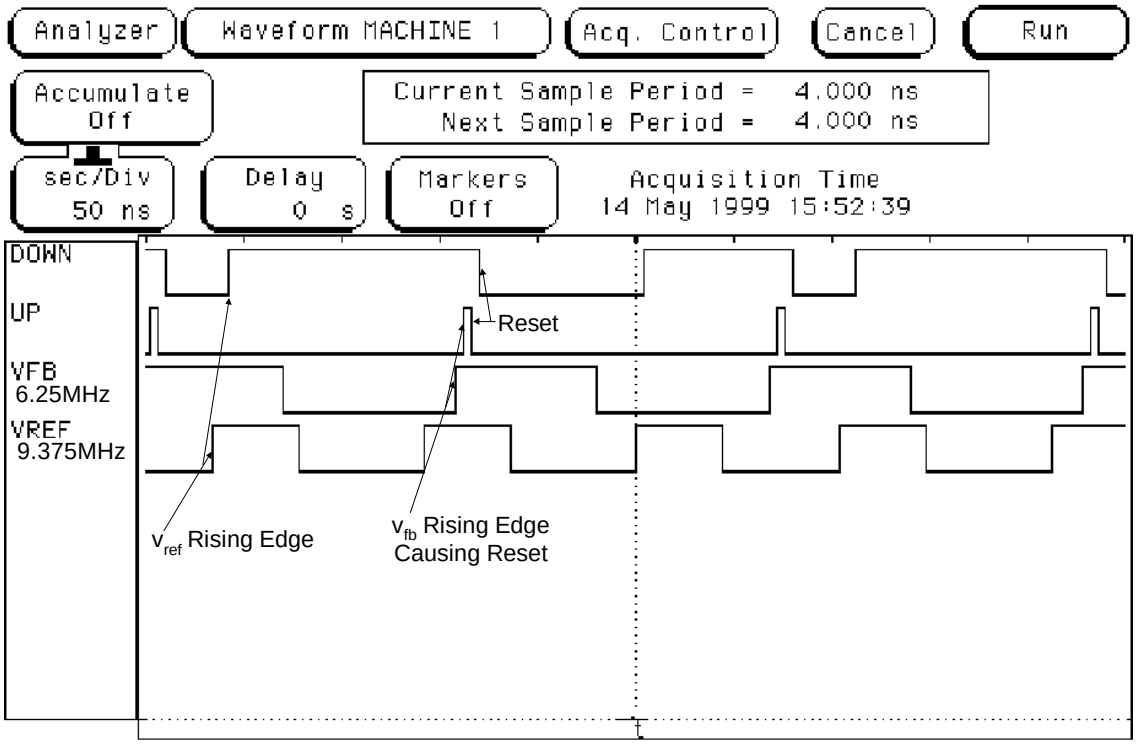

Figure 113 - Phase/Frequency Detector Experimental Results

Charge Pump

For a schematic diagram of this circuit refer to Figure 66 of the previous section. The functionality of the charge pump was verified. The verification was performed by loading the charge pump with a 10.8nF capacitor and studying the charge time to calculate the average output current. The *UP* and *DOWN* control signals are complementary ±1.35V 200Hz square waves. The charge pump positively charges the load capacitor with I_{UP} when *UP* is high and negatively charges the load capacitor with I_{DOWN} when *DOWN* is high.

The experimental results for the charge pump are shown in Figure 114 and Figure 115. The average output current is measured from the voltage slope over a ±0.8125V region with the following relation.

$$\text{Average } I_{OUT} = \frac{C\Delta V}{\Delta t} \qquad \textbf{(148)}$$

The off-chip bias currents are tweaked to yield average I_{UP} and I_{DOWN} output currents of 25µA. A bias current of 30.4µA is needed for I_{UP} and 26.3µA is needed for I_{DOWN}.

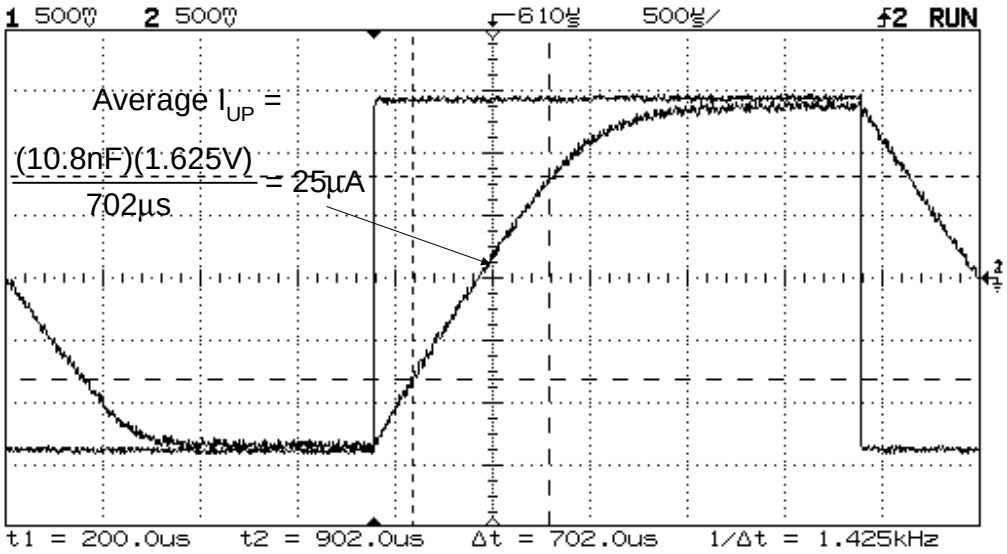

Figure 114 - Measured Average I_{UP} Output Current

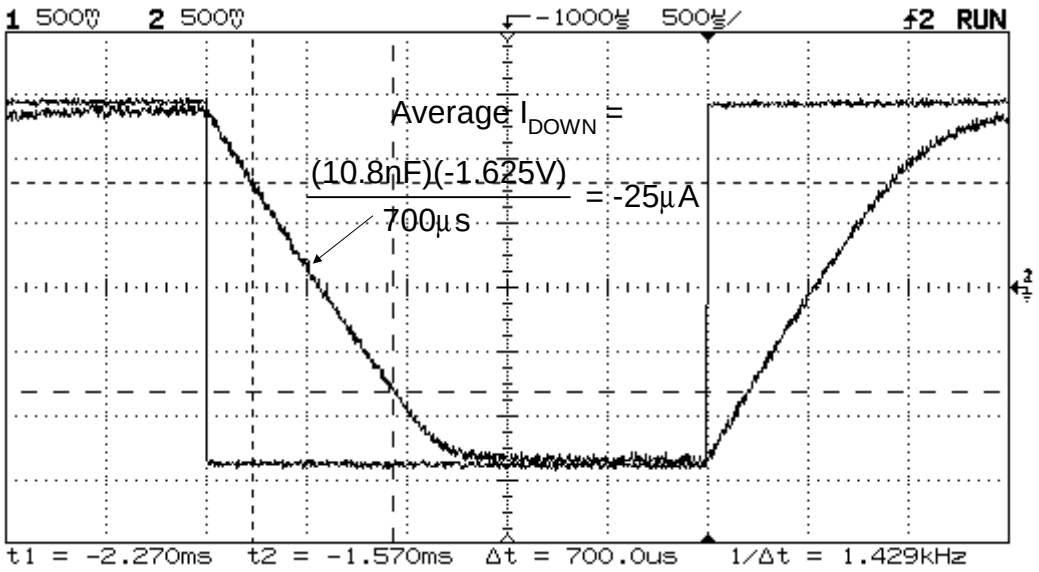

Figure 115 - Measured Average I_{DOWN} Output Current

Switched Tuning VCO

The performance of the switched tuning VCO was determined experimentally on the high frequency printed circuit board shown in Figure 112. A schematic of the switched tuning VCO is shown in Figure 72. MAXIM's MAX4201 high frequency output buffers are used in order to measure the output with a 50O input impedance Rohde & Schwartz FSEB30 Spectrum Analyzer. 50O termination resistors are integrated in the buffer chips to provide matching with the spectrum analyzer. These buffers have an input impedance of approximately 500kO in parallel with a 2pF capacitor. The VCO is not designed to drive a 50O load because the design is intended for a fully integrated multi-standard transceiver. The VCO would be driving an integrated high input impedance mixer in this application and 50O matching is not necessary. The VCO output signal on chip approximates a square wave as shown in the previous sections' simulation results. This is optimal for switching a mixer in a transceiver system[22]. However, the signal appears to be a sinusoid when driven outside the chip because of the filtering associated with the bond pad, pin, and board capacitance.

In testing the switched tunable VCO, the continuous control voltage, v_c, was swept from –0.8V to 0.8V. Digital control signals of ±1.35V were applied to the discrete control signals $D1-D3$. The minimum VCO output frequency is 111MHz. The VCO oscillates at 111MHz when the continuous control voltage, v_c, is at 0.8V and the three digital control signals, $D1-D3$ are all high. The output signal measured with the HP1661CS Logic Analyzer/Oscilloscope is shown in Figure 116. The output frequency spectrum obtained with the Rohde & Schwartz FSEB30 Spectrum Analyzer is shown in Figure 117. The output signal phase noise is –84.33dBc/Hz at a 50kHz offset.

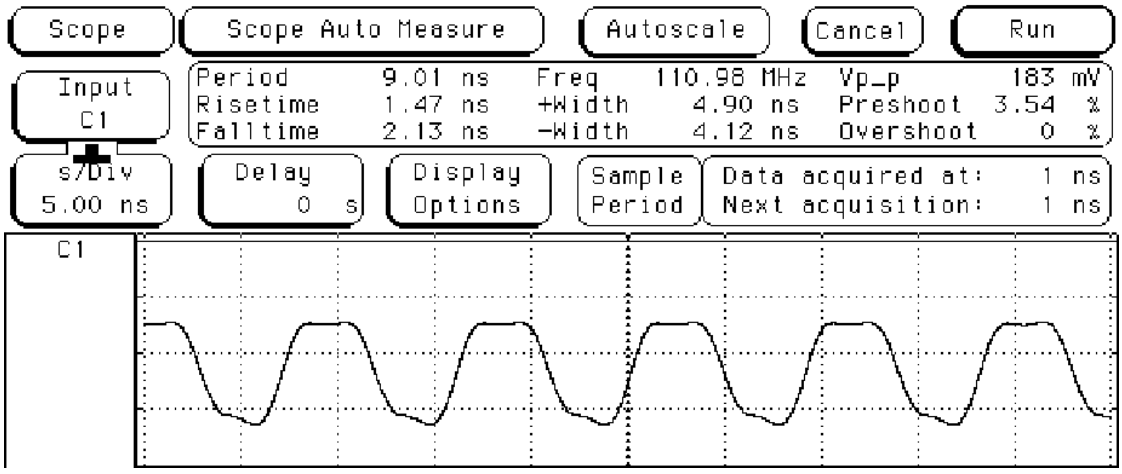

Figure 116 - Minimum Frequency VCO Output

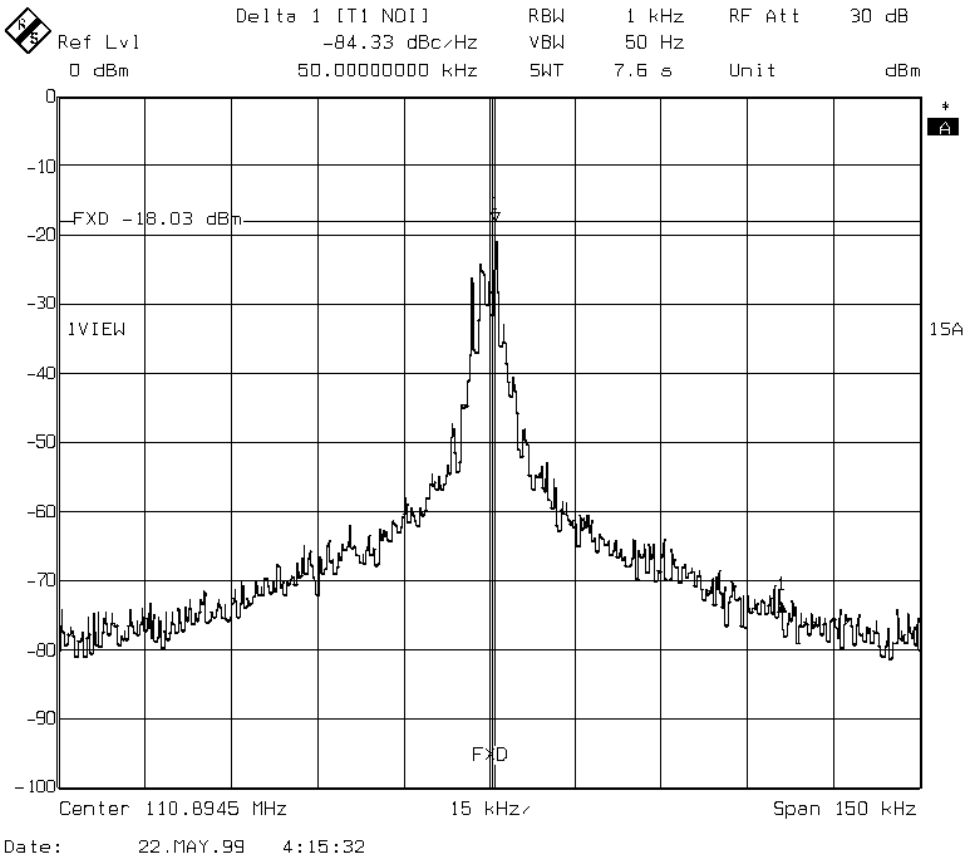

Figure 117 - Minimum Frequency VCO Output Frequency Spectrum

The maximum measured VCO output frequency is 297MHz. The VCO oscillates at 297MHz when the continuous control voltage, v_c, is at -0.8V and the three digital control signals, $D1-D3$ are all low. The output signal measured with the oscilloscope is shown in Figure 118. The output frequency spectrum obtained with the spectrum analyzer is shown in Figure 119. The output signal phase noise is –71.84dBc/Hz at a 50kHz offset.

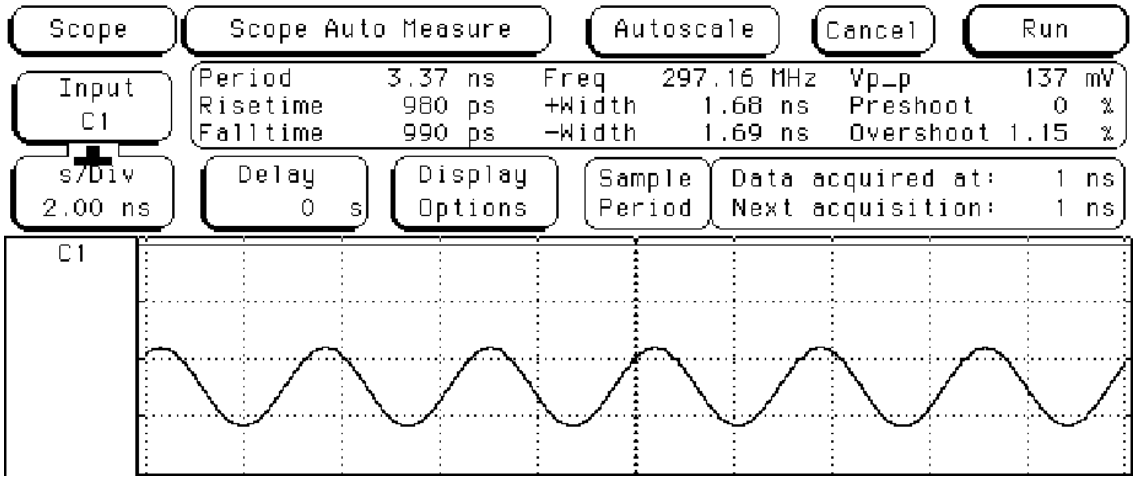

Figure 118 - Maximum Frequency VCO Output

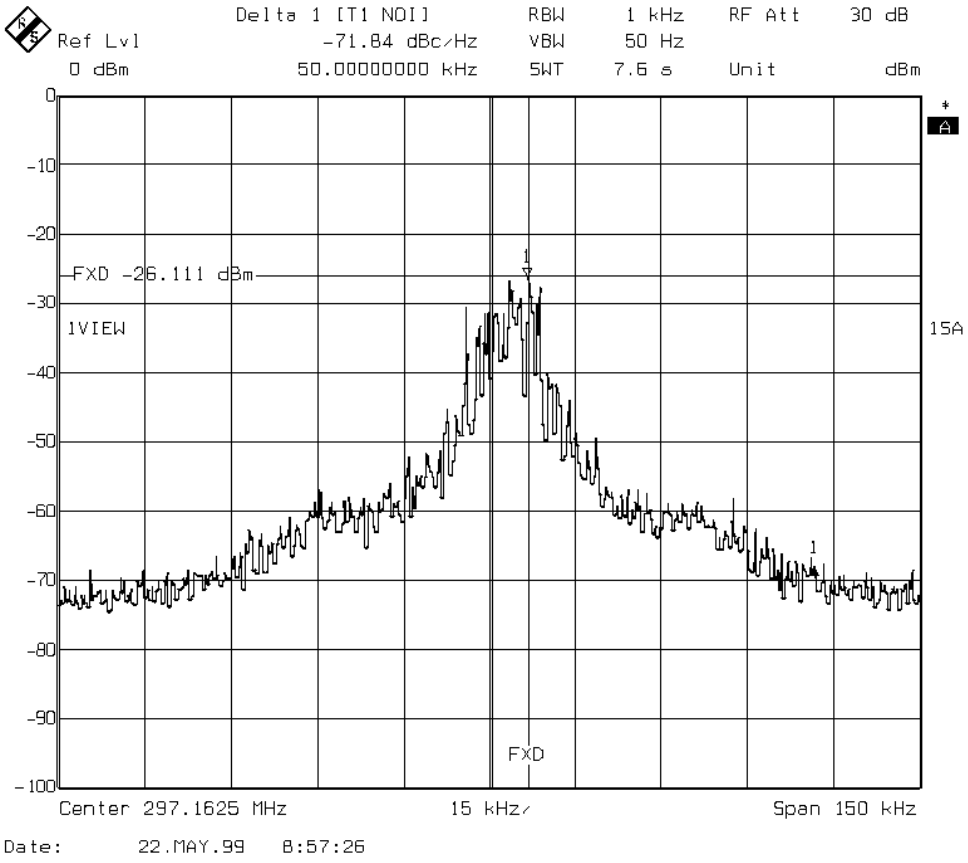

Figure 119 - Maximum Frequency VCO Output Frequency Spectrum

The switched tuning VCO's frequency response over the different bands of operation is given in Table 19. The transfer curves of the switched tuning VCO are shown in Figure 120. Note the high phase noise values for the switched tuning VCO. These high phase noise values occur when the VCO is synthesizing a mid-band frequency where the conversion gain, K_{VCO}, is highest. The high mid-band conversion gain degrades the phase noise performance. Figure 121 shows a mid-band frequency of 208MHz. The VCO oscillates at 208MHz when the continuous VCO control, v_c, is at -0.2V, the digital control signal $D1$ is high, and $D2 - D3$ are low. The output frequency spectrum obtained with the spectrum analyzer is shown in Figure 122. The output signal phase noise is -60.3dBc/Hz at a 50kHz offset.

Table 19 - Experimental Switched Tuning VCO Performance

Band	Description	Frequency Range (MHz)	Phase Noise @ 50kHz Offset (dBc/Hz)
1	All Switches Closed	111 – 149	-69.2 ? -86.91
2	2 Switches Closed	129 – 181	-64.05 ? -81.99
3	1 Switch Closed	155 – 228	-60.3 ? -77.87
4	All Switches Open	193 – 297	-65.52 ? -78.09

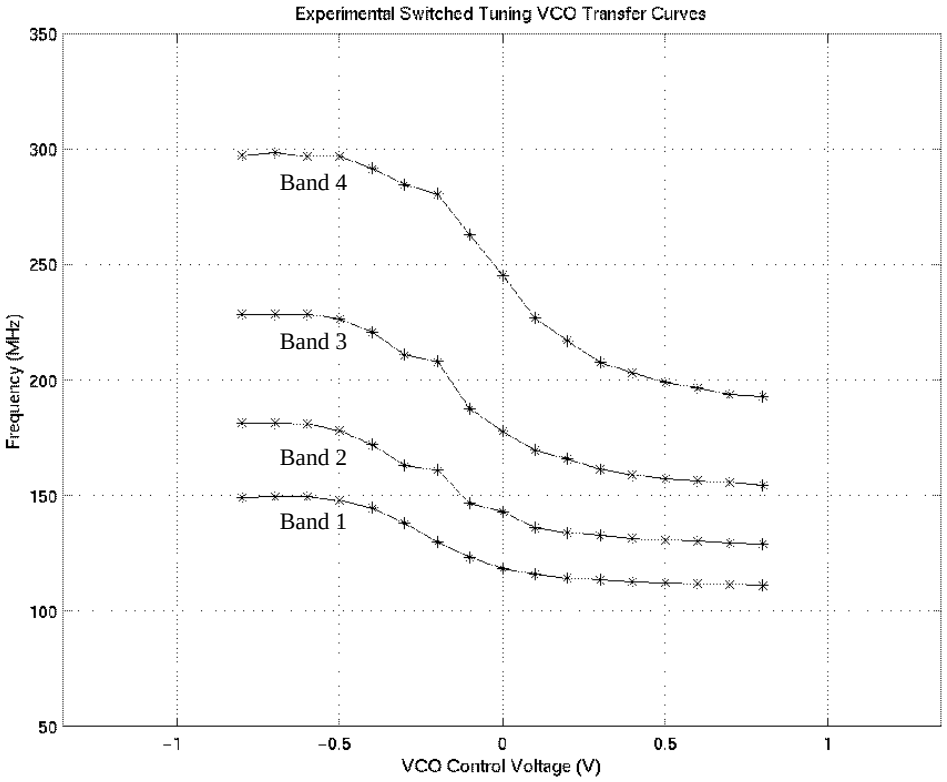

Figure 120 - Experimental Switched Tuning VCO Transfer Curves

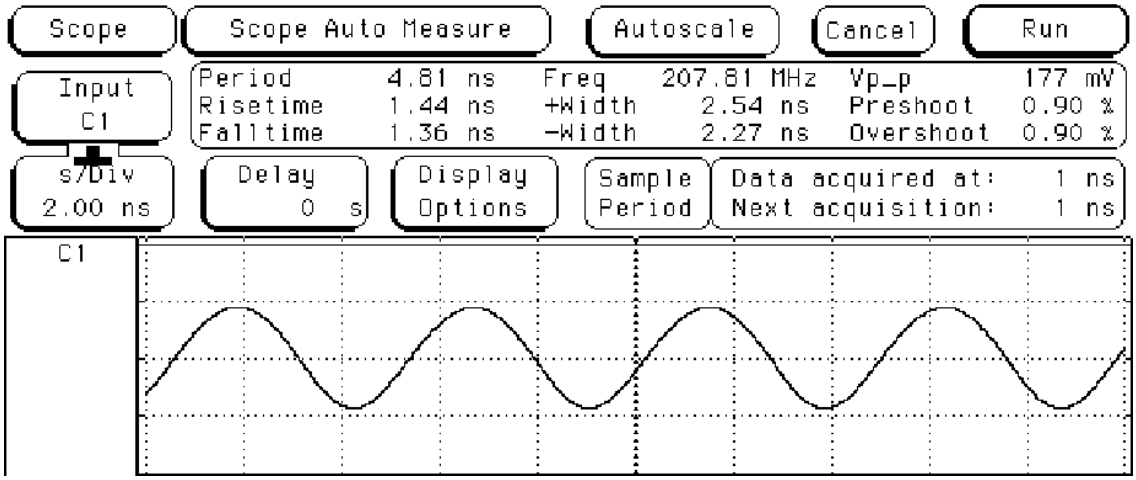

Figure 121 - Mid-Band Frequency VCO Output

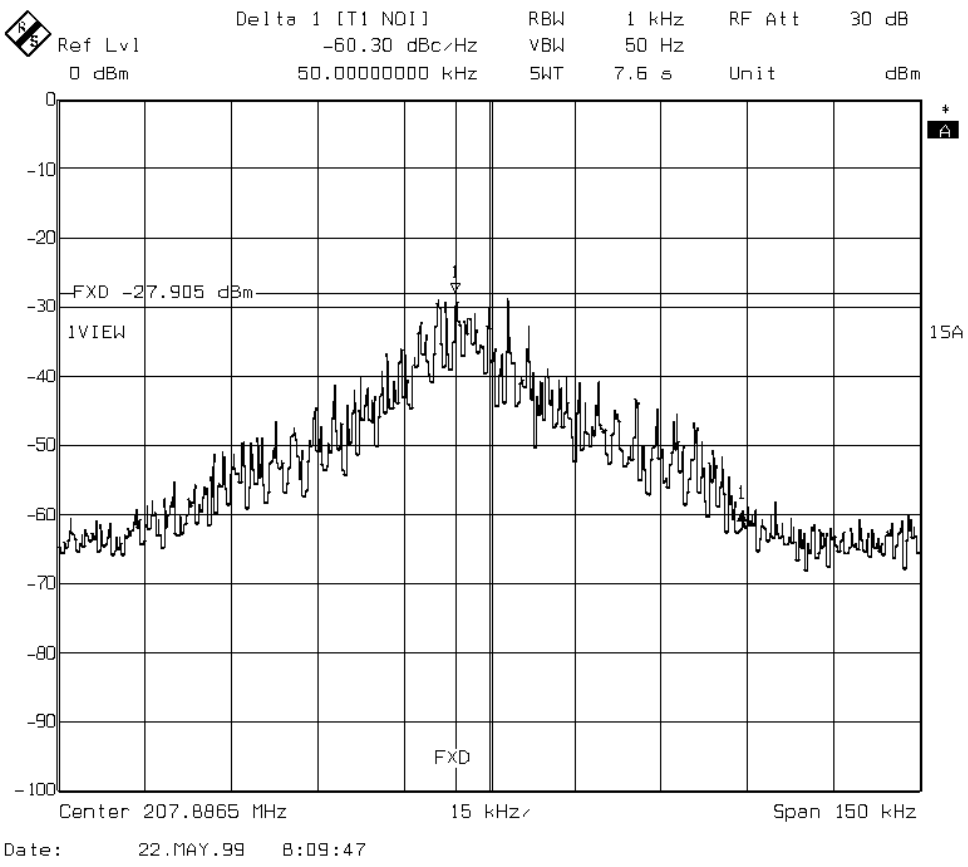

Figure 122 - Mid-Band Frequency VCO Output Frequency Spectrum

The switched tuning VCO frequency range of 111-297MHz will only allow the multi-band PLL system to synthesize 93% of the desired 100-300MHz. The multi-band PLL will not be able to lock on the low and high frequency extremes because the switched tuning VCO cannot oscillate at these frequencies.

Switch Control State Machine

The functionality of the switch control state machine was verified as well; the corresponding schematic diagram is shown in Figure 81. A ±1.35V 100kHz square wave is applied to the *CLK* input. The *UP* and *DOWN* signals are ±1.35V 10kHz

non-overlapping square waves generated from a single ±2.5V 10kHz square wave with the following circuit shown in Figure 123.

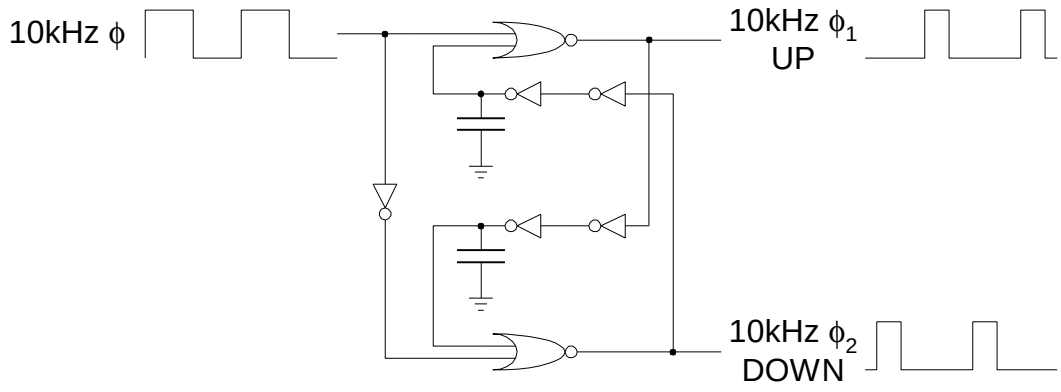

Figure 123 - Non-Overlapping Clock Circuit

The TTL outputs are scaled down to approximately ±1.35V square wave signals with voltage dividers. The 10kHz inputs allow all of the states of the state machine to be observed with a 100kHz clock input.

The experimental results for the switch control state machine are shown in Figure 124. The results were obtained with the HP1661CS Logic Analyzer/Oscilloscope. The state machine is initially in state A when the $D1$ - $D3$ outputs are high. The UP input then goes high and the state machine cycles from state A to state D after the circuit is clocked three times. UP then goes low and $DOWN$ becomes high. The state machine cycles from state D to state A after the circuit is clocked three times.

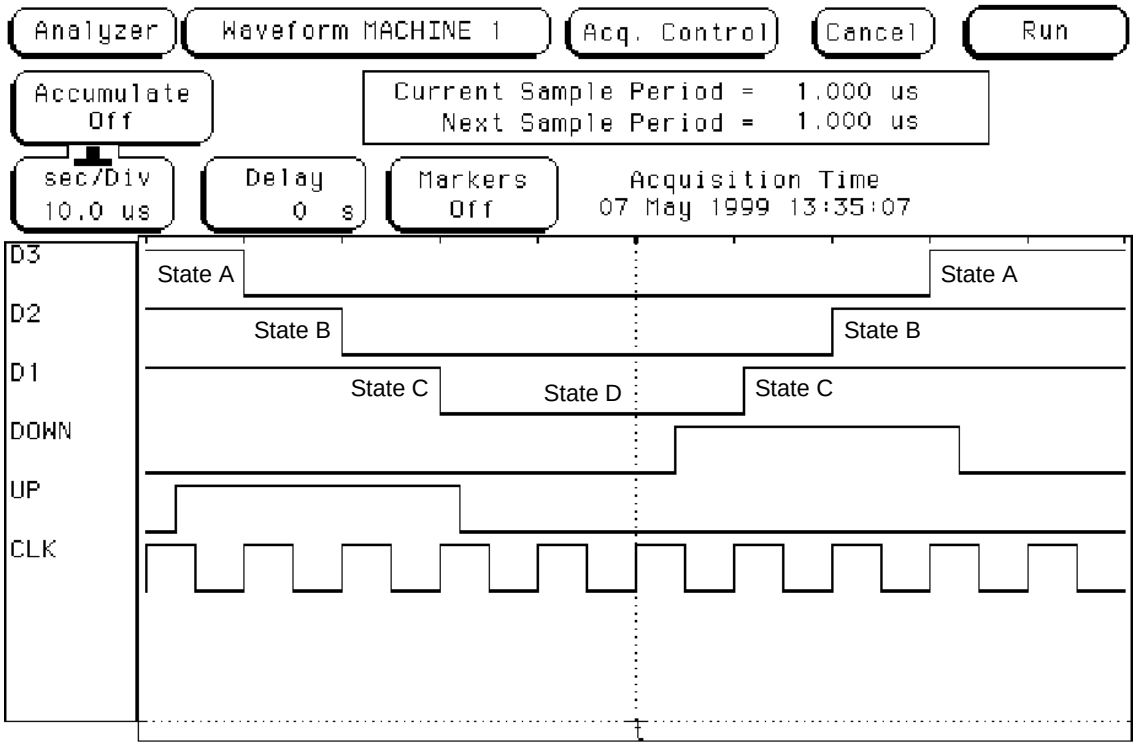

Figure 124 - Switch Control State Machine Experimental Results

Comparators with Hysterisis

Refer to Figure 83 and Figure 84 for the schematics of the comparators. An 800mV reference signal was placed at the negative input terminal of the positive NMOS comparator and a –800mV reference signal was placed at the positive input terminal of the negative PMOS comparator. A rail-to-rail $2.7V_{pp}$ 1kHz triangle wave input signal, v_{in}, was applied to the positive terminal of the positive NMOS comparator and the negative terminal of the negative PMOS comparator.

The NMOS comparator experimental transfer characteristic is shown in Figure 125. This transfer characteristic was obtained with the XY function of the oscilloscope and is a plot of v_{out} versus v_{in}. The output is low when the input signal is below the 800mV reference signal. The output is high when the input signal is above the 800mV reference

signal. Two trip points are observed due to the hysterisis. The rising input signal must pass the 800mV reference signal to approximately 990mV before the output goes high. The falling input signal must fall below 800mV to approximately 635mV before the output signal goes high. This amount of hysterisis satisfies the required minimum of 100mV due to the VCO control voltage ripple. The output levels are ±1.35V as expected due to the clamping in the comparator.

Positive NMOS Comparator with Hysterisis Measurement Results
V_{REF} = 0.8V

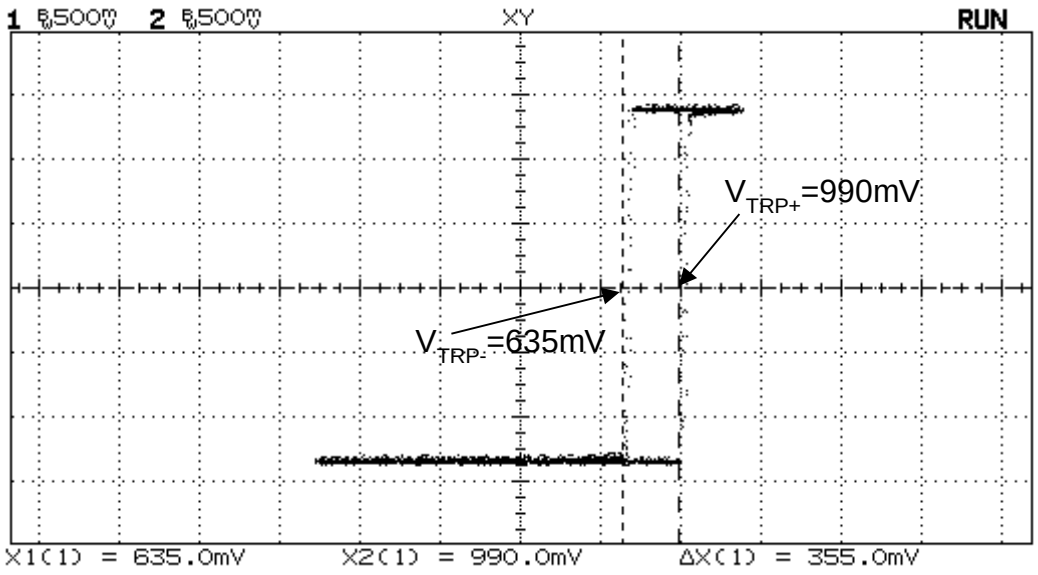

Figure 125 - Positive NMOS Comparator with Hysterisis Measurement Results

The PMOS comparator experimental transfer characteristic is shown in Figure 126. This transfer characteristic was obtained with the XY function of the oscilloscope and is a plot of v_{out} versus v_{in}. The output is high when the input signal is below the -800mV reference signal. The output is low when the input signal is above the -800mV reference signal. Two trip points are observed due to the hysterisis. The falling input signal must pass the -800mV reference signal to approximately –1.02V before the output goes high.

The rising input signal must rise above the -800mV to approximately -470mV before the output signal goes low. This amount of hysterisis satisfies the required minimum of 100mV due to the VCO control voltage ripple. The output levels are ±1.35V as expected due to the clamping in the comparator.

Negative PMOS Comparator with Hysterisis Measurement Results
V_{REF} = -0.8V

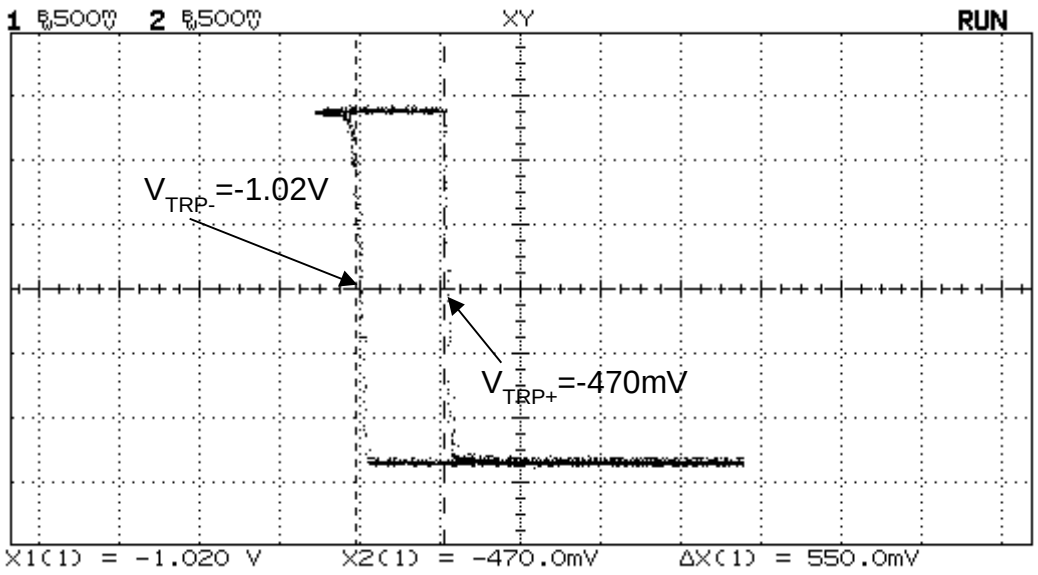

Figure 126 - Negative PMOS Comparator with Hysterisis Measurement Results

Loop Divider

The performance of the loop divider was determined experimentally on a high frequency printed circuit board shown earlier in Figure 112. A $2.7V_{pp}$ sine wave was applied to the input of the loop divider. The actual shape of the input signal in the PLL systems would be a square wave. However, due to the unavailability of a high frequency square wave generator, a sine wave is used. This difference in the input signal shape has little effect on the loop divider performance. The input signal frequency was swept to determine the loop divider frequency range.

The loop divider has a measured frequency range of 110-510MHz. Figure 127 shows the loop divider operating at 510MHz. The bottom signal is the 510MHz input signal. The 1Gsample/s HP1661CS Logic Analyzer/Oscilloscope has problems displaying this signal. The top signal is the divide-by-32 15.9375MHz output signal.

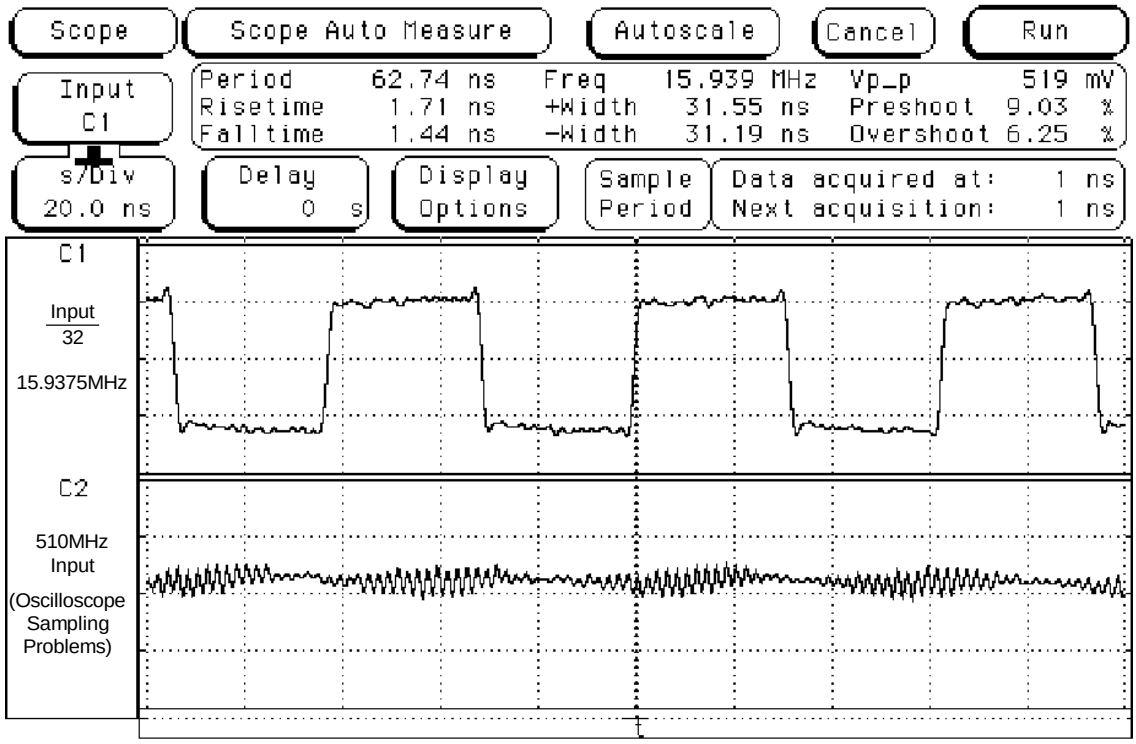

Figure 127 - Loop Divider Operating at 510MHz

Figure 128 shows the loop divider operating at 110MHz. The bottom signal is the 110MHz signal. The top signal is the divider-by-32 3.4375MHz output signal.

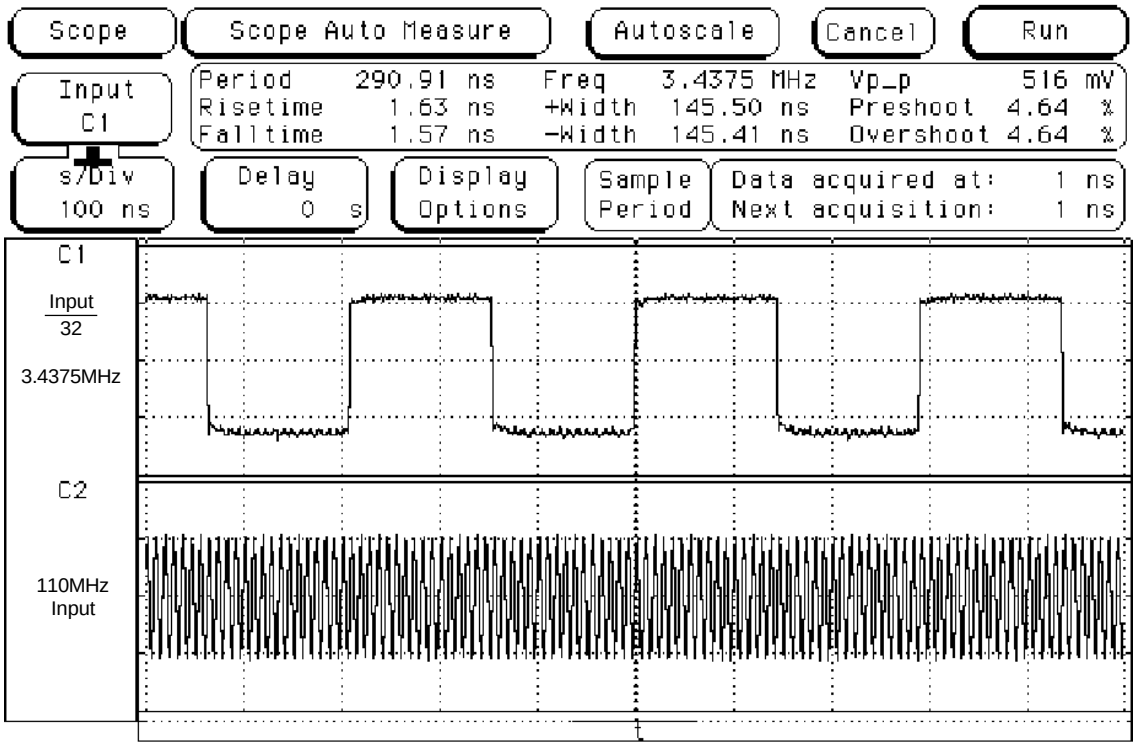

Figure 128 - Loop Divider Operating at 110MHz

The loop divider fails for frequencies under 110MHz. The second flip-flop in the divider fails to divide by two at low frequencies and the loop divider only divides by 16. The inability of the flip-flop to operate at frequencies below 110MHz will cause the PLL systems to fail when attempting to synthesize frequencies below 110MHz. This is because when the VCO output frequency drops below 110MHz the loop will now multiply the input frequency by 16 instead of 32. The VCO will not be able to synthesize this low frequency and the loop will not lock. An example of this constraint is attempting to synthesize 100MHz. The input frequency will be 3.125MHz. The loop will attempt to synthesize 100MHz until the VCO output frequency drops below 110MHz. Then the division factor will be 16 and the loop will attempt to synthesize 50MHz. However, the limited VCO frequency range will not allow it to lock on a 50MHz signal.

Multi-Band PLL Frequency Synthesizer

The prototype chip shown in Figure 129 contains the multi-band PLL frequency synthesizer.

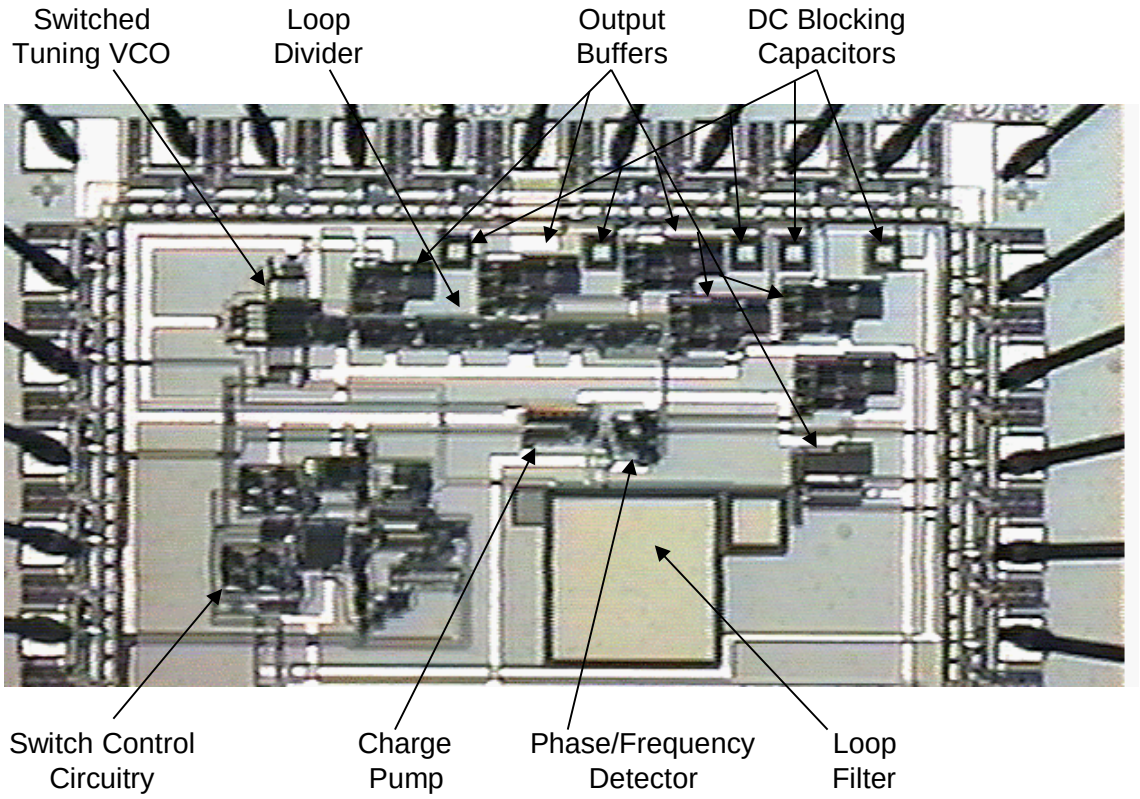

Figure 129 - Multi-Band PLL Frequency Synthesizer Prototype Chip

The multi-band PLL frequency synthesizer was characterized to determine the frequency range and phase noise performance on a high frequency test board shown in Figure 130.

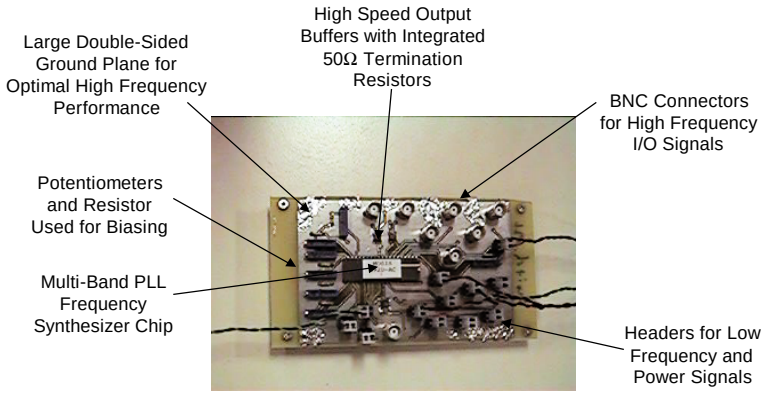

Figure 130 - Multi-Band PLL Frequency Synthesizer Test Board

The test cases presented in the previous section are reproduced experimentally to illustrate the multi-band PLL frequency synthesizer performance. Table 20 summarizes the setup for each case. The frequencies have been adjusted from the previous section to comply with the measured multi-band PLL regions.

Table 20 - Multi-Band PLL Frequency Synthesizer Experimental Case Studies

Case	Initial Frequency	Final Frequency	? f	Experiment Type	Acquisition Time
A	240MHz	270MHz	30MHz	Mid-Band	4.5µs
B	240MHz	190MHz	-50MHz	Mid-Band (Band Change)	8.56µs
C	240MHz	111MHz	-129MHz	Lowest Edge-of-Band	17.024µs
D	240MHz	290MHz	50MHz	Highest Edge-of-Band	16.036µs
E	240MHz	160MHz	-80MHz	Overlap	8.024µs

In all cases the multi-band PLL is initially operating in the mid-band region of band 4 at a frequency of 240MHz. The initial output signal measured with an oscilloscope is shown in Figure 131. The initial output frequency spectrum is shown in Figure 132. The initial output signal phase noise is –90.83dBc/Hz at a 50kHz offset.

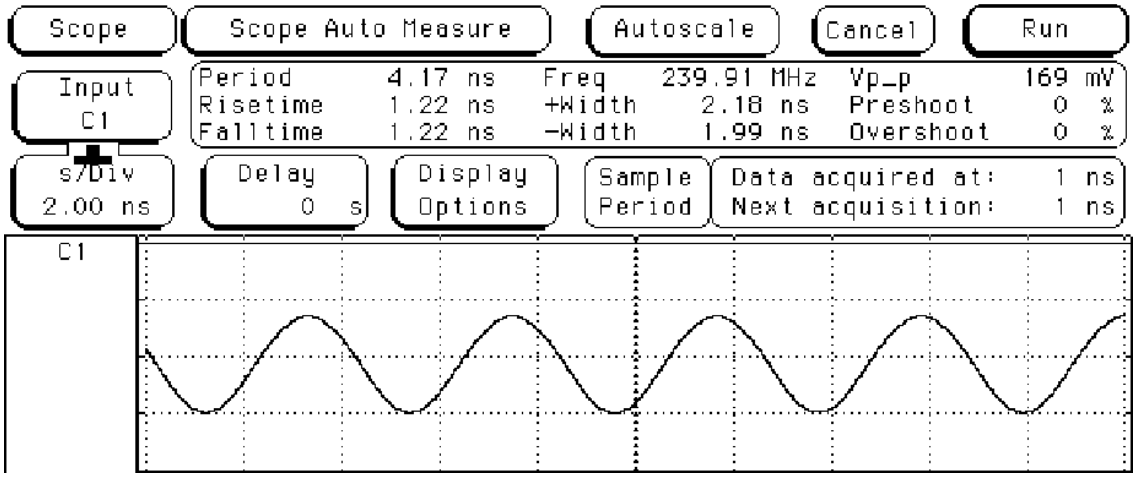

Figure 131 - Initial Experimental 240MHz Multi-Band PLL Output Signal

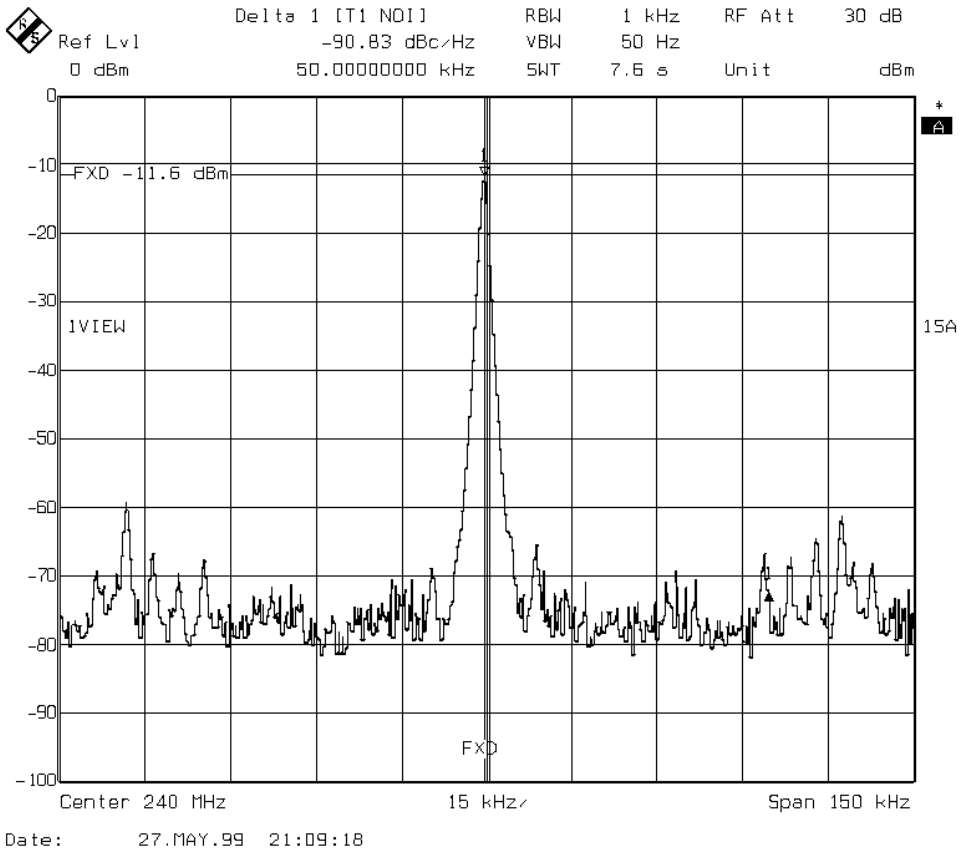

Figure 132 - Initial Experimental 240MHz Multi-Band PLL Output Frequency Spectrum

Case A

The first experimental result presented shows the multi-band PLL synthesizing a 270MHz signal. This illustrates a situation where a mid-band frequency in the current band is being synthesized. Figure 133 shows the continuous VCO control voltage. All three digital VCO control signals are initially low which means the multi-band PLL is in the correct band of operation. The PLL was previously locked on a 240MHz signal. This corresponds to a VCO control voltage of approximately 35mV in band 4. The VCO control voltage then tunes down to approximately -.143V to synthesize 270MHz. The measured acquisition time is 4.5µs. This acquisition time is low because the frequency change is within the lock range. The output signal measured with the oscilloscope is shown in Figure 134. The output frequency spectrum obtained with the spectrum analyzer is shown in Figure 135. The output signal phase noise is –96.14dBc/Hz at a 50kHz offset.

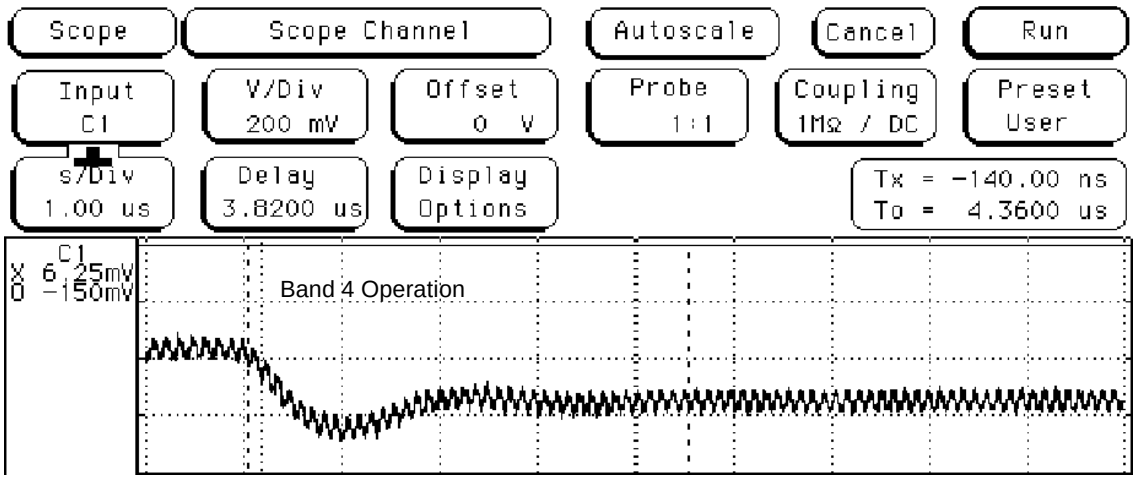

Figure 133 - Continuous VCO Control Voltage for Multi-Band PLL 270MHz Output

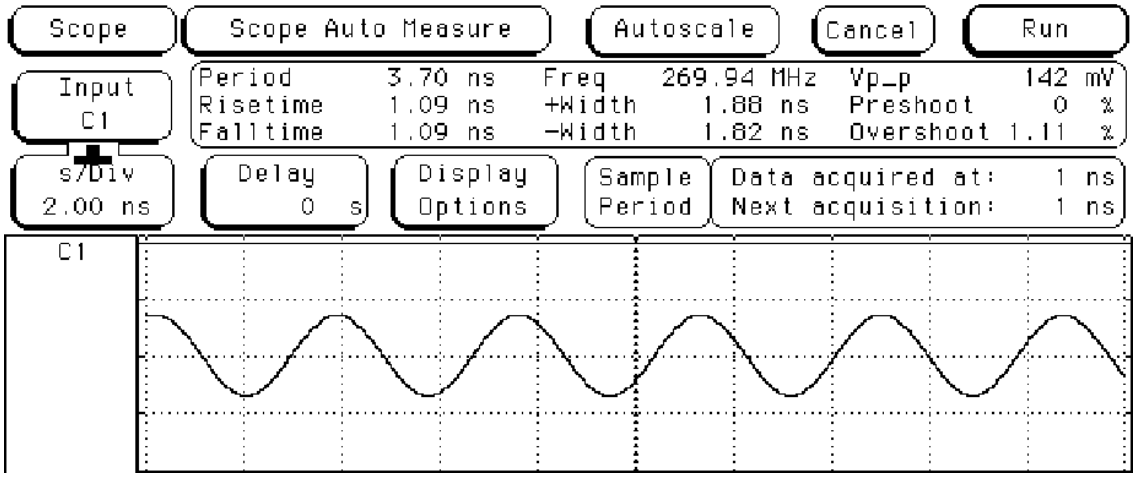

Figure 134 - Experimental 270MHz Multi-Band PLL Output Signal

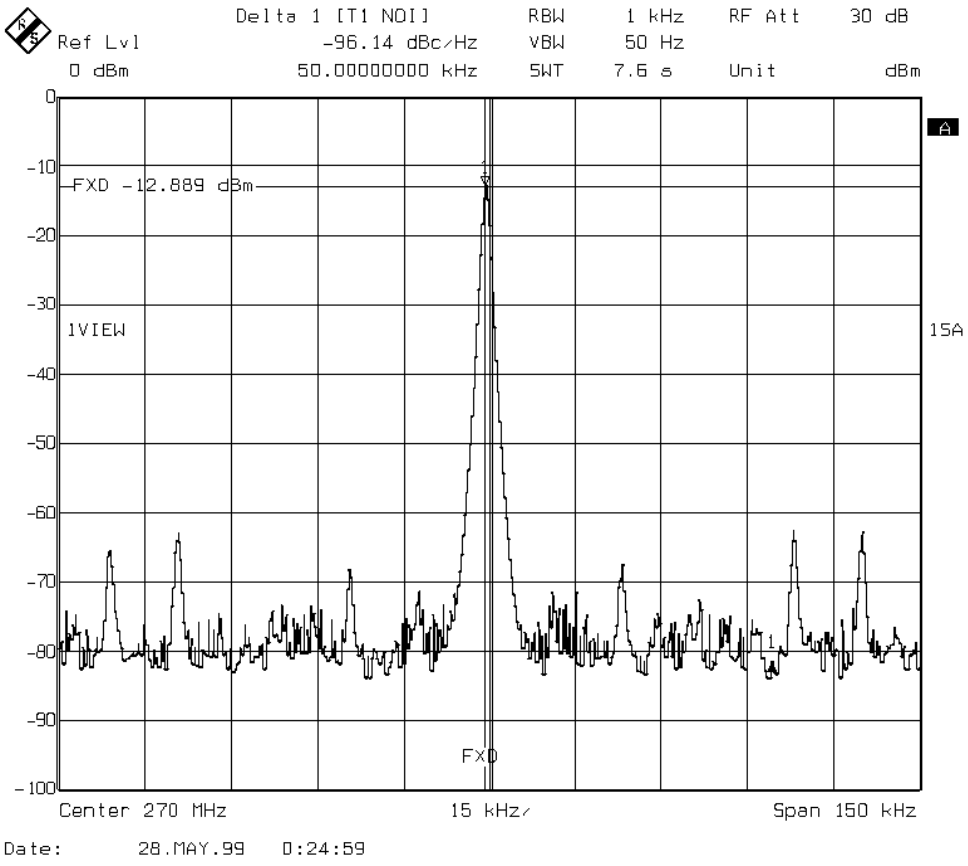

Figure 135 - Experimental 270MHz Multi-Band PLL Output Frequency Spectrum

Case B

The second experimental result presented shows the multi-band PLL synthesizing a 190MHz signal. This is a situation where a mid-band frequency out of the current band is being synthesized. Figure 136 shows the continuous VCO control voltage. All three digital control signals are initially low which means the multi-band PLL is not in the correct band of operation. The multi-band PLL was previously locked on a 240MHz signal. This corresponds to a VCO control voltage of approximately 35mV in band 4. The VCO control voltage then tunes up and switches to band 3 where it settles to –92mV to synthesize 190MHz. The measured acquisition time is 8.56µs. This acquisition time is longer because the frequency change is outside the lock range and the acquisition process becomes a pull-in process. The output signal measured with the oscilloscope is shown in Figure 137. The output frequency spectrum obtained with the spectrum analyzer is shown in Figure 138. The output signal phase noise is –92.76dBc/Hz at a 50kHz offset.

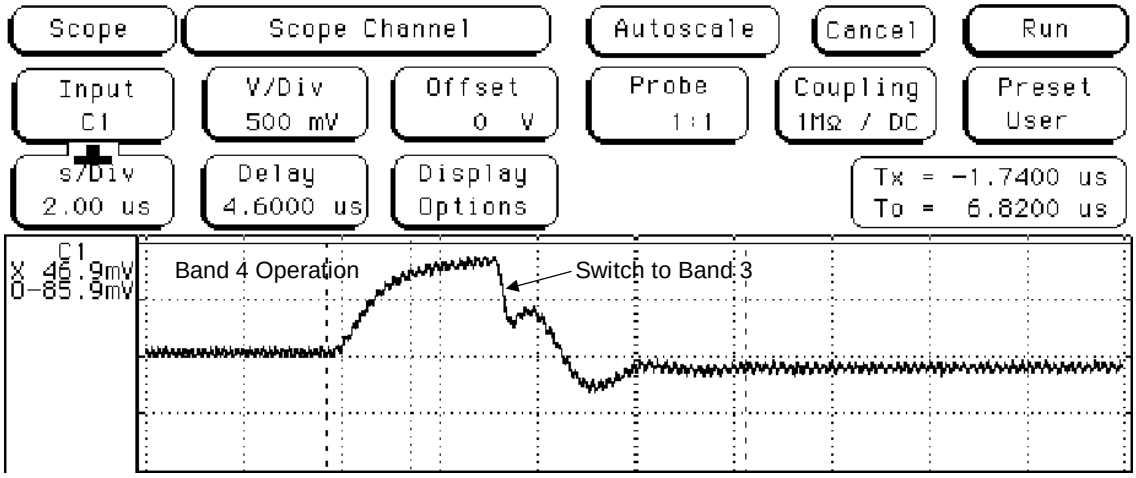

Figure 136 - Continuous VCO Control Voltage for Multi-Band PLL 190MHz Output

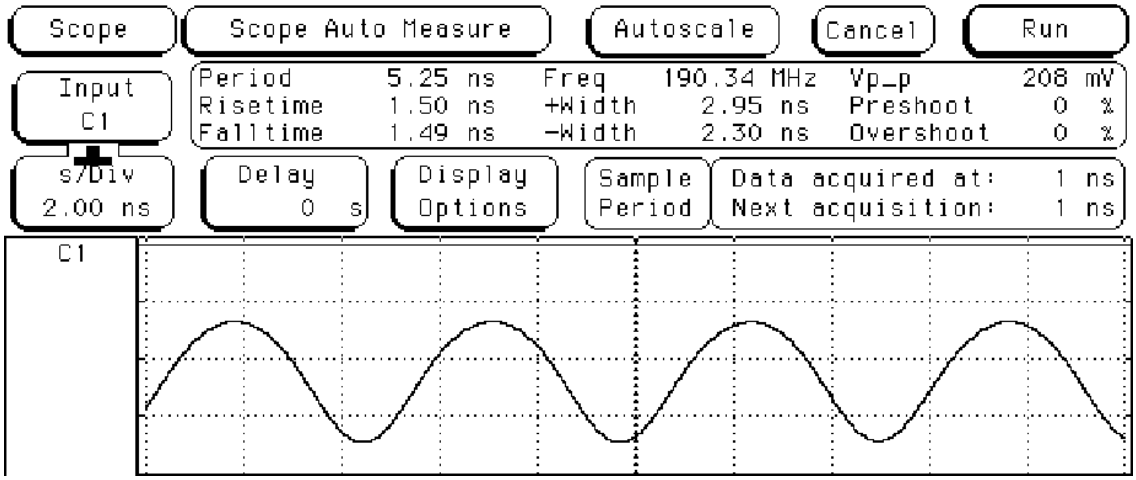

Figure 137 - Experimental 190MHz Multi-Band PLL Output Signal

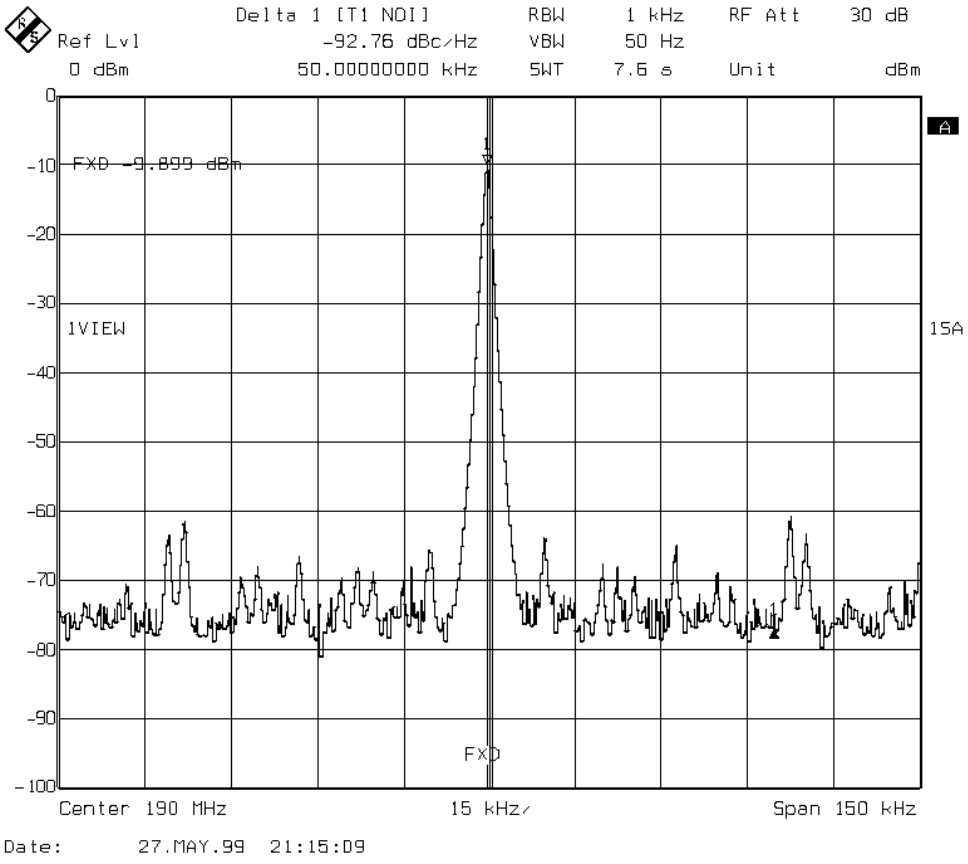

Figure 138 - Experimental 190MHz Multi-Band PLL Output Frequency Spectrum

Case C

The third experimental result presented shows the multi-band PLL synthesizing a 111MHz signal. This illustrates a situation in which a signal close to the lowest edge-of-band frequency is being synthesized. Figure 139 shows the continuous VCO control voltage. All three digital control signals are initially low which means the multi-band PLL is not in the correct band of operation. The multi-band PLL was previously locked on a 240MHz signal. This corresponds to a VCO control voltage of approximately 35mV in band 4. The VCO control voltage then tunes up and switches from band 4 through band 3 and 2 and finally settles in band 1 at approximately 0.295V to synthesize 111MHz. The measured acquisition time is 17.024µs. This acquisition time is longer because the frequency change is outside the lock range and the acquisition process becomes a pull-in process. The output signal measured with the oscilloscope is shown in Figure 140. The output frequency spectrum obtained with the spectrum analyzer is shown in Figure 141. The output signal phase noise is –87.68dBc/Hz at a 50kHz offset.

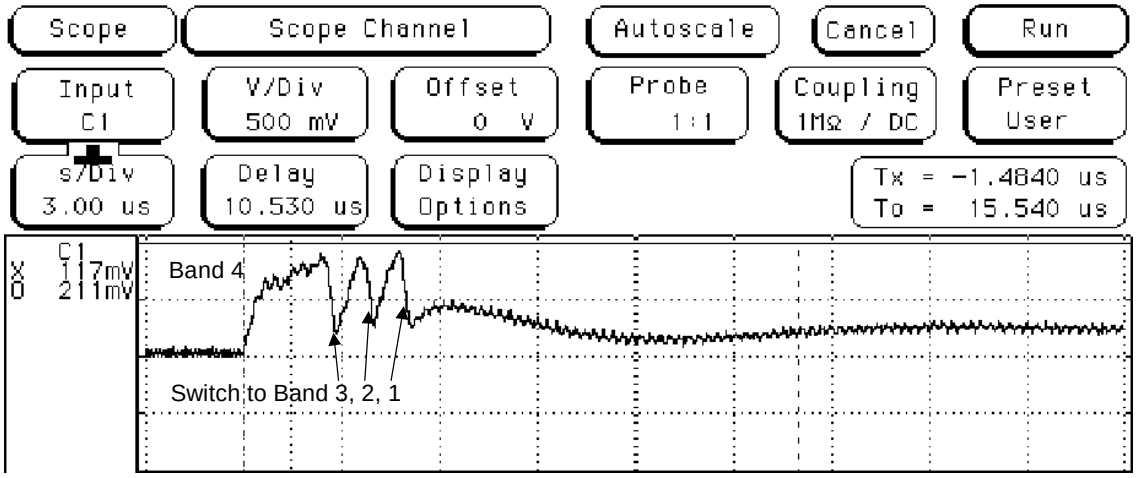

Figure 139 - Continuous VCO Control Voltage for Multi-Band PLL 111MHz Output

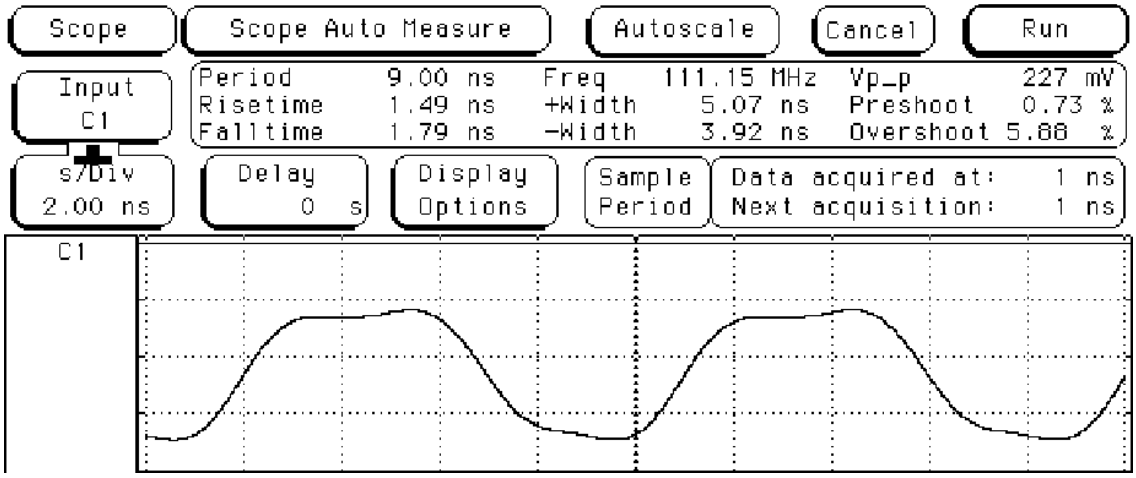

Figure 140 - Experimental 111MHz Multi-Band PLL Output Signal

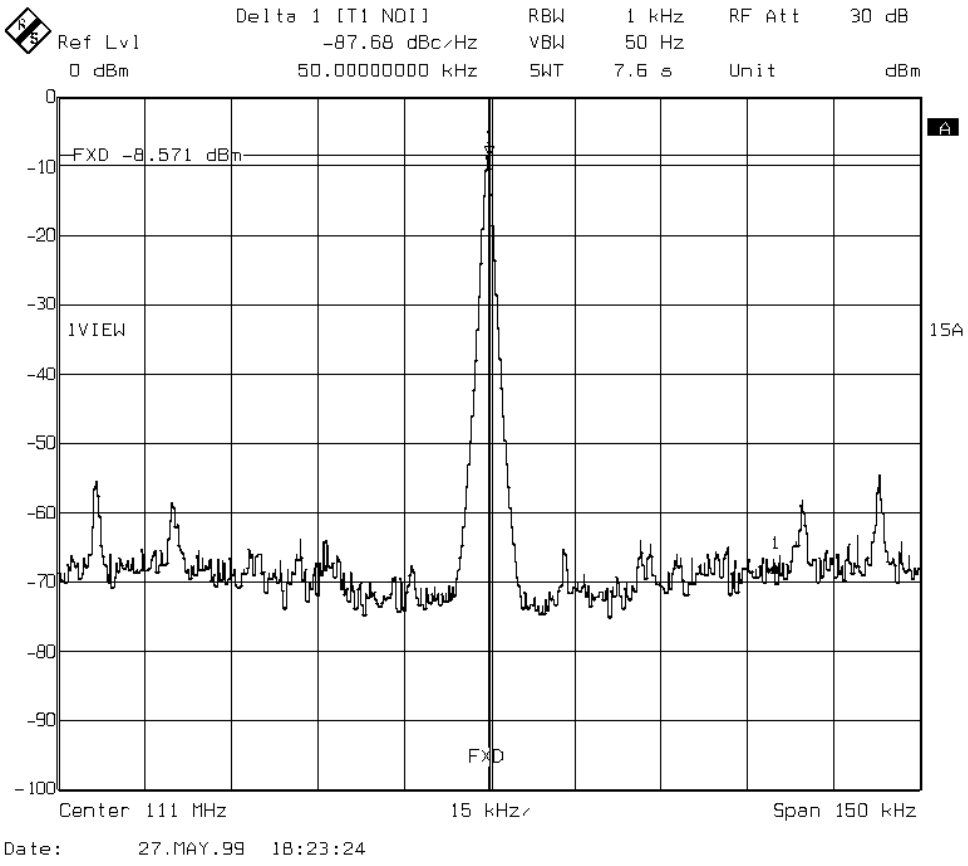

Figure 141 - Experimental 111MHz Multi-Band PLL Output Frequency Spectrum

The multi-band PLL cannot lock on frequencies much lower than 111MHz. Figure 142 shows the multi-band PLL output frequency spectrum when it is synthesizing a 110MHz signal. Notice the high spurious signals at equal offsets of the fundamental. This is from the multi-band PLL being on the edge of its frequency range.

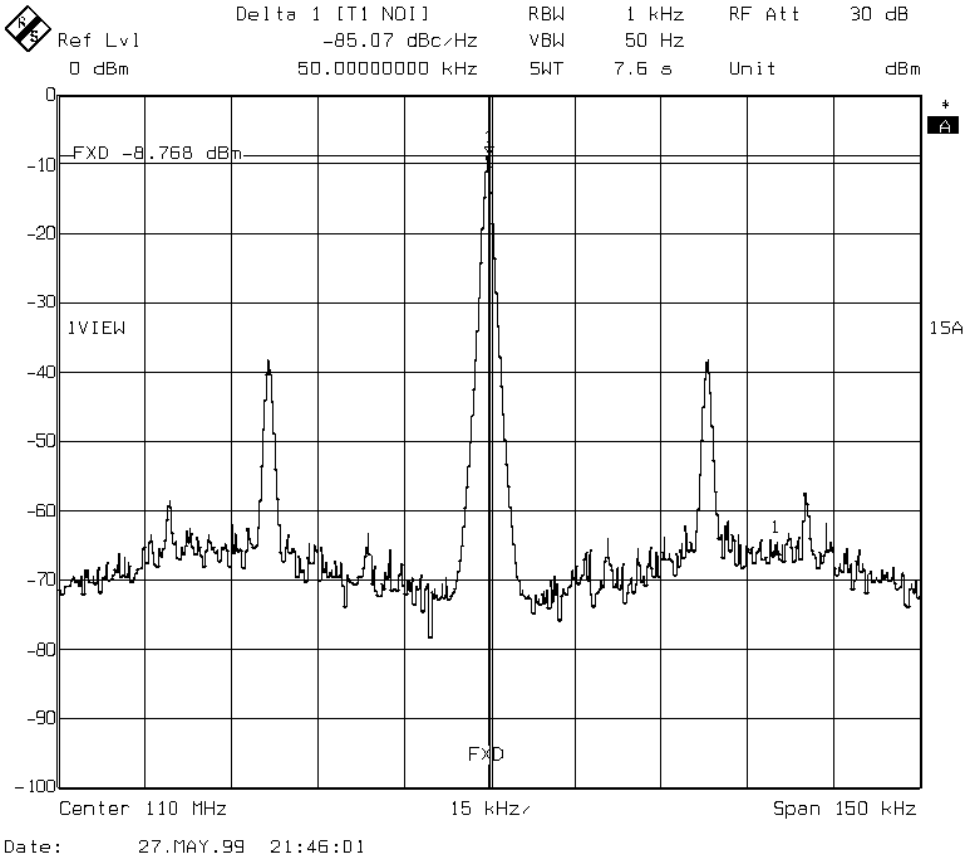

Figure 142 - Experimental 110MHz Multi-Band PLL Output Frequency Spectrum

Case D

The fourth experimental result presented shows the multi-band PLL synthesizing a 290MHz signal. This illustrates a situation in which a signal close to the highest edge-of-band frequency is being synthesized. Figure 143 shows the continuous VCO control voltage. All three digital control signals are initially low which means the multi-band PLL is in the correct band of operation. The multi-band PLL was previously locked on a

240MHz signal. This corresponds to a VCO control voltage of approximately 35mV in band 4. The VCO control voltage then tunes down and unnecessarily triggers the switch control mechanism due to operating at the edge of the synthesizer's range. The control voltage finally settles to -.459V to synthesize 290MHz. The measured acquisition time is 16.036µs. This acquisition time is longer because the frequency change is outside the lock range and the acquisition process becomes a pull-in process. The output signal measured with the oscilloscope is shown in Figure 144. The output frequency spectrum obtained with the spectrum analyzer is shown in Figure 145. The output signal phase noise is –89.97dBc/Hz at a 50kHz offset.

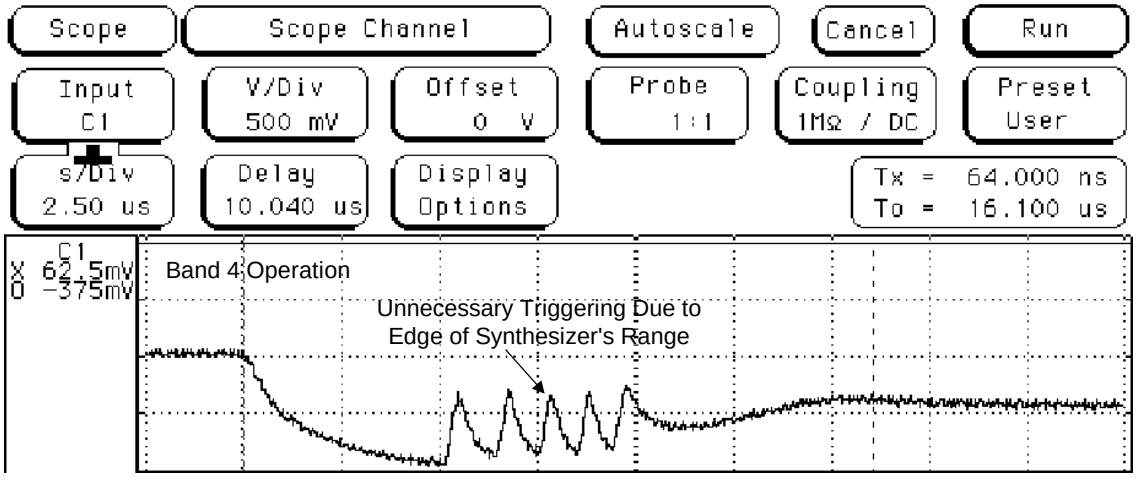

Figure 143 - Continuous VCO Control Voltage for Multi-Band PLL 290MHz Output

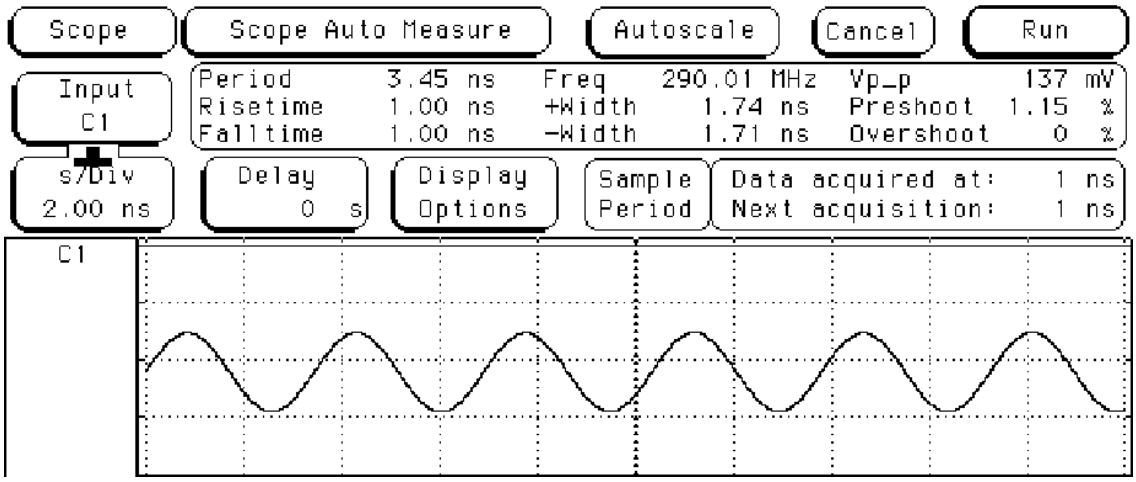

Figure 144 - Experimental 290MHz Multi-Band PLL Output Signal

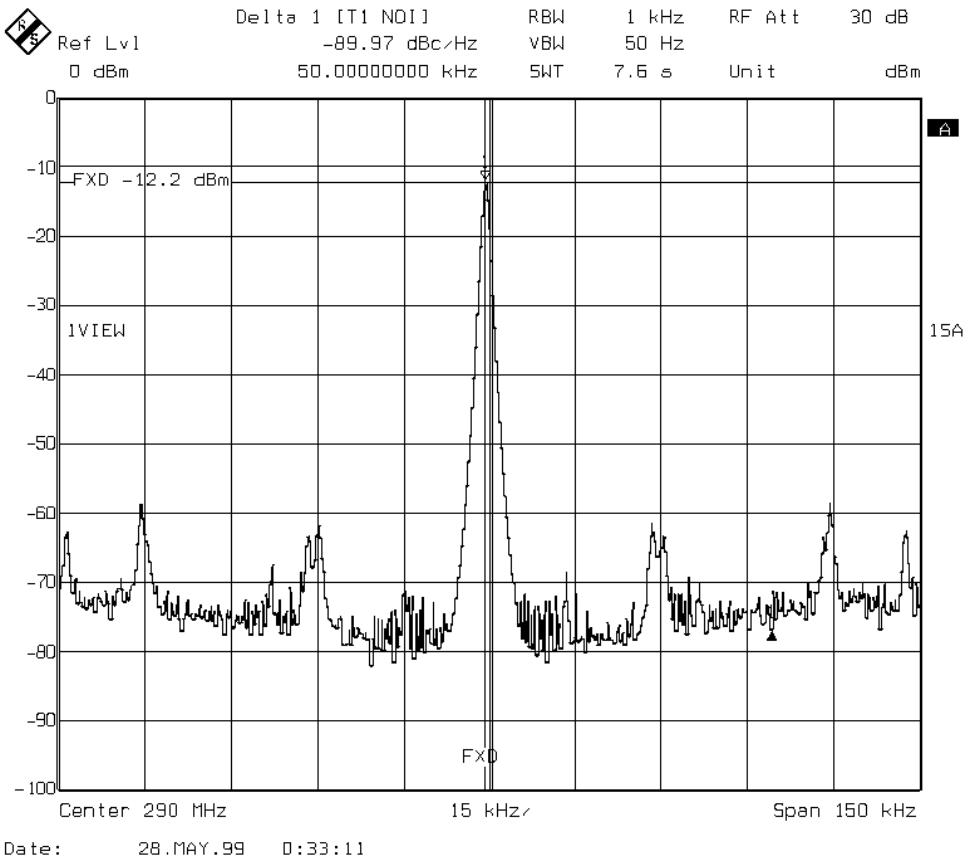

Figure 145 - Experimental 290MHz Multi-Band PLL Output Frequency Spectrum

The multi-band PLL cannot lock on frequencies much higher than 290MHz. Figure 146 shows the multi-band PLL output frequency spectrum when it is synthesizing a 291MHz signal. Notice the high energy content at equal offsets of the fundamental. This is from the multi-band PLL being on the edge of its frequency range.

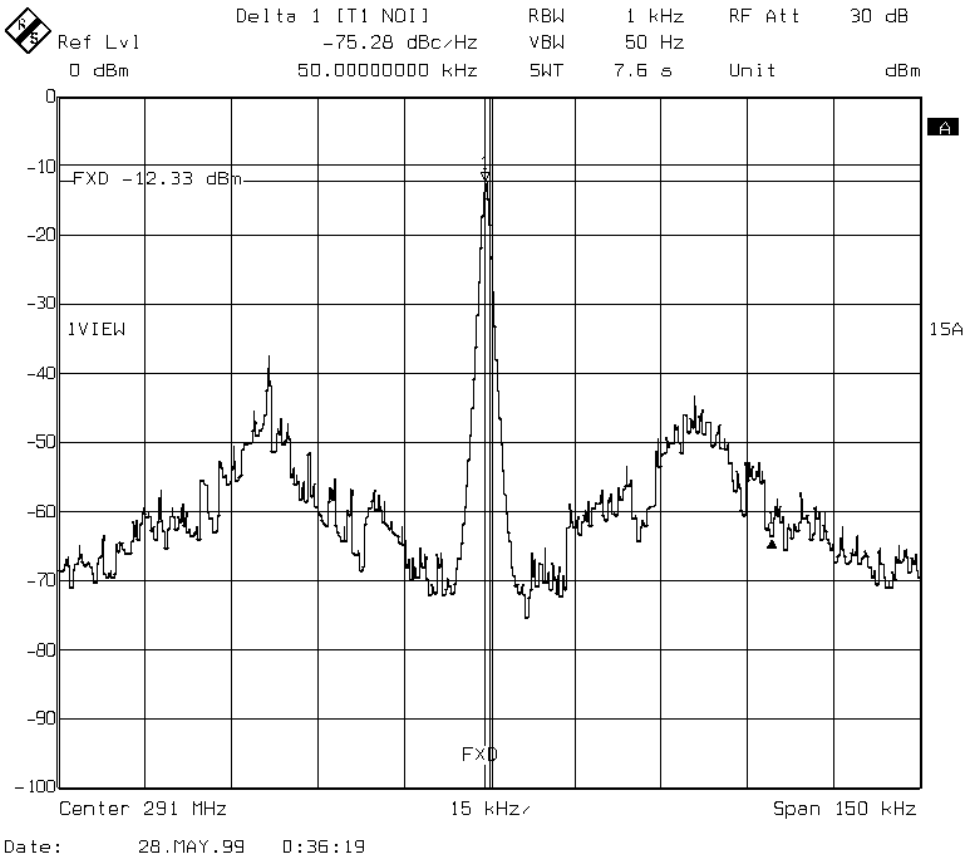

Figure 146 - Experimental 291MHz Multi-Band PLL Output Frequency Spectrum

Case E

The final experimental result presented shows the multi-band PLL synthesizing a 160MHz signal. This is a situation where a frequency that lies in the overlap between two channels is being synthesized. Figure 147 shows the continuous VCO control voltage. All three digital control signals are initially low which means the PLL is not in the correct band of operation. The multi-band PLL was previously locked on a 240MHz

signal. This corresponds to a VCO control voltage of approximately 35mV in band 4. The VCO control voltage then tunes up and switches from band 4 to band 3. It settles on .268V in band 3 to synthesize 160MHz. The measured acquisition time is 8.024µs. This acquisition process is a pull-in process. The output signal measured with the oscilloscope is shown in Figure 148. The output frequency spectrum obtained with the spectrum analyzer is shown in Figure 149. The output signal phase noise is –92.35dBc/Hz at a 50kHz offset.

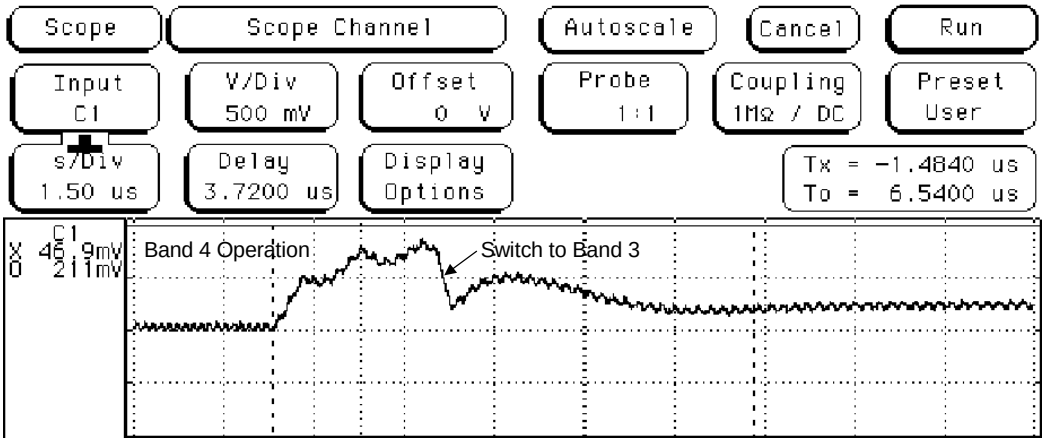

Figure 147 - Continuous VCO Control Voltage for Multi-Band PLL 160MHz Output

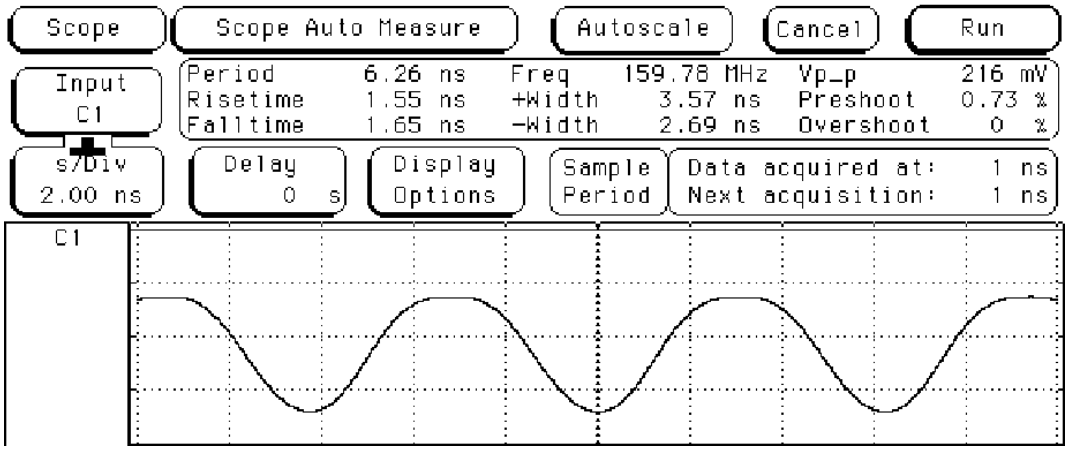

Figure 148 - Experimental 160MHz Multi-Band PLL Output Signal

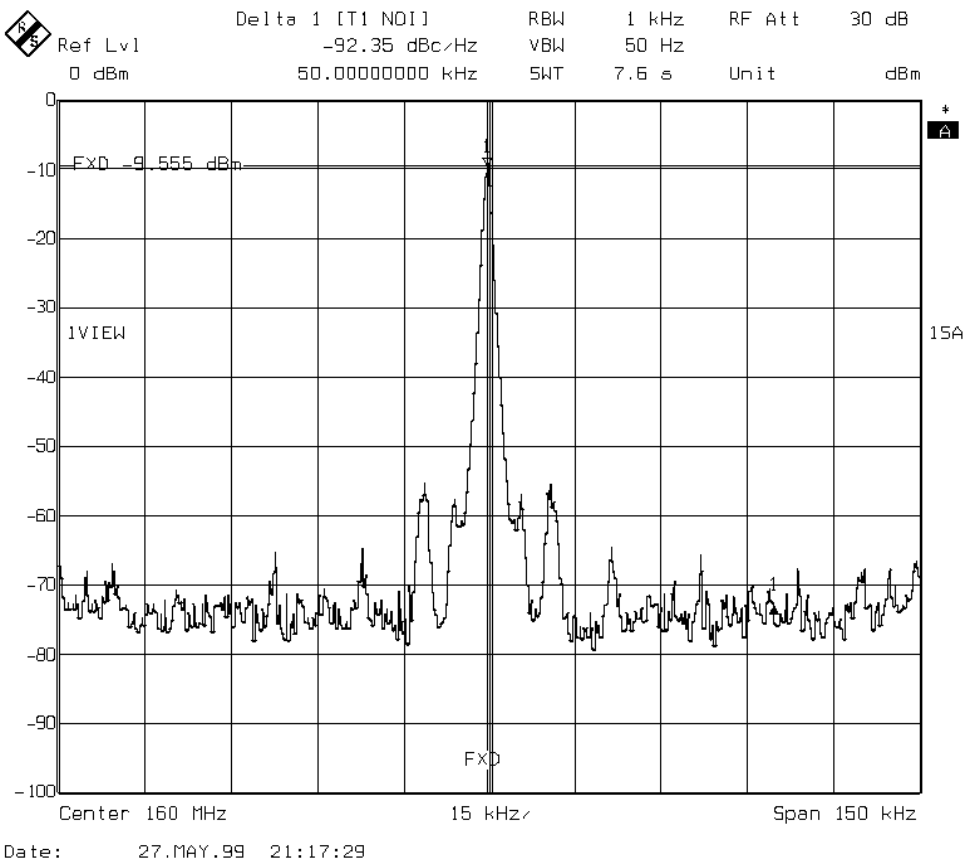

Figure 149 - Experimental 160MHz Multi-Band PLL Output Frequency Spectrum

The multi-band PLL synthesizes a frequency range of 111 to 290MHz. The experimental multi-band PLL frequency response and phase noise performance over the different VCO bands of operation is summarized in Table 21. The multi-band PLL frequency response over the different VCO bands is shown in Figure 150. The frequency overlap between the VCOs and the tuning mechanism insures that the majority of the frequencies are synthesized in the mid-band regions. This overlap also makes it possible for the same frequency to be synthesized by two bands. The band a frequency is synthesized in is a function of the synthesizer's original band of operation. If the synthesizer is originally operating in band 1 and attempts to synthesize a frequency that is capable of being synthesized in band 1 or 2 it is more probable to remain in band 1 because the overshoot will not cause it to switch to band 2. The multi-band PLL phase

noise performance over the different VCO bands is shown in Figure 151. The synthesizer's phase noise performance mostly lies in the –90 to –95dBc/Hz at a 50kHz offset. A few points along the edges of the bands perform worse than –90dBc/Hz.

Table 21 - Experimental Multi-Band PLL Results

Band	Description	Frequency Range (MHz)	Phase Noise @ 50kHz Offset (dBc/Hz)
1	All Switches Closed	111 – 140	-87.68 ? -94.06
2	2 Switches Closed	130 – 175	-87.98 ? -94.52
3	1 Switch Closed	155 – 220	-87.54 ? -93.99
4	All Switches Open	195 – 290	-88.03 ? -96.49

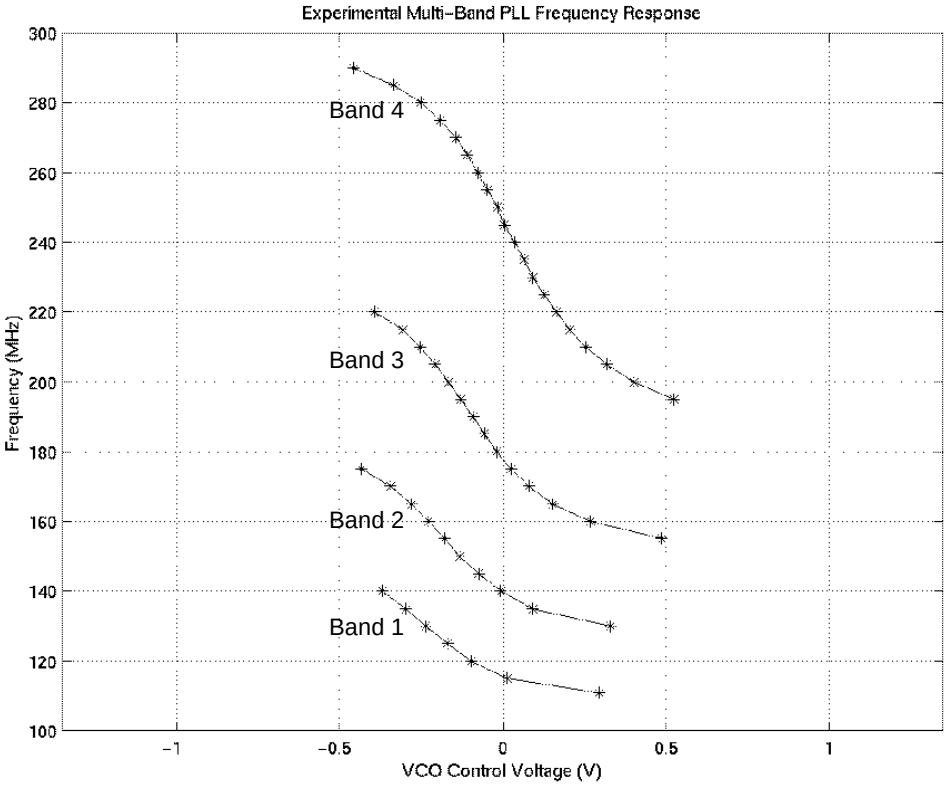

Figure 150 - Experimental Multi-Band PLL Frequency Response

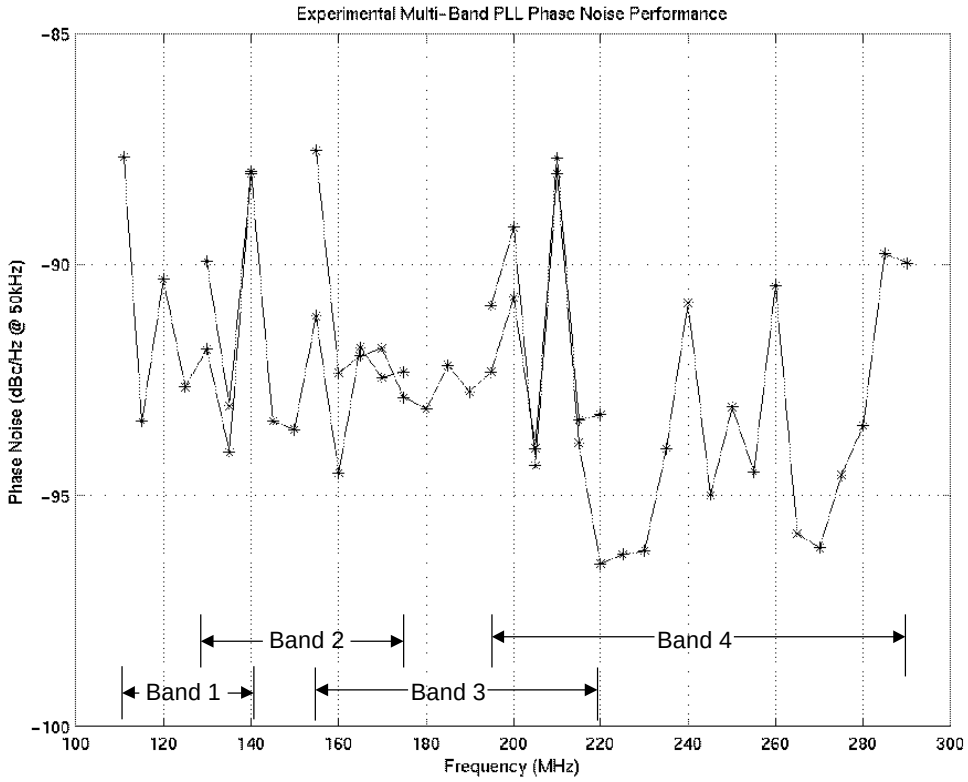

Figure 151 - Experimental Multi-Band PLL Phase Noise Performance

Classic Digital PLL Frequency Synthesizer

The prototype chip shown in Figure 152 contains the classic digital PLL frequency synthesizer.

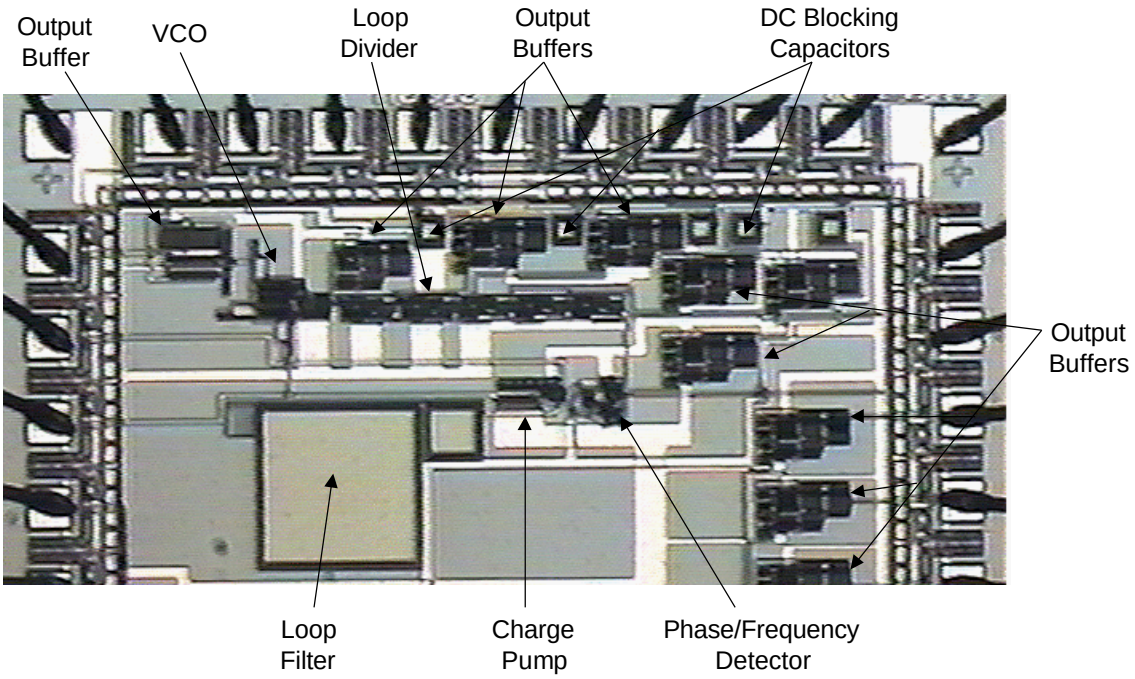

Figure 152 - Classic Digital PLL Prototype Chip

The classic digital PLL frequency synthesizer was characterized to determine the frequency range and phase noise performance on a high frequency test board shown in Figure 153.

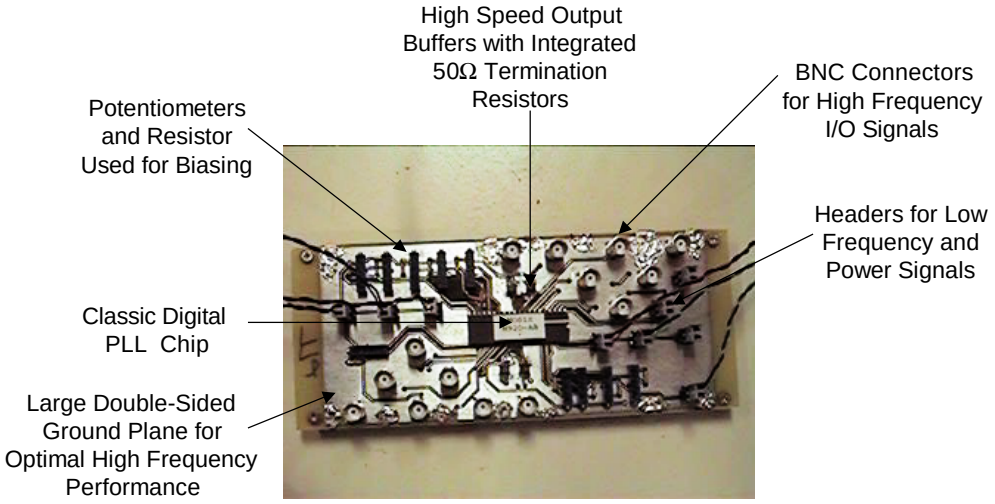

Figure 153 - Classic Digital PLL Test Board

The test cases presented in the previous section are reproduced experimentally to illustrate the PLL frequency synthesizer performance. Table 22 summarizes the setup for each case. The frequencies have been adjusted from the previous section to comply with the measured multi-band PLL regions.

Table 22 - Classic Digital PLL Frequency Synthesizer Experimental Case Studies

Case	Initial Frequency	Final Frequency	? f	Experiment Type	Acquisition Time
A	340MHz	370MHz	30MHz	Maximum Frequency	9.53µs
B	340MHz	221MHz	-119MHz	Minimum Frequency	20.548µs
C	340MHz	250MHz	-90MHz	Mid-Band	4.004µs

In all cases the classic digital PLL is initially operating in the mid-band region at a frequency of 340MHz. The initial output signal measured with the oscilloscope is shown in Figure 154. The initial output frequency spectrum is shown in Figure 155. The initial output signal phase noise is –89.38dBc/Hz at a 50kHz offset.

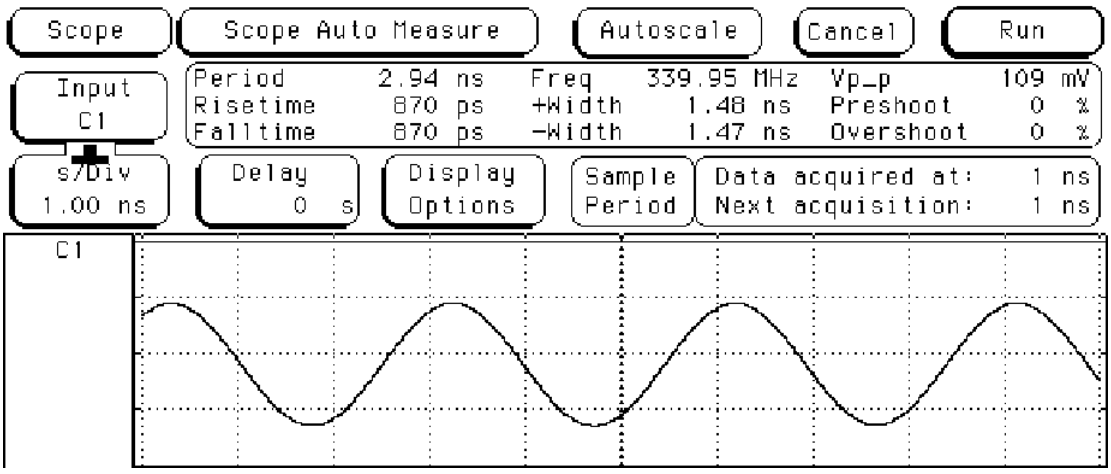

Figure 154 - Initial Experimental 340MHz Classic Digital PLL Output Signal

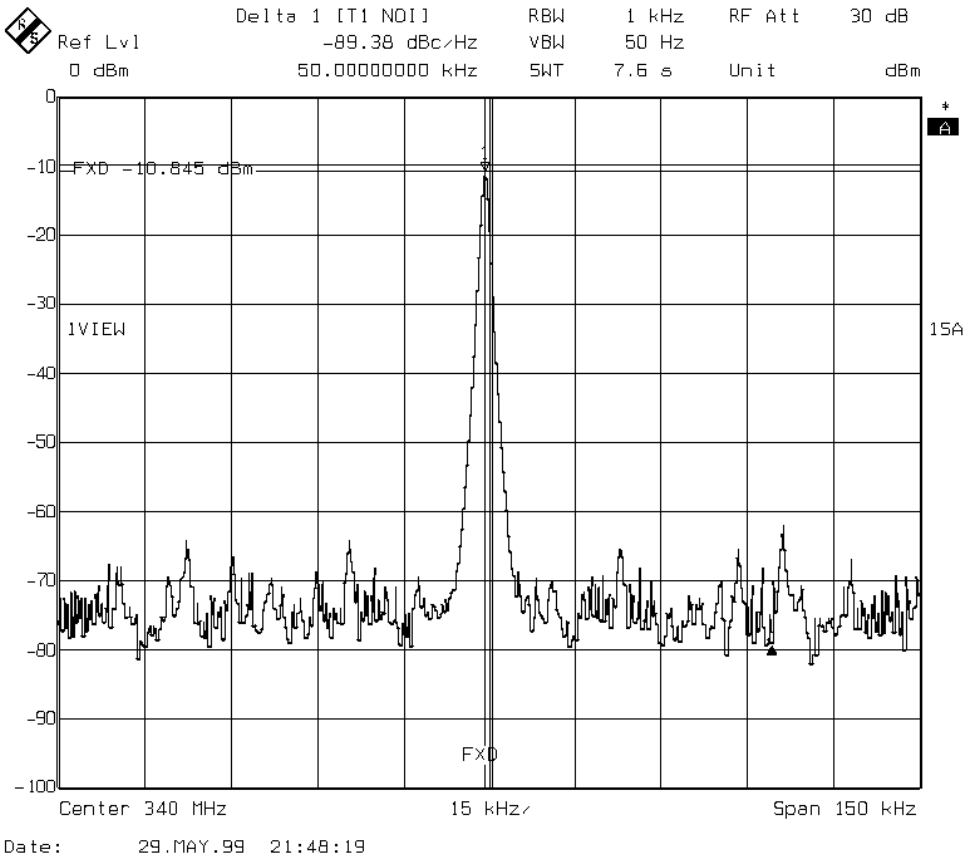

Figure 155 - Initial Experimental 340MHz Classic Digital PLL Output Frequency Spectrum

Case A

The first experimental result presented shows the classic digital PLL synthesizing a 370MHz signal. This illustrates a situation where close to the maximum frequency is being synthesized. Figure 156 shows the VCO control voltage. The PLL was previously locked on a 340MHz signal. This corresponds to a VCO control voltage of approximately -80mV. The VCO control voltage then tunes down to -.463V to synthesize 370MHz. The measured acquisition time is 9.53µs. The reason for the length of the acquisition time is that the PLL is operating in a region where the VCO gain has decreased due to non-linearity in the gain. The output signal measured with an oscilloscope is shown in Figure 157. Figure 158 shows the output frequency spectrum obtained with a spectrum analyzer. The output signal phase noise is –73.96dBc/Hz at a 50kHz offset.

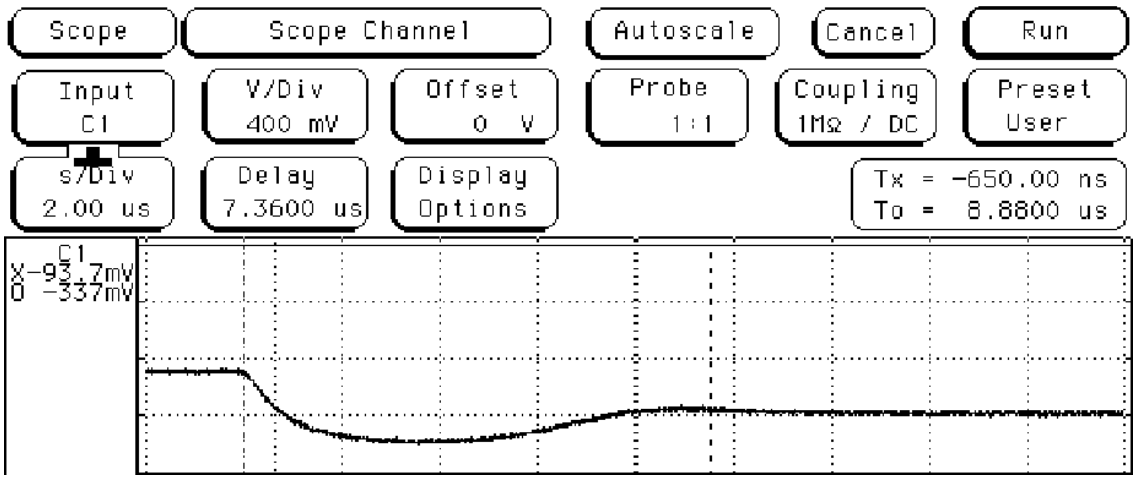

Figure 156 - VCO Control Voltage for Classic Digital PLL 370MHz Output

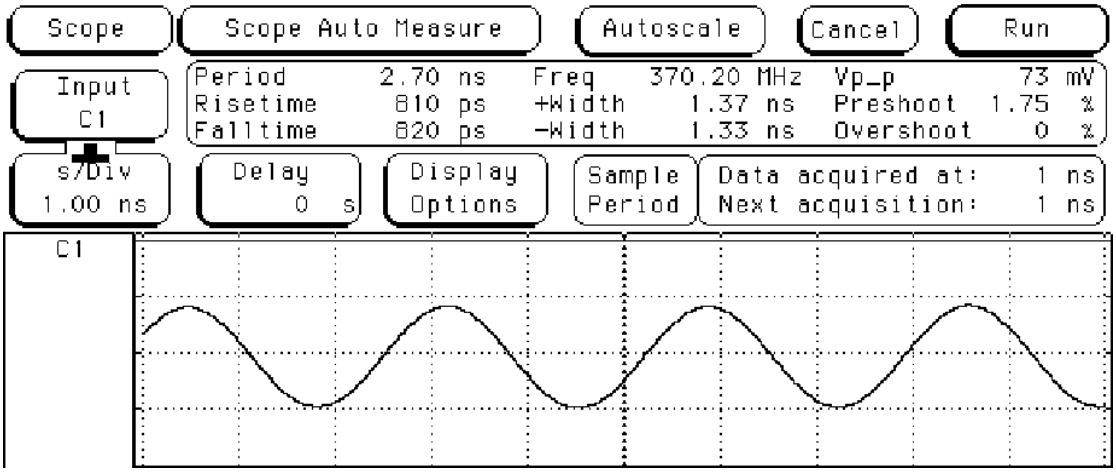

Figure 157 - Experimental 370MHz Classic Digital PLL Output Signal

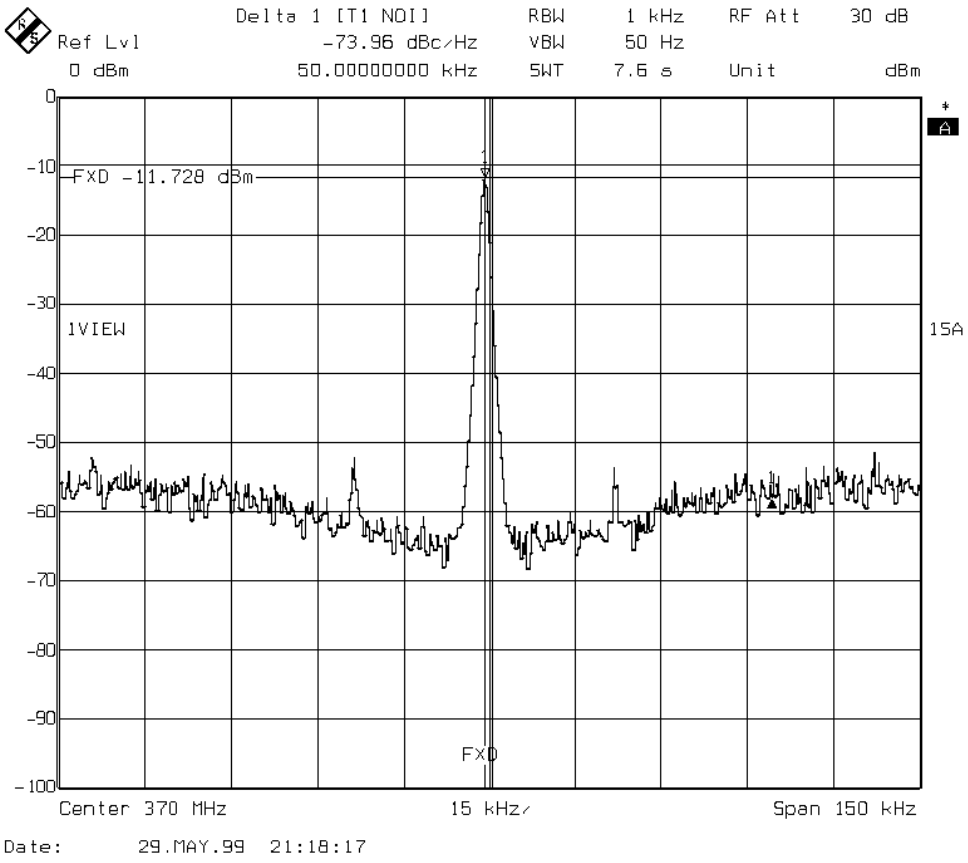

Figure 158 - Experimental 370MHz Classic Digital PLL Output Frequency Spectrum

The classic digital PLL cannot synthesize frequencies much higher than 370MHz due to VCO tuning range limitations. Figure 159 shows the PLL failing to synthesize a 371MHz signal. The output frequency spectrum has a slight peak at 370.5MHz and the majority of the energy is spread from 370 to 370.8MHz.

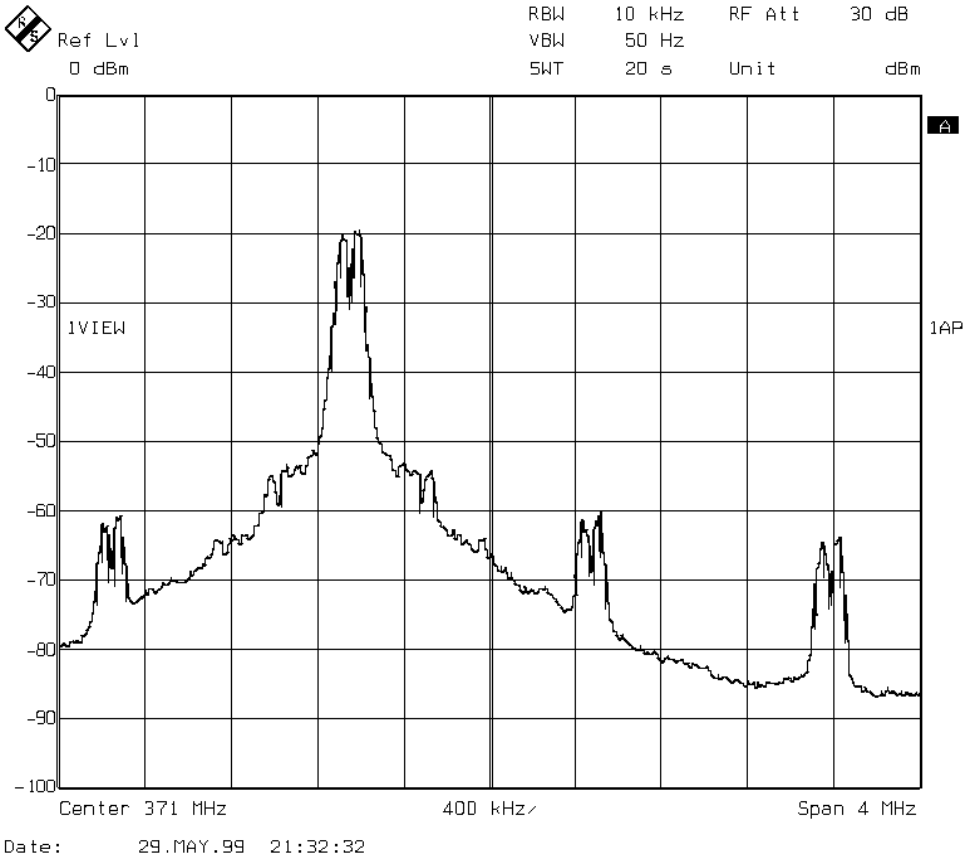

Figure 159 - Classic Digital PLL Failing To Synthesize 371MHz

Case B

The second experimental result presented shows the classic digital PLL synthesizing a 221MHz signal. This illustrates a situation where close to the minimum frequency is being synthesized. Figure 160 shows the VCO control voltage. The PLL was previously locked on a 340MHz signal. This corresponds to a VCO control voltage of approximately -80mV. The VCO control voltage then tunes up to approximately 0.97V

to synthesize 221MHz. The measured acquisition time is 20.548µs. The length of the acquisition time is due to the frequency change being outside of the lock range. The acquisition process is a pull-in process. The output signal measured with an oscilloscope is shown in Figure 161. The output frequency spectrum obtained with a spectrum analyzer is shown in Figure 162. The output signal phase noise is –75.26dBc/Hz at a 50kHz offset.

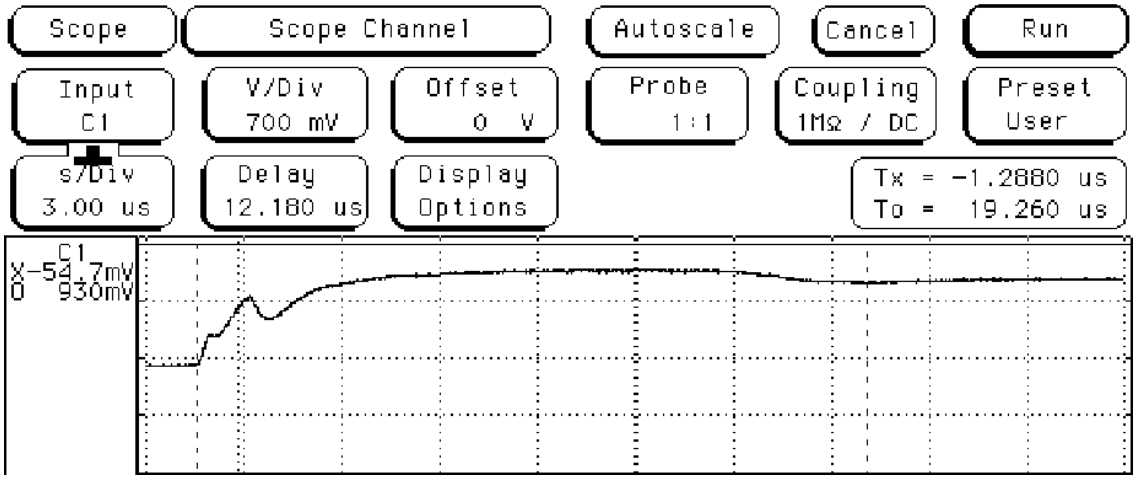

Figure 160 - VCO Control Voltage for Classic Digital PLL 221MHz Output

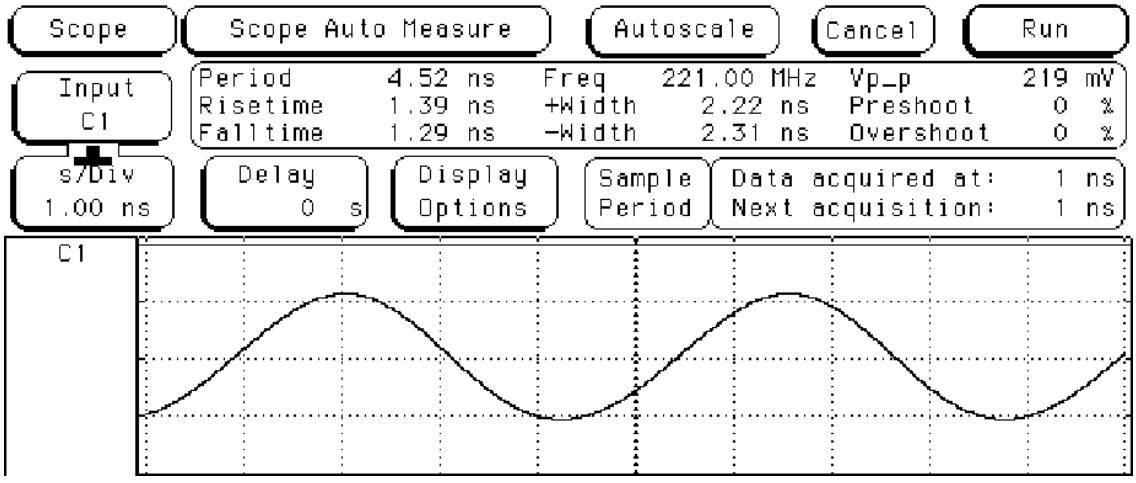

Figure 161 - Experimental 221 MHz Classic Digital PLL Output Signal

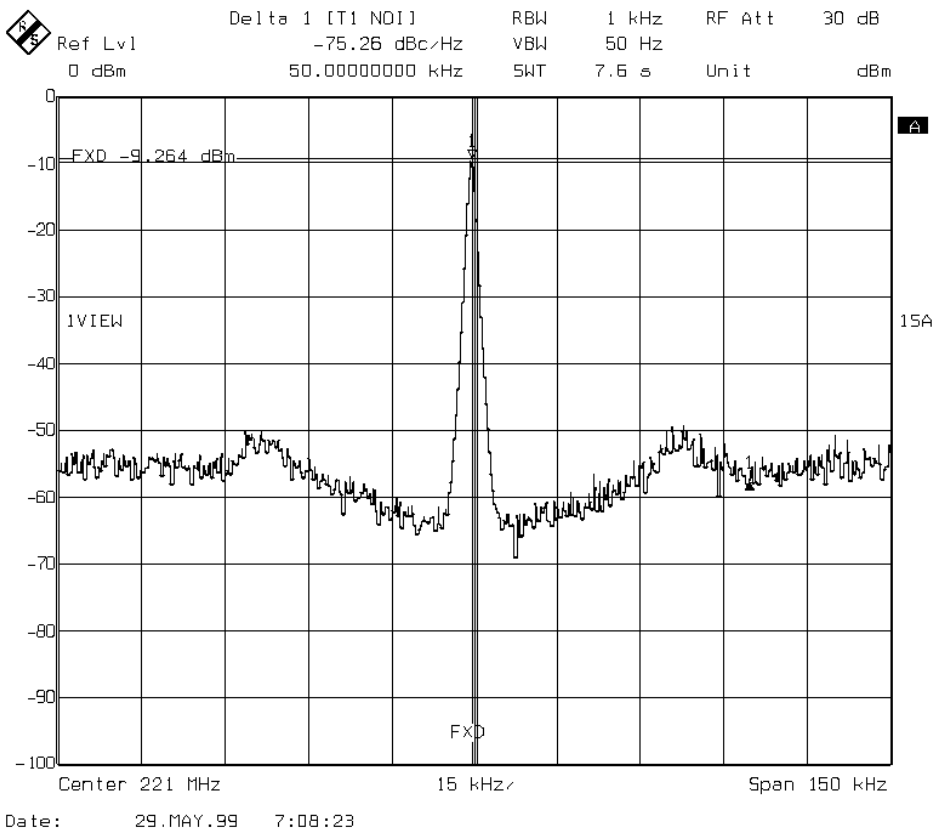

Figure 162 - Experimental 221MHz Classic Digital PLL Output Frequency Spectrum

The classic digital PLL cannot lock on frequencies much lower than 221MHz. Figure 163 shows the PLL output frequency spectrum when it is synthesizing a 220MHz signal. The output frequency spectrum has a large phase noise value of –69.27dBc/Hz at a 50kHz offset. This is from the PLL being on the edge of it's frequency range.

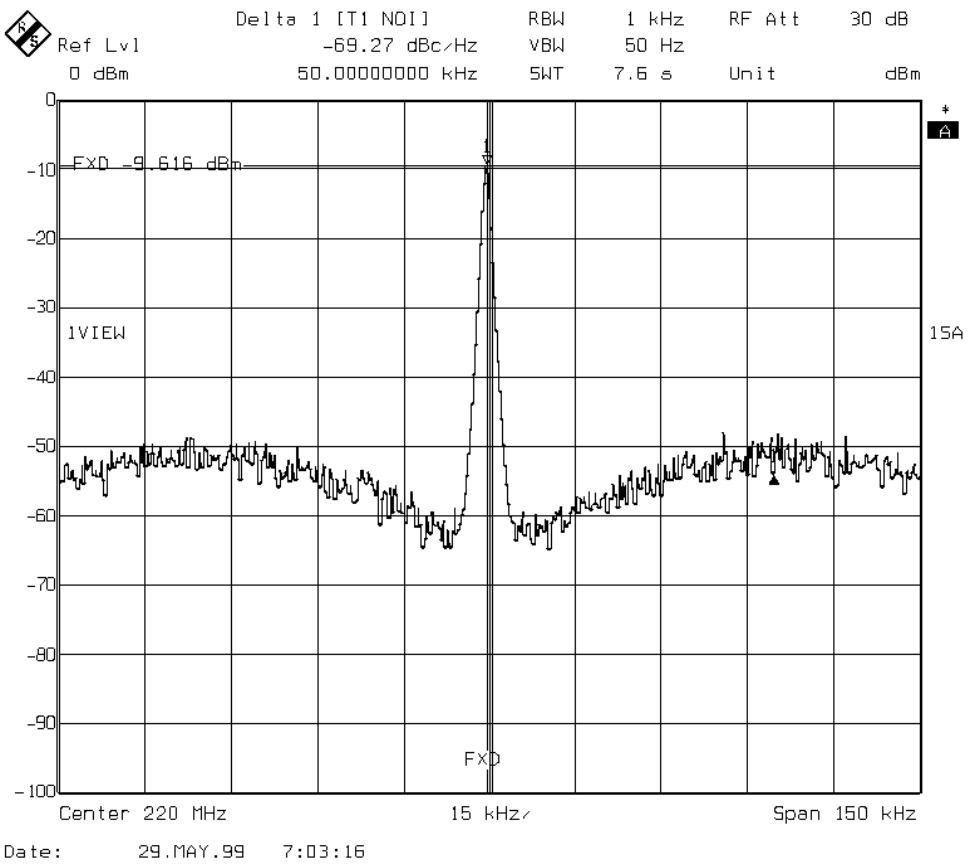

Figure 163 - Experimental 220MHz Classic Digital PLL Output Frequency Spectrum

Case C

The third experimental result presented shows the classic digital PLL synthesizing a 250MHz signal. This illustrates a situation where a mid-band frequency is being synthesized. Figure 164 shows the VCO control voltage. The previous signal the PLL was locked on was 340MHz. This corresponds to a VCO control voltage of approximately -80mV. The VCO control voltage then tunes up to approximately .378V to synthesize 250MHz. The measured acquisition time is 4.004µs. This acquisition time is short because the frequency change is within the lock range. The output signal measured with an oscilloscope is shown in Figure 165. The output frequency spectrum

obtained with a spectrum analyzer is shown in Figure 166. The output signal phase noise is –86.15dBc/Hz at a 50kHz offset.

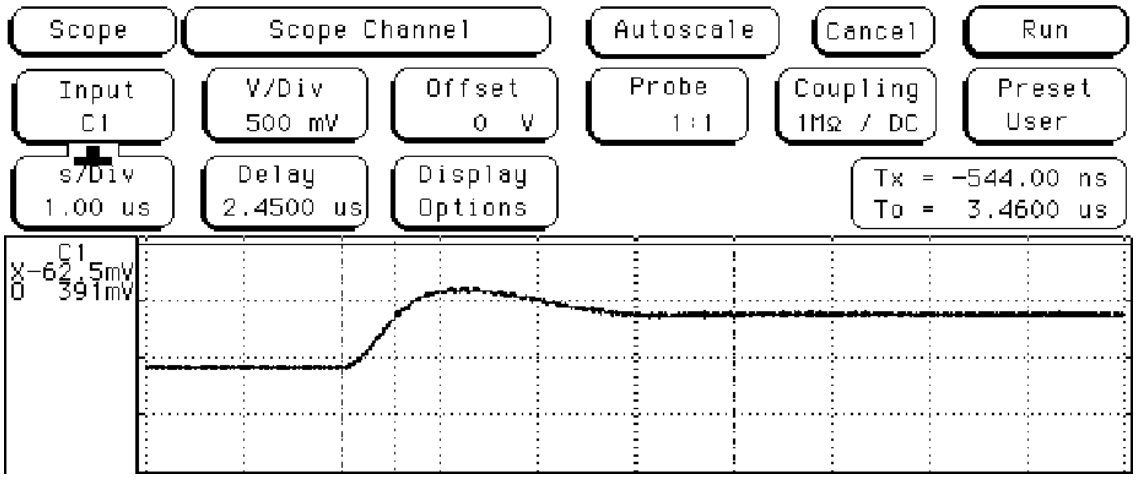

Figure 164 - VCO Control Voltage for Classic Digital PLL 250MHz Output

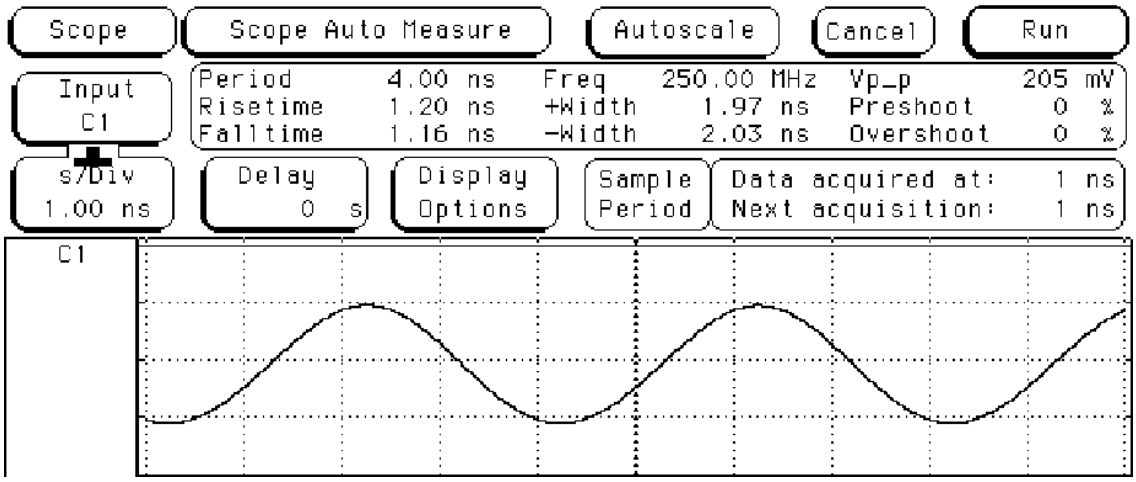

Figure 165 - Experimental 250MHz Classic Digital PLL Output Signal

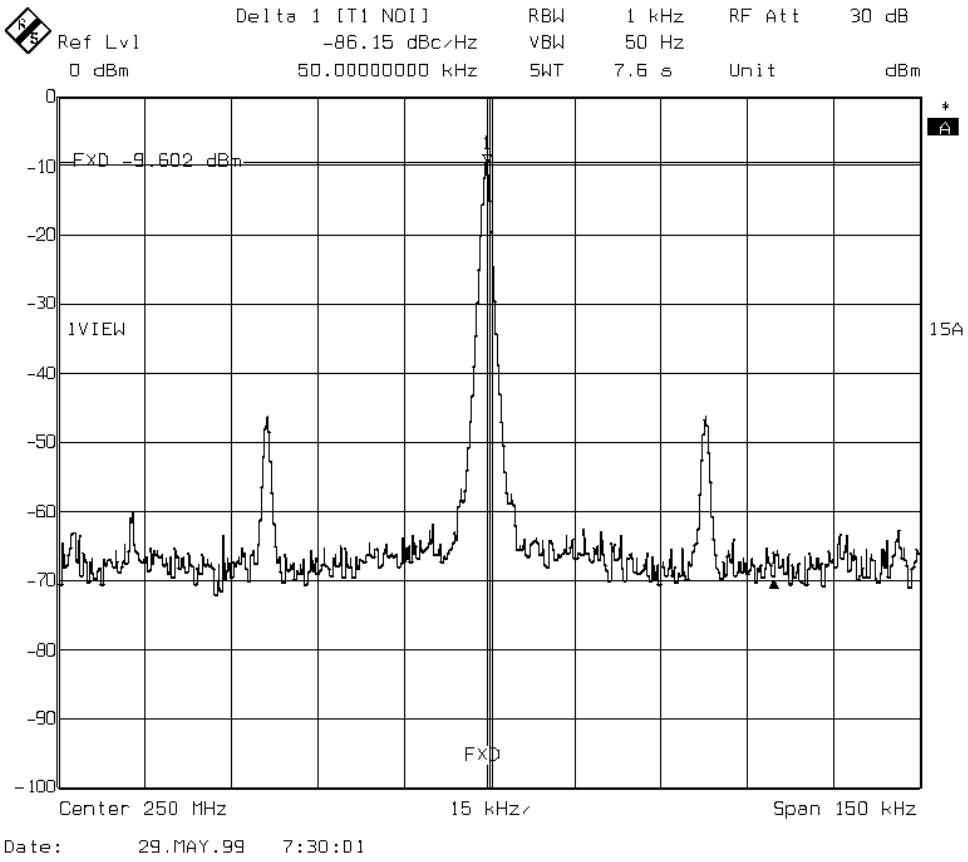

Figure 166 - Experimental 250MHz Classic Digital PLL Output Frequency Spectrum

The classic digital PLL synthesizes a frequency range of 221 to 370MHz. The frequency response over the tuning range is shown in Figure 167. The multi-band PLL phase noise performance over the tuning range is shown in Figure 168. The synthesizer's phase noise performance mostly lies in the –80 to –90dBc/Hz at a 50kHz offset. A few points along the edges of the bands perform worse than –80dBc/Hz.

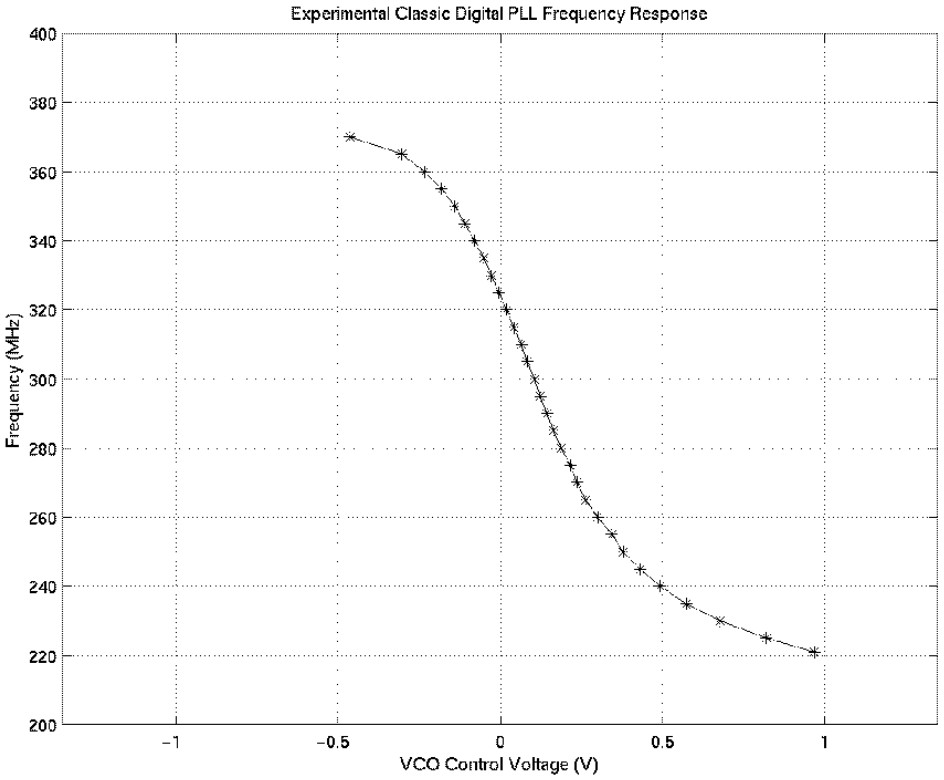

Figure 167 - Experimental Classic Digital PLL Frequency Response

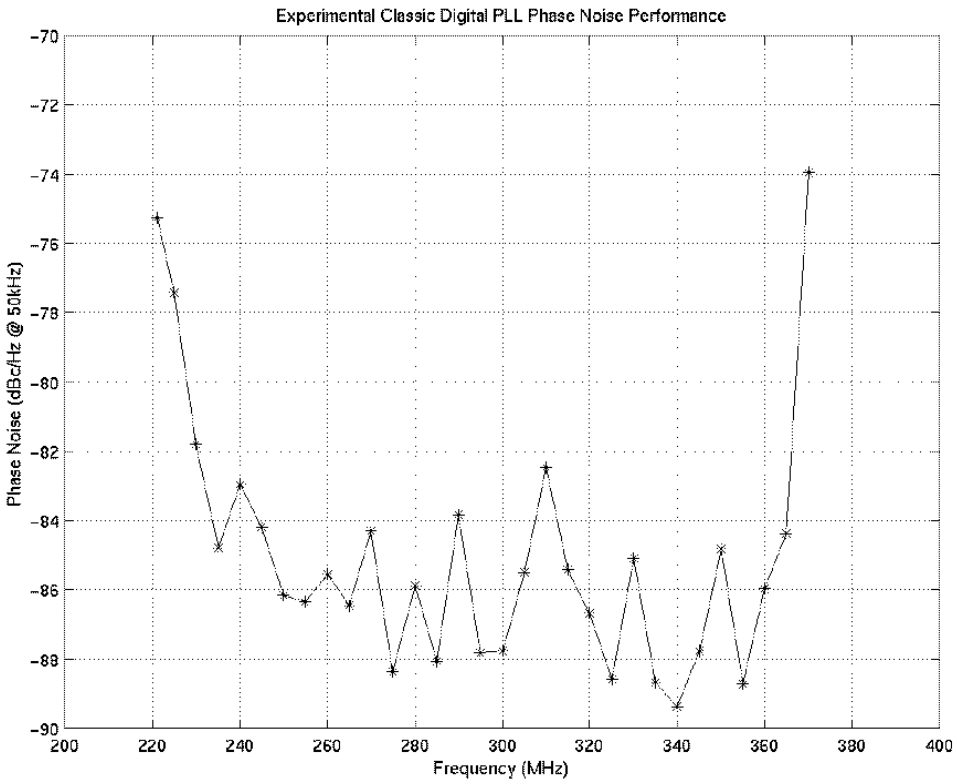

Figure 168 - Experimental Classic Digital PLL Phase Noise Performance

A Performance Comparison between the Multi-Band and the Classic Digital PLL Frequency Synthesizers

Table 23 provides a comparison between the experimental performance of the multi-band PLL and the classic digital PLL. In summary, the multi-band PLL achieved a 20% wider tuning range than the classic digital PLL. The multi-band PLL was able to achieve a wider tuning range while maintaining a lower VCO conversion gain. This lower VCO conversion gain allowed the multi-band PLL frequency synthesizer to outperform the classic digital PLL in the area of phase noise performance by an average of 7.3dB. The synthesizer's acquisition time depends on the region that the PLL operates in and is a strong function of the VCO conversion gain. Case A of the multi-band PLL and the classic digital PLL can be used to compare the acquisition time for a

frequency step of 30MHz. The multi-band PLL has an acquisition time of 4.5µs and the classic digital PLL has an acquisition time of 9.53µs. However, the reason for the classic digital PLL to have a slow acquisition is because it is operating near the edge of the synthesizer's range in a region where the VCO gain is low. Case C of the multi-band PLL and case B of the classic digital PLL can be used to compare the acquisition time for a large frequency step to close to the minimum operating frequency. This is a pull-in process for both synthesizers, with the multi-band PLL switching down three bands. The multi-band PLL acquires lock in 17.024µs, while the classic digital PLL locks in 20.548µs. Case E of the multi-band PLL and case C of the classic digital PLL can be used to compare the acquisition time for a mid-band frequency step. The multi-band PLL has an acquisition time of 8.024µs and the classic digital PLL has an acquisition time of 4.004µs. This is a pull-in process for the multi-band PLL, during which the PLL switches bands. The acquisition time is much lower for the classic digital PLL because the frequency step is within the lock range due to the large VCO conversion gain of the PLL.

Table 23 - Multi-Band and Classic Digital PLL Experimental Performance Comparison

PLL System	Frequency Range (MHz)	Average PLL System Phase Noise (dBc/Hz @ 50kHz)	Acquisition Time (µs)
Multi-Band	111 – 290	-92.29	4.5 – 17
Classic	221 – 370	-84.98	4 – 20.5

CONCLUSIONS

The implementation of a proposed multi-band phase-locked loop frequency synthesizer was accomplished in this thesis work. This research was motivated by the necessity for integrated multi-band frequency synthesizers for use in multi-standard transceivers. The multi-band PLL frequency synthesizer uses a switched tuning VCO that allows a wide frequency range with a low conversion gain. Experimental results show that the multi-band PLL frequency synthesizer is superior over the classic digital frequency synthesizer in terms of frequency range and phase noise performance. These results prove that the switched tuning VCO structure is suitable for a multi-band synthesizer.

Future work could be performed to improve the performance of the multi-band PLL frequency synthesizer and make it easier to integrate into a multi-standard transceiver. The use of a four-stage differential ring oscillator would improve the phase noise performance due to the higher rejection of supply and common-mode noise. Also, a four-stage oscillator provides quadrature outputs necessary in typical communication systems. The use of differential current-mode flip-flops in the loop divider would also aid in noise performance and improve the robustness of the loop divider. These flip-flops could be integrated into a dual-modulus prescaler for use in fractional-N frequency synthesis.

The multi-band PLL frequency synthesizer was implemented using a 1.2µm technology. The multi-band PLL frequency synthesizer can synthesize higher frequencies with the use of sub-micron technology. Operating at higher frequencies with the use of sub-micron technology would reduce the area required to use a higher Q switched tuning LC oscillator. A higher Q switched tuning LC oscillator has better phase noise performance over a low Q ring oscillator. The use of an LC oscillator would thus result in superior synthesizer phase noise performance.

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APPENDIX A

SPECTREHDL MULTI-BAND PLL FREQUENCY SYNTHESIZER

BEHAVIORAL MACROMODEL

```
// Multi-Band Phase Locked Loop Frequency Synthesizer Macromodel
// Main Spectre File
// Samuel Palermo

simulator lang=spectre

include "/home/samuel/research/pll/macromodels/pd/dig_pfd/dig_pfd.def"
include "/home/samuel/research/pll/macromodels/lpf/lpf.def"
ahdl_include "/home/samuel/research/pll/macromodels/vco/vco.def"
ahdl_include "/home/samuel/research/pll/macromodels/vco/switch_vco.def"
ahdl_include
+ "/home/samuel/research/pll/macromodels/divider/divider.def"
include "/home/samuel/research/pll/macromodels/vco/reference.def"

// Power Supply
vdd dd 0 vsource dc=1

// Reference Signal
xref 0 control fref reference
vcontrol control 0 vsource type=pwl wave=[0 0.64 1u 0.64]

// Digital Tri-State Phase/Frequency Comparator
xdig_pfd 0 dd fref fvco up upbar down downbar dig_pfd

// Charge Pump
iup dd 1 isource dc=25u
idown 2 0 isource dc=25u

gup 1 vd up 0 relay vt1=0 vt2=1 ropen=100M rclosed=1m
gupbar 1 0 upbar 0 relay vt1=0 vt2=1 ropen=100M rclosed=1m
gdown vd 2 down 0 relay vt1=0 vt2=1 ropen=100M rclosed=1m
gdownbar dd 2 downbar 0 relay vt1=0 vt2=1 ropen=100M rclosed=1m

// Loop Filter
xfilter 0 vd lpf
gvdgnd vd 0 vd_gnd 0 relay vt1=0 vt2=1 ropen=100M rclosed=10

// Voltage Controlled Oscillator
//xvco vd out vco (gain=40e6 fc=256e6)
xvco 0 vd out nv_temp vd_gnd
+ switch_vco (u=0.8 d=-0.8 gain=40e6 fc=256e6)

// Divider
xdivider 0 out fvco buffer n_temp divider (divisor=32)

op dc
```

```
timedom tran stop=20u step=20p ic=all maxstep=20p skipdc=yes
relref=alllocal
simulator lang=spice
.ic vd=0
save vd control fref fvco nv_temp vd_gnd
.OPTIONS rawfmt=psfbin save=selected diagnose=yes vabstol=.01
+ reltol=.99
********************************************************************************

// Digital Phase Frequency Detector Macromodel
// Samuel Palermo

subckt dig_pfd (gnd dd fref fvco up upbar down downbar)

ahdl_include "/home/samuel/research/pll/macromodels/pd/dig_pfd/dff.def"
ahdl_include
+ "/home/samuel/research/pll/macromodels/pd/dig_pfd/nand.def"

xdffup gnd dd fref up upbar r dff
xdffdown gnd dd fvco down downbar r dff
xnand gnd up down r nand

ends dig_pfd
********************************************************************************

// D Flip Flop Macromodel
// Samuel Palermo

module dff(gnd, D, CLK, Q, QBAR, R) ()
node [V, I] gnd, D, CLK, Q, QBAR, R ;
{

  real Q_temp;
  real QBAR_temp;

  initial {
    Q_temp=0;
    QBAR_temp=1;
    }

  analog {
    if ($threshold (V(CLK, gnd)-1, 1)) {
      if (V(D,gnd)==1) {
        Q_temp=1;
      QBAR_temp=0;
      }
      else {
      Q_temp=0;
      QBAR_temp=1;
      }
    }
    if (V(R, gnd)==0) {
      Q_temp=0;
      QBAR_temp=1;
```

```
    }
      V(Q, gnd) <- Q_temp;
      V(QBAR, gnd) <- QBAR_temp;
    }
}
*********************************************************************

// NAND Macromodel
// Samuel Palermo

module nand(gnd, A, B, O) ()
node [V, I] gnd, A, B, O ;
{

  real O_temp;

  analog {

    if ((V(A, gnd)==1) && (V(B, gnd)==1)) {
      O_temp=0;
    }
    else {
      O_temp=1;
    }
      V(O, gnd) <- O_temp;
    }
}
*********************************************************************

// Low Pass Filter Macromodel
// Samuel Palermo

subckt lpf(gnd vd)

c1 vd z capacitor c=62.2p
// Damping Factor = 0.7
r z gnd resistor r=31.8k
//Damping Factor = 1
//r z gnd resistor r=45.7k
//Damping Factor = 10
//r z gnd resistor r=457k
//Damping Factor = 0.1
//r z gnd resistor r=4.57k
//Damping Factor = 2
//r z gnd resistor r=91.4k
//Damping Factor = 0.5
//r z gnd resistor r=22.9k
c2 vd gnd capacitor c=6p

ends lpf
*********************************************************************

// VCO Macromodel
// Samuel Palermo
```

```
#define PI 3.14159265359

module vco(IN, OUT) (gain, fc)
node [V, I] IN, OUT;
parameter real gain = 1, fc = 1;
{
      analog
            V(OUT) <- sin(2*PI*(integ(fc + gain*V(IN), 0)));
}
**********************************************************************

// Switched Tuning VCO Macromodel
// Samuel Palermo

#define PI 3.14159265359

module switch_vco(gnd, vd, out, nv_temp, vd_gnd) (u, d, gain, fc)
node [V, I] gnd, vd, out, nv_temp, vd_gnd;
parameter real u = 1, d = 1, gain = 1, fc = 1;
{

      integer n;
      real vd_gnd_temp;

      initial {
            n=0;
      }

      analog {
            if((V(vd, gnd) < 1m) && (V(vd,gnd) > -1m)) {
                  vd_gnd_temp = 0;
            }
            if ($threshold ((V(vd, gnd)-(u)), +1)) {
                  n=n+1;
                  vd_gnd_temp=1;
            }
            if ($threshold ((V(gnd, vd)+(d)), +1)) {
                  n=n-1;
                  vd_gnd_temp=1;
            }
            V(out, gnd) <- 1.35*sin(2*PI*(integ((fc+(2*.7*u*n*gain)) +
+ gain*V(vd, gnd), 0)));
            V(nv_temp, gnd) <- n;
            V(vd_gnd, gnd) <- vd_gnd_temp;
      }
}
**********************************************************************

// Loop Divider Macromodel
// Samuel Palermo

module divider(gnd, out, fvco, buffer, n_temp) (divisor)
parameter integer divisor = 1;
```

```
node [V, I] gnd, out, fvco, buffer, n_temp ;
{

      real buffer_temp;
      integer n;
      real fvco_temp;

      initial {
            buffer_temp=0;
            n=1;
            fvco_temp=1;
      }

      analog {
            if(V(out, gnd)>0) {
                  buffer_temp=1;
            }
            else {
                  buffer_temp=-1;
            }
            if($threshold (V(buffer, gnd)-1, 1)) {
                  n=n+1;
            }
            if($threshold (V(buffer, gnd)+1, -1)) {
                  n=n+1;
            }
            if(n==divisor) {
                  n=0;
                  fvco_temp=(-1*fvco_temp);
            }
      V(fvco, gnd) <- fvco_temp;
      V(buffer, gnd) <- buffer_temp;
      V(n_temp, gnd) <- n;
      }
}
*********************************************************************************

// Reference Macromodel
// Samuel Palermo

subckt reference(gnd control in)

ahdl_include "/home/samuel/research/pll/macromodels/vco/buffer.def"

xvco control out vco (gain=1.25e6 fc=8e6)
xbuffer gnd out in buffer

ends reference
*********************************************************************************

// Buffer Macromodel
// Samuel Palermo

module buffer(gnd, in, out)
```

```
node [V, I] gnd, in, out ;
{

	real out_temp;

	initial {
		out_temp=0;
	}

	analog {
		if(V(in, gnd)>0) {
			out_temp=1;
		}
		else {
			out_temp=-1;
		}
	V(out, gnd) <- out_temp;
	}
}
*********************************************************************************
```

VITA

Samuel Michael Palermo was born in Bryan, TX, on October 28, 1974. He graduated magna cum laude with a B.S. degree in electrical engineering from Texas A&M University in May 1997. He will receive the M.S. degree in electrical engineering in August 1999.

From 1995 to 1997, he worked as an intern for Texas Instruments, Dallas, TX, where he designed SRAM's for ASIC designs and performed ESD and latch-up characterization. During the summer of 1997, he was with Motorola, Austin, TX, where he performed design work on integrated test circuitry for HC08 micro-controllers. He will soon join Texas Instruments, Dallas, TX, where he will work on high-speed CMOS clock recovery and data synchronization circuits.

Mr. Palermo is a member of IEEE, Eta Kappa Nu, and Phi Eta Sigma. He received a Texas A&M University Regents' Fellowship in 1997 and a National Science Foundation Graduate Research Fellowship in 1999.

PERMANENT ADDRESS

1589 Palermo Lane
Bryan, TX 77808