

BUILT-IN SELF TEST FOR PIPELINE ADC'S

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Abstract

This paper presents a new Built-In Self-Test for Pipeline ADC's. The test set is divided in 3 parts: Monotonicity test for basic functionality verification, DC gain of each stage and frequency bandwidth of each stage. The approach is based on the "Divide and conquer" principle. Adaptive schemes are used to get a precise analog timer, ramp generator and compensation for process variations.

1. Introduction

Analog testing, because of its complexity, is a very active research area. Several research groups have suggested techniques to make ADC BISTs. Gordon et al have proposed methods to make frequency domain tests on Sigma-Delta converters by generating precise on-chip sine-waves and analyzing the results with an on-chip DSP [1]. Also, Ehsanian and Kaminska, have proposed a technique to make dc and frequency domain tests on ADCs by using the already present DAC in the ADC and generate precise analog signals. Once converted back into digital form by the ADC under test, the results are compared and analyzed [2]. A technique for bandwidth test is also proposed by Arabi and Kaminska. It is based on feedback configuration of the ADC. This configuration forces the ADC to run at its maximum speed and allows to analyze its frequency bandwidth as well as some DC non-linearities [3].

This paper presents a Built-In Self-Test scheme for pipeline ADC's based on functionality tests of internal key components¹. DC precision, frequency bandwidth and overall functionality are tested on-chip without the use of any DSP or precise signal generator. Also, the objective was to design a test circuit with good area, power and precision tradeoffs. This circuit provides a final "go-no go" type of signal to the user. Moreover, the circuit also provides some auto-calibration. The paper is divided in 6 sections. Section 2 will give an overview of the steps used in the test procedure. Section 3 will describe each test step in detail. Then, section 4 describes the simulation procedures, and the results are given in section 5. Finally, section 6 provides a brief conclusion.

2. Test Steps

A typical block-diagram of a pipeline ADC is shown in figure 1. As described in [4], the main source of DC errors in this architecture is the gain of each analog stage. At full speed, the limitations are due to the frequency bandwidth of each stage. The precision requirement on the gain of the first analog stage is the same as the precision of the whole

ADC, whereas the precision requirement for the gain of the second stage is half the precision of the whole ADC, and so on. For simplicity, we have assumed a pipeline architecture with a 1.5 bit/stage (redundancy necessary for digital error correction) and a gain of 2 at each stage.

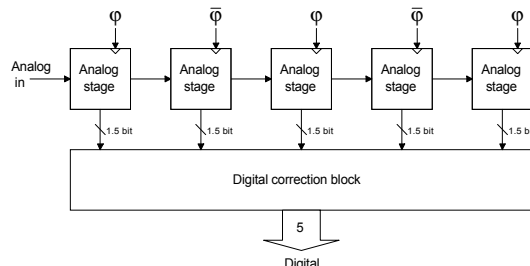


Figure 1: Typical block-diagram of a pipeline ADC.

Our test will be divided into 3 main steps: simple monotonicity test on the overall ADC, test of the DC gain of each analog block and frequency response of each analog block in time-domain. Since a precise analog timer is needed for the frequency response test, a sub-step is to calibrate the analog timer. The DC gain test includes an overall calibration of the analog stages to eliminate small errors due to process variations, temperature variation, etc. and a second test of each stage's gain precision. To verify that the overall ADC is functioning correctly, a simple monotonicity test is performed at the beginning.

3. Detailed Description of each Test Step

3.1 Monotonicity Test

The monotonicity test can reveal most of the possible errors that we may have in a converter. In other words, if there is a catastrophic fault large enough to cause the comparator or an interconnect to malfunction in such a way that one of the characteristics of the converter is not met, it will show on the monotonicity test. The principle is to send a slow ramp to the input of the converter. The ramp has to be slow enough so that the ADC does not skip any output code. The test consists of making sure that the digital output goes from 0 at the beginning of the test to the maximum value when the test is finished. Also, and most importantly, every new value on the digital output must be higher than the preceding. This ensures that no code is skipped.

The most challenging part of this test is the generation of a very low slope ramp. If we use a simple integrator (current source and capacitor), we need either a very low constant current source, or a very large capacitor. For example, if the resolution of the ADC is a 12 bits, its speed 20 Ms/s and its input range 2V, then we need a ramp with a slope lower than 9.7 V/ms. If we want to use a 10pF integrating capacitor, we need a charging current of 0.1μA.

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Generating such a low and precise current on-chip is impractical. The solution we are using is an adaptive scheme on the ramp generation to make it very slow. The advantage of this approach is that we do not need to provide a very low voltage reference (in the millivolt range) to the current source transistor to generate a low current. The adaptive scheme will generate this value automatically to satisfy the Least Mean Square (LMS) condition. The monotonicity of the output can be done with the use of simple digital comparators.

The simplified schematic of the ramp generator used for this test as well as for the analog timers for bandwidth test is shown in figure 2. The principle of operation is the following: A step constructed with the start and stop signals turn on and off the reference current through a capacitor. The resulting output voltage is a ramp directly proportional to the time between the start and stop signals. The two main sources of error in this circuit are the imprecision of the reference current and the value of the capacitor. The result of these errors is shown on figure 3.

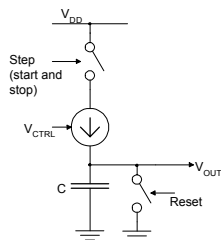


Figure 2: Basic circuit of the analog timer.

Our calibration procedure to solve these two problems is based on discrete adaptive tuning with the help of two reference values: the clock signal and a reference voltage. The clock signal is a very precise timing signal on which we can count. The reference voltage can be any reference voltage already available in the pipeline ADC (like the reference threshold voltages for the flash ADC's).

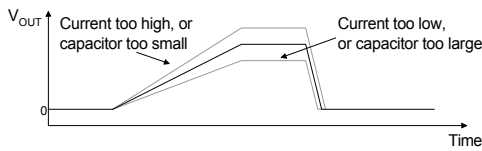


Figure 3: Results of the analog timer.

The block-diagram of the auto-calibrating analog timer and monotonicity ramp generator is shown in figure 4. The principle of operation is the following: A Master Timer is activated for a very precise and known time delay (a certain number of clock cycles) and the output value at the end of the delay is compared with a reference. The number of clock cycles is chosen such that the expected final value is the same as the available reference voltage. Then, the difference between the reference and final voltages is integrated (LMS method) to produce a control signal. This control signal is sent back to the timer to correct the reference current such that the difference between the final analog value and the reference value will be decreased. This control signal is also sent to the Slave Timer, which can be used to process real signals.

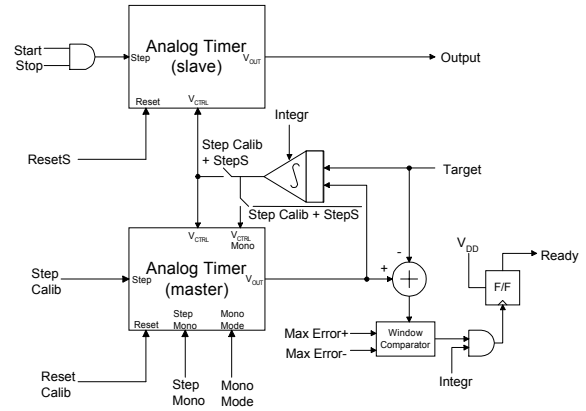


Fig. 4: Block-diagram of the auto-calibrating analog timer and ramp generator.

The only difference from a traditional adaptive scheme is the addition of a control signal on the integrator, “Integr”. Only when this signal is high does the integrator actually integrate. This allows for a discrete process instead of a continuous process like in the traditional adaptive scheme. Figure 5 shows an example of the control signals and timer results. When the error signal is small enough, a “Ready” signal is generated which tells the test controller that the analog timer is now well calibrated and can be used for precise measurements.

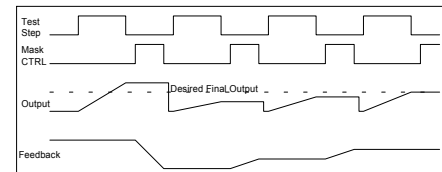


Fig. 5: Example of the control and output signals.

This auto-calibrating ramp generator is used for the bandwidth test and the monotonicity ramp generation. In “Mono Mode”, the master timer uses a larger capacitor and a longer current generation transistor to generate the slow ramp. Also, in “Mono mode”, the slave timer is not used since we just have to generate a constant ramp instead of timing an unknown signal.

3.2 DC Gain and Auto-Calibration

The goal of this test is to verify the precision of the gain of 2 in each analog basic cell. For this purpose, we will use a very precise switched-capacitor voltage doubler [5]. It is based on capacitor swapping to cancel the effect of mismatch between the capacitors. Unfortunately, this precise gain block cannot be used as a gain stage in a pipeline ADC because it needs 4 clock phases to operate and thus would slow down the data conversion excessively. However, it can still be used in our test scheme since we are not running the gain test at full speed. The test is divided in two parts: The continuous calibration of all the gain stages in parallel and the test of each gain stage separately.

The most precise approach to test and calibrate each gain stage would be to use an independent adaptive scheme on each stage and send a “fail” signal when the error signal

cannot be reduced to an acceptable value. However, this approach would cause a high area overhead and would consume a large amount of current (since adaptive scheme has to be working continuously). The other extreme would be to use only one precise gain of 2 and test one stage after the other by switching the signals. This would reduce the area and power overhead, but would be less precise and would not allow continuous calibration to overcome the errors caused by process variations.

Our approach is a tradeoff between these two solutions. The block-diagram is shown on figure 6. The test is divided in two parts. The first part is the calibration of a replica circuit of a gain stage by an adaptive scheme. The control signal is also sent to all the gain stages in parallel to calibrate them according to the replica circuit. This procedure overcomes the errors due to global process variations. This calibration procedure can run in continuous mode while the pipeline is processing data.

The second part is a test of each gain block one after the other by comparing its output signal with the output signal from the precise voltage doubler connected in parallel to the gain stage under test. This test will inform the test controller if any gain stage is still defective after global calibration. This test will only be done once in a while when the test mode is executed.

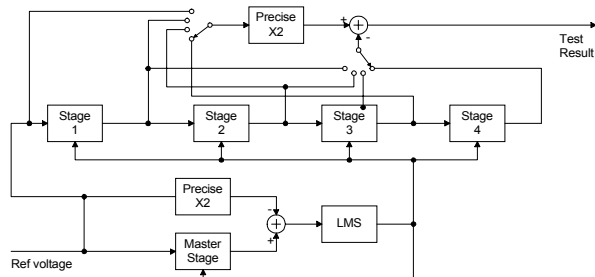


Fig. 6: Block-diagram for gain testing and calibration.

3.3 Bandwidth Test

We use a technique based on time-domain testing of amplifiers to test the frequency response of the gain stages of the pipeline ADC [6]. This technique is based on the measurement of the rise time and delay of the gain block. For simplicity, we limit our test to the measurement of the delay time. The block-diagram of a gain stage configured in test mode is shown on figure 7.

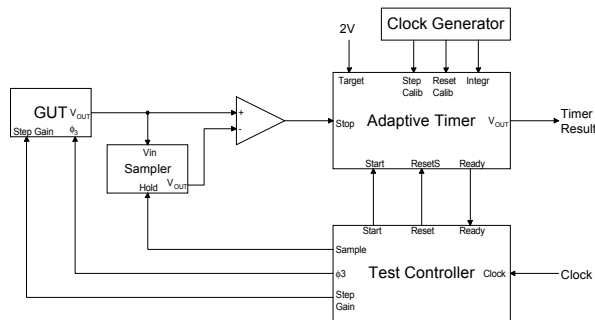


Fig. 7: Block-diagram of the gain stage in test mode.

One of the problems with time-domain testing is the high bandwidth when the gain is only 2. For this reason, we increase the gain of the stage under test to a higher value so that the bandwidth will be equally decreased and thus easier to measure. In figure 7, the gain under test (GUT) has been set to 20. To test the delay, we first let the GUT to rise to steady state and store half of the output into a sample-and-hold (sampler). Then, we set the input of the GUT to 0 and start the timer. The comparator will give a low value at its output as soon as the output of the gain under test has fallen below the 50% value. The timer, which has been started when the process was initiated, stops when the gain stage goes lower than the 50% value. The analog value at the output of the timer is then proportional to the delay time of the gain stage. If we do not consider the error from the imprecision of the analog timer (since it has been previously calibrated), the main source of error is a combination of the DC gain imprecision of the GUT at a gain of 20 and the imprecision of the divider by 2 (which is a simple resistive voltage divider). It can be shown that in the worst case, the final error on the delay measurement will be lower than 1%.

4. Simulation Procedure

Since the goal is to test the entire pipeline ADC, the test circuitry has to be validated with the complete pipeline. Even though the principle of a pipeline ADC is simple, the switched-capacitor implementation of several of its main modules results in long simulations. To simplify the procedure and to shorten the simulation time, we are developing a precise macromodel of the entire pipeline. Then, the simulation procedure consists of replacing the basic block under test with its real transistor-level implementation and simulate the whole pipeline, along with the test circuitry. This procedure is valid under the assumption that we are detecting single faults only, which is the most probable case. The macromodel implements all the main sources of error in a real pipeline ADC (gain error, finite CMRR, offset, clock-feedthrough, etc.). By varying the magnitude of these errors, the user can evaluate the performance of the test circuitry. At the final step of the project, i.e. once the test scheme works correctly, all the stages are replaced by the transistor level version and a final simulation is performed.

5. Results

To this date, three steps in the design process were completed: The behavioral macromodel of the pipeline ADC, the device-level circuit of a pipeline stage and the auto-calibrating analog timer and monotonicity ramp generator. The behavioral macromodel of the pipeline ADC reproduces the functionality of each analog stage in a real pipeline ADC, as well as the digital error correction. It is used as a tool to verify the functionality of the device-level stage and the test procedures. The device-level analog block was designed as simple as possible, since our main goal is the test scheme. It contains a switched-capacitor single-ended gain stage which also implements the DAC and the adder. It also contains a flash ADC made of switched-capacitor comparators. The results obtained once the device-level is included in the behavioral pipeline ADC are

satisfactory. The auto-calibrating analog timer was designed using a cascode current source for improved linearity. The results are shown on figure 8. We can see that within 12 iterations, the final analog value converges to the desired value, which means that the slope is calibrated. Then the Ready signal is generated to inform the test controller that the timer is ready to be used. Figure 9 shows a close-up on the delay measurement of the gain stage. We can see that the timer output rises to 45 mV. This value is directly proportional to the 50% delay time of the gain stage.

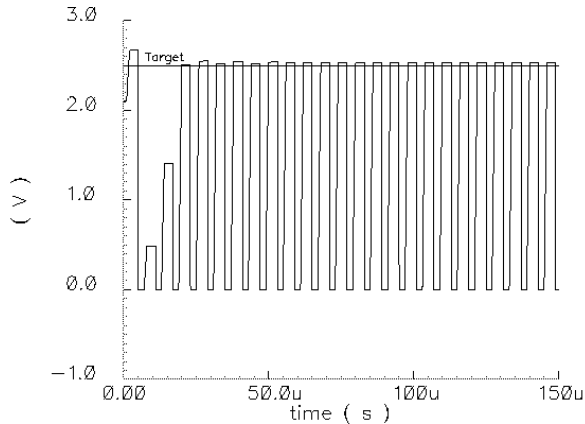


Figure 8: Results from the auto-calibrating analog timer.

The adaptive scheme to produce an low slope for the monotonicity ramp has also been designed and simulated. Figure 10 shows the calibration process. This ramp has a slope of 0.8 V/ms. Using this input ramp for a 12 bits, 20 Ms/s ADC with a 2V input range, we have more than 10 samples per code. This allows to make histogram measurements, which is even more precise than a simple monotonicity test. This result was obtained with a 100pF integrating capacitor in the ramp generator. If a simple monotonicity test is needed (with a ramp that produces no more than one LSB increase per sample), a 10pF capacitor can be used, significantly decreasing the area overhead.

The design of the remaining blocks (DC gain test circuits, digital test controller and complete system integration) is under way. Also, the layouts for the adaptive timer and ramp generator will be sent for fabrication in the near future.

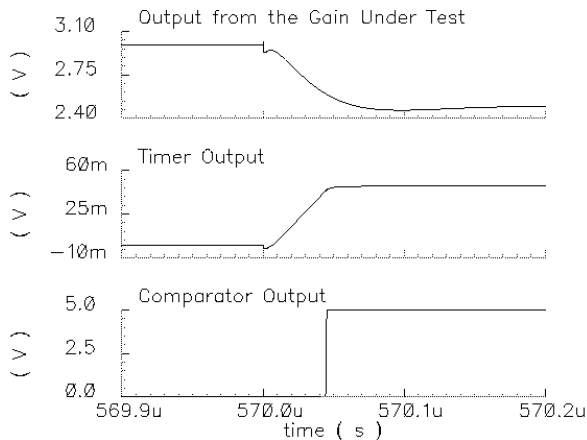


Fig. 9: Delay measurement of the amplifier.

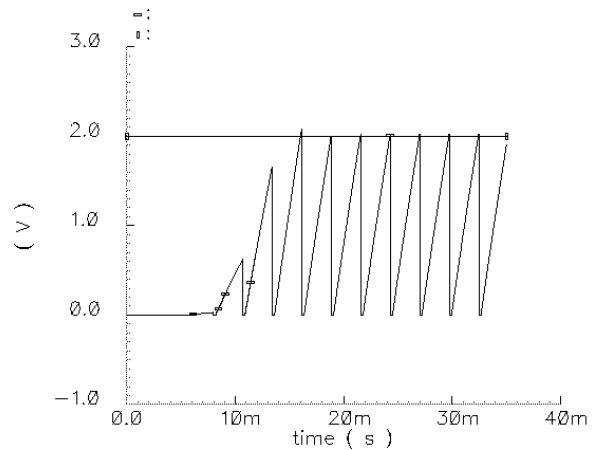


Figure 10: Calibration of the monotonicity ramp generator.

6. Conclusion

In this paper, we have presented a set of new techniques to test pipeline ADC's. The test consists of an overall monotonicity test, a DC gain test of each stage with process variation compensation, and a bandwidth test of each stage. Some of these techniques, like the time-domain testing, can be used in many other basic analog circuits. Compared to the digital timer based on a counter, it presents the important advantage of not needing a high frequency clock to offer a high accuracy. The results for the auto-calibrating analog timer, ramp generator and delay measurement are excellent. The simulation of the whole system with a realistic fault coverage evaluation is presently being designed.

Acknowledgment

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