Proposed final research projects ECEN 607 Spring 2014

These final projects can be done by one student, or a team of two students. The level of work and innovation should be proportional to the number of students. Please provide via e-mail a list of your **three preferred projects** by Thursday April 9th or earlier. The sooner you send me your preferences the better your chances to pick your desired project. *All projects should use 0.18um technology.*

<table>
<thead>
<tr>
<th>Design</th>
<th>[2]</th>
<th>[3]</th>
<th>[5]</th>
<th>[22]</th>
<th>[23]</th>
<th>[24]</th>
<th>[25]</th>
<th>[26]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage [V]</td>
<td>2.7~5.4</td>
<td>2.7~4.8</td>
<td>3.7</td>
<td>5.0</td>
<td>2.7</td>
<td>3.0~5.5</td>
<td>3.0</td>
<td>2.5~5.5</td>
<td>2.7</td>
</tr>
<tr>
<td>PSRR [dB] @ 217Hz</td>
<td>70</td>
<td>72</td>
<td>80</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>96</td>
<td>82</td>
<td>88</td>
</tr>
<tr>
<td>THD+N [%] @ 1kHz</td>
<td>0.03</td>
<td>0.02</td>
<td>0.01</td>
<td>0.08</td>
<td>0.02</td>
<td>0.022</td>
<td>0.0012</td>
<td>0.02</td>
<td>0.018</td>
</tr>
<tr>
<td>Efficiency [%]</td>
<td>75.5</td>
<td>84</td>
<td>92</td>
<td>91</td>
<td>87</td>
<td>77</td>
<td>93</td>
<td>84</td>
<td>85.5</td>
</tr>
<tr>
<td>SNR (A-weighted) [dB]</td>
<td>98.5</td>
<td>96.5</td>
<td>92</td>
<td>85</td>
<td>-</td>
<td>80</td>
<td>103</td>
<td>100</td>
<td>92</td>
</tr>
<tr>
<td>Output power (THD+N[%]) [W]</td>
<td>0.7</td>
<td>1.1</td>
<td>1.0</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>3.1</td>
<td>0.41</td>
<td>1.15</td>
</tr>
<tr>
<td>Load [Ω]</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>-</td>
<td>4</td>
<td>32</td>
<td>4</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Switching frequency [kHz]</td>
<td>410</td>
<td>-</td>
<td>350</td>
<td>500</td>
<td>3000~4000</td>
<td>3200</td>
<td>1000</td>
<td>380</td>
<td>320</td>
</tr>
<tr>
<td>Quiescent current [mA]</td>
<td>4.7</td>
<td>1.9</td>
<td>-</td>
<td>2.0</td>
<td>7.8</td>
<td>2.56</td>
<td>4.0</td>
<td>0.55</td>
<td>3.02</td>
</tr>
<tr>
<td>Topology</td>
<td>PWM</td>
<td>PWM</td>
<td>PWM</td>
<td>SMC</td>
<td>ΔΩ</td>
<td>ΔΩ</td>
<td>PWM</td>
<td>ISMC</td>
<td>PWM</td>
</tr>
<tr>
<td>(Digital input)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMOS process</td>
<td>90-nm CMOS</td>
<td>65-nm CMOS</td>
<td>0.14-μm CMOS</td>
<td>0.5-μm CMOS</td>
<td>0.35-μm CMOS</td>
<td>0.18-μm CMOS</td>
<td>-</td>
<td>0.5-μm CMOS</td>
<td>0.18-μm CMOS</td>
</tr>
<tr>
<td>Die area [mm²]</td>
<td>&lt; 0.44</td>
<td>&lt; 0.44</td>
<td>-</td>
<td>4.7</td>
<td>6</td>
<td>1.6</td>
<td>1.44</td>
<td>1.65</td>
<td>1.01</td>
</tr>
<tr>
<td>Package (Number of pins)</td>
<td>-</td>
<td>-</td>
<td>HVQFN</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>WLCSP</td>
<td>DIP</td>
<td>LQFP</td>
</tr>
<tr>
<td>(Number of pins)</td>
<td>(39)</td>
<td>(24)</td>
<td>(68)</td>
<td>(36)</td>
<td>(9)</td>
<td>(40)</td>
<td>(144)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SMC: Sliding Mode Control scheme  
ISM: Integral sliding Mode Control scheme

**Project 1** Design a class-D amplifier with the same specs as “This work” shown in Table above, but with 45% less quiescent power and at least 33% better PSRR. The topology must be different from the one reported in [6]. Use if possible transistors in moderated inversion and/or bulk biased.

**Project 2** Design an RC- active filter meeting the specs described in [17] but using switched-R techniques [15-16]

**Project 3** Design a low-supply voltage CMOS Bandgap reference as the one shown below as “This Work”, use a different circuit topology PSRR at 10MHz with better than -52dB. The major emphasis is to have a very high PSR bandgap.
Project 4 Design a LDO [14, 18] with the specs of last column of the following table except that you must use 0.18um technology with a load line (settling time) as fast as possible. The structure must be capacitor-less and LDO must be stable for a load capacitance CL varying from 0.1pF to 200pF.

![Table II. Summary of the LDO Performance](image)

Project 5 Design a three- (or higher-) stage amplifier capable of driving 1-to-20nF capacitive load with a GBW>1Mhz and power consumption less than 150uW [7] and an input offset voltage < 4uV. You must use LV techniques such as bulk bias or/and bulk-driven, adaptive bias techniques to handle large load capacitor range.
Project 6 Techniques for improving the light load efficiency of a DC-DC switching converter for portable applications.

Project 7. Design of a capacitor-less LDO with bulk driven feed-forward ripple cancellation [14] technique. Use this technique plus others yielding the PSR at low-frequencies (1 to 100 kHz) with an improvement of at least 30dB for the following load currents (IL): 100µA, 1mA, 10mA, and 50mA.

Parameters Specifications
Unity gain frequency > 1.5 MHz
Phase Margin for IL = 100µA and 50mA > 60 degrees
PSR at low frequencies (1 to 10kHz) > 60 dB
Total quiescent current (including the current in the feedback resistors) < 80 µA

Line and load transient tests must be performed with rise and fall times of 100 ns. For the line transient test, a voltage step from 1.8 V to 2.8 V and vice versa must be applied. For the load transient test, a current step from 100 µA to 50 mA and vice versa must be applied.

Project 8. Design a voltage buffer [20-21] with lowest output impedance and capable to operate a power supply below 1v. Minimize the input referred noise.

Project 9. Design a circuit capable to detect salinity[19]. Explore different approaches and their trade-offs.

Oral Presentations in Power Point Form: April 24, and 26 (outside regular class room), 2014

Progress Report (April 27, 2014) with discussion of the specifications; clearly define the problem, preliminary simulations and identification of the future work and a summary of the reported related publications in the literature. No more than 5 pages. The technology to be used for all projects is 0.18um. This (word document) report must have the following format:

Title

Statement of the problem.

Background, previous work.

Potential applications of your circuit. You must proved specific examples and references.

Basic idea of your solution. Preliminary Results.

Problems (pending) to be solved in the near future.
References, a complete list of references must be included.

*Final Written Report (May 7, 2014).* This final (word Document) must include:

1. Title, authors name
2. An abstract
3. Introduction
4. Background and a comparative tale of previous results
5. Proposed Solution
   - Conceptual idea of solution
   - Circuit Diagram and explanation
   - Design Procedure, how to determine the (W/L)’s and bias
   - Simulate the temperature, noise and process variation effects
   - Simulate the operation of your circuit around the corners of the technology.
6. A comparative Table between Hand calculation and Simulation
7. Discussion of Results with other reported results and suggested improvements
8. Layout of the Circuit if time permits
9. References

**References**


