RESIDUE AMPLIFIER PIPELINE ADC

A direct-conversion ADC designed only with Op-Amps

Abstract

This project explores the design of a type of direct-conversion ADC called a Residue Amplifier Pipeline ADC. Direct-conversion ADCs are a class of ADCs that operate at very high speeds, because the input signal is converted to a digital value in a single iteration. Other types of ADCs require many comparison iterations to convert the signal, resulting in much slower conversion times. This design also takes advantage of residue amplifiers to further improve its performance over other direct-conversion ADCs. This paper will explore the theory and design of this ADC.

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Introduction

Analog to digital converters (ADCs) are any circuits that can be used to convert a continuous time analog signal to a discrete valued digital signal. This conversion is done by quantizing the analog signal into discrete voltage levels in discrete time. These discrete voltage levels can then be converted to a digital representation using a digital logic circuit. The simplest ADC is the voltage comparator. The voltage comparator outputs a logical “high” or digital “1” if the analog signal is greater than a certain threshold, otherwise the comparator outputs a logical “low” or digital “0”. This only gives us one bit of precision, however, other more complex techniques are used to improve precision.

Many types of ADCs exist, but most fall into one of two classes: successive-approximation ADCs (SAR ADCs) & direct-conversion ADCs. SAR ADCs generally operate by performing a 1 bit comparison as described previously using the comparator. This one bit digital value is then converted back to an analog level and the input signal is now compared to this new level. This cycle repeats, generating one more binary bit of precision for every cycle. Unfortunately, because these ADCs require several cycles to achieve a reasonable level of digital precision, the conversion time can be slow. Typical SAR ADCs are limited to sample rates below 5 Msps. Direct-conversion ADCs address this issue by performing the entire conversion process in one cycle. The most common direct-conversion ADC, the flash ADC (shown in **Figure 1**), uses a resistor divider network to divide the voltage into ‘n’ smaller voltages. These smaller voltages are then sampled with an array of comparators, and the comparator outputs are converted to a digital value using digital logic circuitry. This results in a much faster conversion time than SAR ADCs, allowing sampling rates of 1 Gsps and higher.

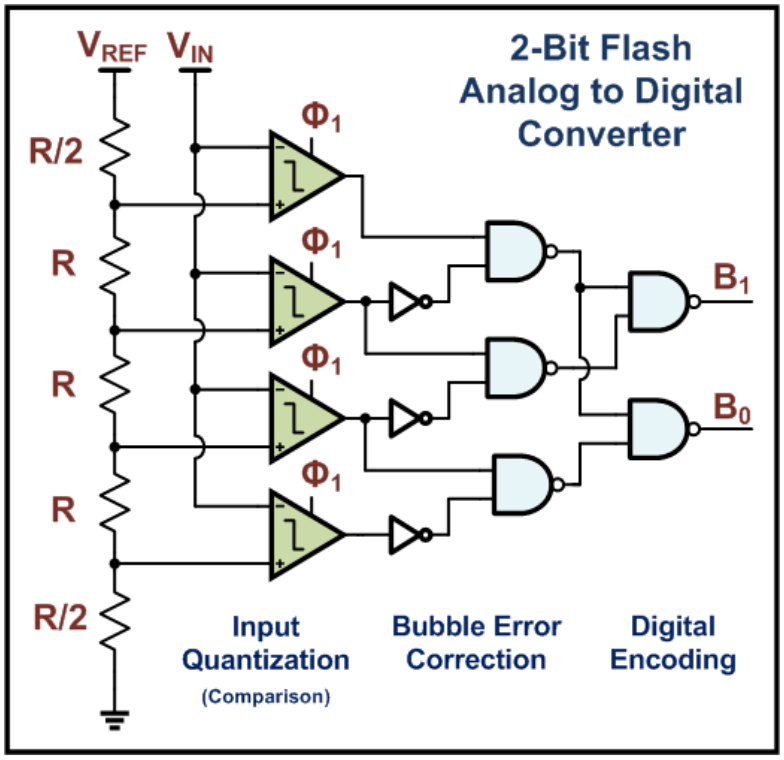

Figure 1: 2-Bit Flash ADC architecture

Finally, residue amplifier pipeline ADCs offer a few advantages over typical flash ADCs. As we can see from the flash ADC architecture shown in **Figure 1**, the number of comparators and logic elements in a flash ADC is on the order of $2^n - 1$, where 'n' is the number of bits, we can see the number of components doubles with each additional bit. This causes two severe limitations. First, the size of this circuit grows exponentially, meaning an ADC with several bits of precision will be very large and expensive to manufacture. In comparison, a residue amplifier pipeline ADC only grows in size on the order of $2 \cdot n$. Second, the number of resistors in the resistor divider network of a flash ADC also grows exponentially with the number of bits of precision. To minimize quantization error in an ADC to a reasonable level, each of these resistors must be matched very closely to each other. This can become impractical as the number of resistors grows. For example, a 12 bit ADC would require 4092 resistors to be matched. The effects of process variations make this impractical. For these two reasons, flash ADCs are often restricted to less than 8 bits of precision. In comparison, the residue amplifier pipeline ADC only requires pairs of resistors to be matched. Matching resistor pairs is practical and shown to be very reliable and precise.

Theory

The residue amplifier pipeline ADC consists of one key block, the residue amplifier. These residue amplifier blocks are then connected in series, forming a pipeline, hence the name. **Figure 2** below shows a block diagram of the residue amplifier. As we can see from the diagram, the amplifier compares the analog input, Vin, to a reference voltage and then generates two outputs. The digital output, D[n], represents the n^{th} data bit of the ADC. R(n) is an analog signal representing the scaled residue or scaled remainder of the signal after comparison. This gives the following equations:

$$D[n] = \begin{cases} 0, & Vin < Vref \\ VDD, & Vin > Vref \end{cases} \qquad R(n) = 2 * V_{in} + D[n]$$

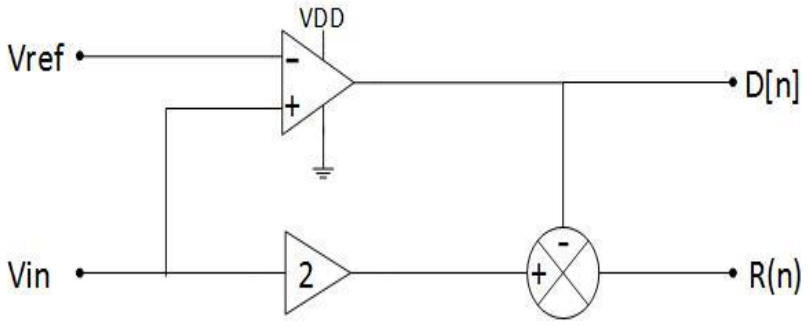

Figure 2: Residue amplifier block diagram

We see that if we set $Vref = \frac{VDD}{2}$, the data bit, D[n], represents the most significant bit of the ADC conversion. The input-output characteristics for VDD = 5V and Vref = 2.5V can be seen below in **Figure 3**. As we can see in this figure, the data bit goes "high" when the input is greater than the reference. More importantly, if we look at the residue signal, we can see that it would generate the next less significant bit of data if we pass it into another comparator. In this way, we can chain together several of these residue amplifier stages to generate a multi-bit ADC conversion. This is illustrated in **Figures 4 & 5**.

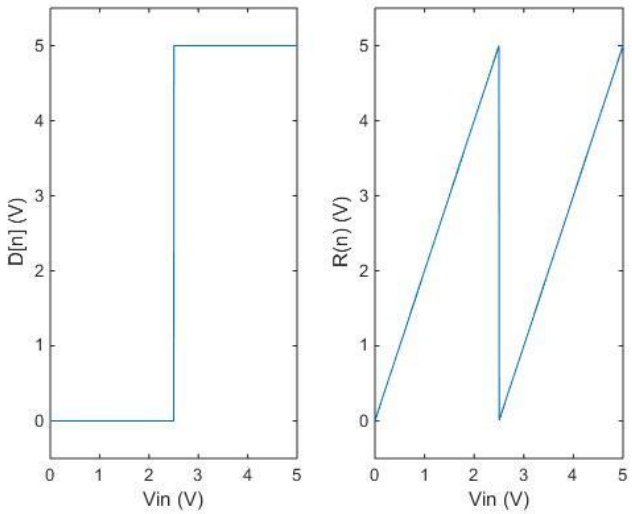

Figure 3: Residue amplifier transfer characteristics

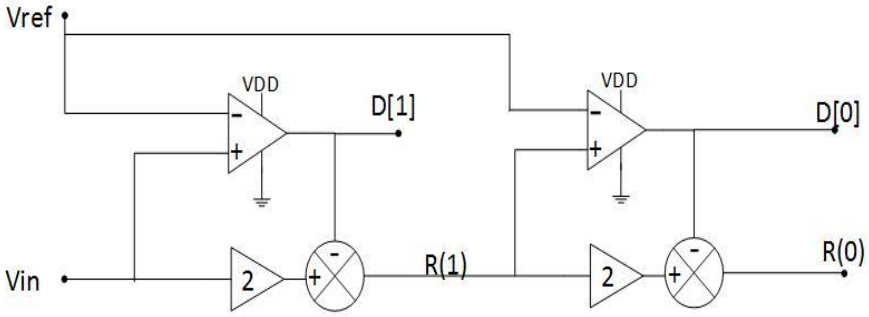

Figure 4: 2 bit residue amplifier pipeline ADC

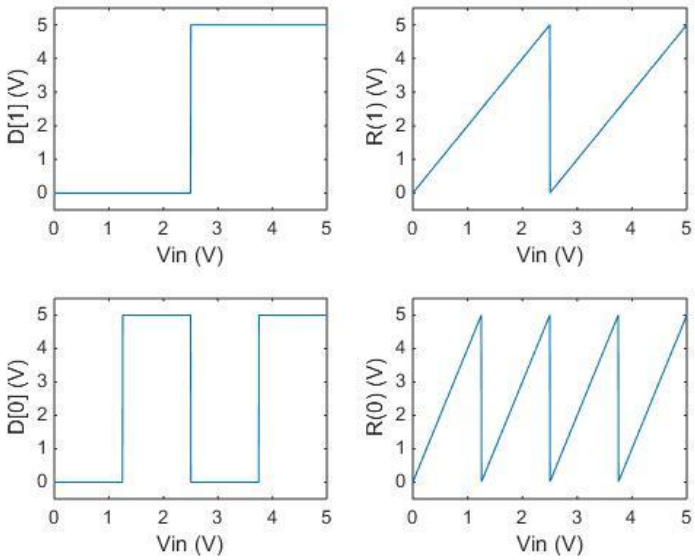

Figure 5: 2 bit residue amplifier pipeline ADC transfer characteristics

Notice in the figure above, that the combination of D[1] and D[0] respectively forms the 2 bit digital representation of Vin. We will use this methodology to design a four bit ADC using only operational amplifiers.

Design

In order to design this ADC, we need to implement the residue amplifier using electronic components. This can be done using a difference amplifier and a comparator as shown below in **Figure 6**. **Figure 7** shows the simulation results of this residue amplifier stage. Notice the simulations results agree with the theoretical results given in **Figure 3**.

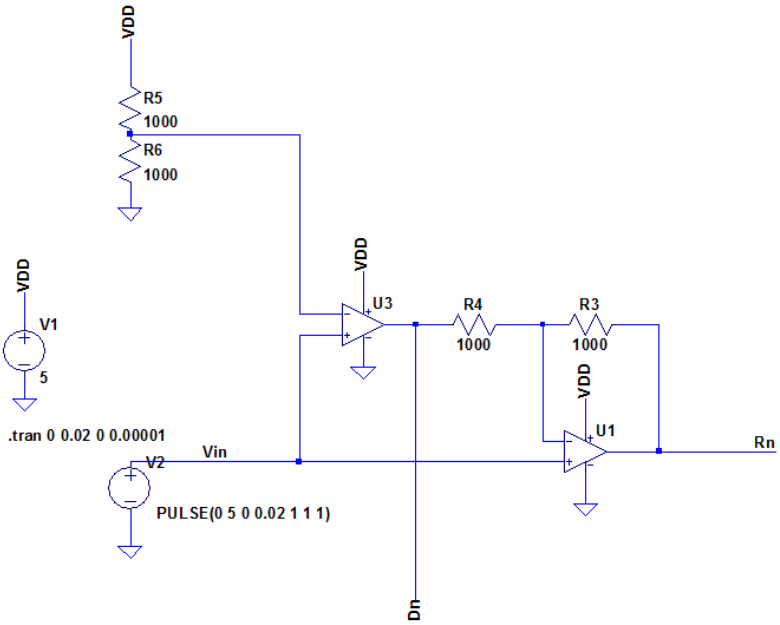

Figure 6: Residue amplifier design using operational amplifiers

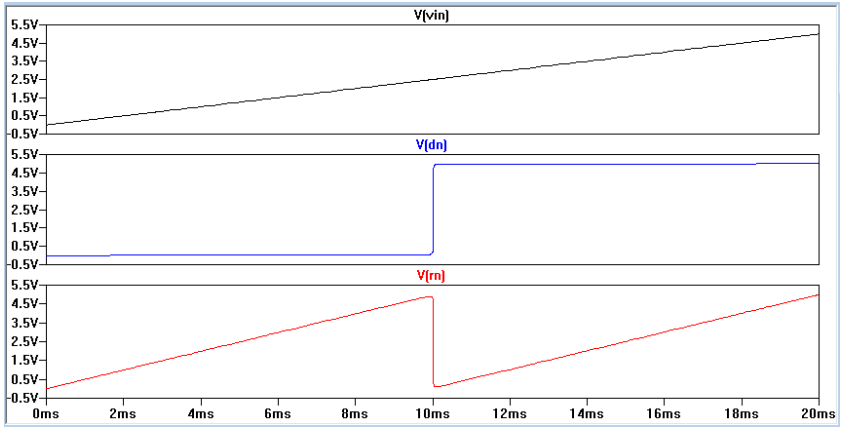

Figure 7: Residue amplifier simulation

This implementation has one major advantage, in that it offers the maximum possible bandwidth from the operational amplifier, since the feedback resistor ratio = 1. With modern operational amplifiers

capable of gain bandwidth products as high as 7 GHz (Texas Instruments LMH3401), we can theoretically realize an ADC with a 3.5 GHz bandwidth using discrete components! This can be shown below with **equation 1**. It is also fair to assume that even better results could be achieved with a fully integrated design.

$$(1)\quad BW = \frac{GBW}{1+\frac{R_{F1}}{R_{F2}}} \quad \rightarrow \quad \frac{7\ GHZ}{1+\frac{R_{F1}}{R_{F2}}} = \frac{7\ GHz}{1+1} = 3.5GHz$$

Using the residue amplifier designed in **Figure 6**, a 4 bit ADC can be designed without much effort, as shown below in **Figure 8**. By examining the simulation results **Figure 9**, we can verify the functionality of the ADC. As we can see, the combination of D[3..0] gives the 4 bit digital representation of Vin at any given time.

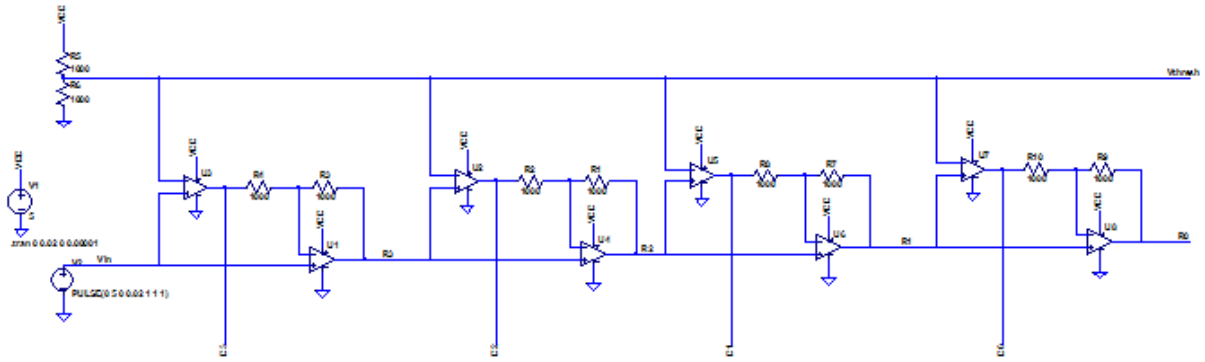

Figure 8: 4 bit residue amplifier ADC schematic

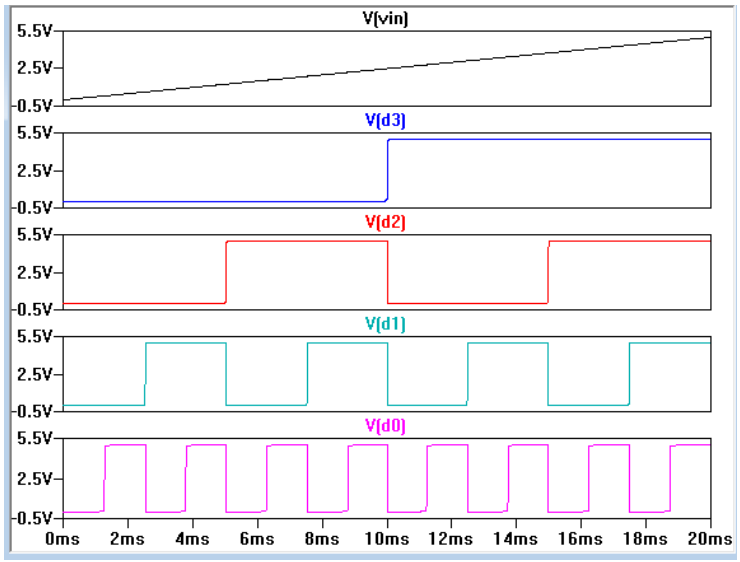

Figure 9: 4 bit residue amplifier pipeline ADC simulation results

Results

The design above meets the expectations of a 4 bit ADC, but also possesses all of the advantages mentioned in the introduction. Notice that the design in **Figure 8** only requires two resistors and two operational amplifiers per stage. This verifies the claim that the size of this ADC grows on the order of $2 \cdot n$. As stated previously, this feature allows for the residue amplifier pipeline ADC to be integrated with a surface area many orders of magnitude smaller than a flash ADC with the same precision. Furthermore, since the size of this ADC grows linearly and only two resistors per stage must be matched, the precision of this ADC is no longer limited by the practical difficulties faced when trying to integrate the exponentially larger flash ADCs. This allows designers to achieve more bits of precision with this design.

Using all of the information described above, a physical version was built (**Figure 10**) using discrete components soldered onto a proto-board. The circuit performs very similarly to the simulations, but with a few exceptions. Most notably, the circuit does not perform well when the Vin voltage level is near GND or VDD. This is understandable, as the uA741 operational amplifiers I am using do not have rail to rail saturation voltages. This error can easily be resolved by using rail to rail output swing operational amplifiers, such as the TLV721.

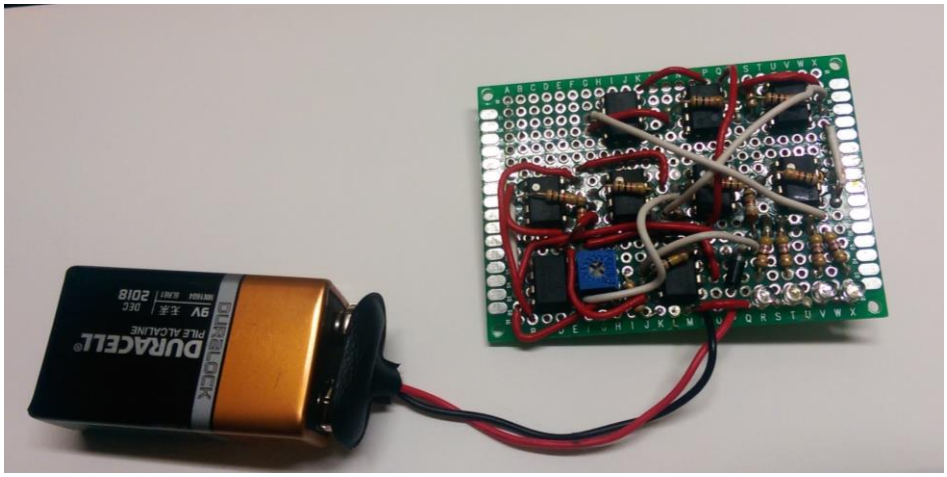

Figure 10: Physical implementation of a 4 bit residue amplifier pipeline ADC, built on proto-board

This circuit also demonstrates another glitch that is more challenging to overcome, called sparkle codes. It is important to note that all direct-conversion ADCs suffer from sparkle codes, so this is not a major factor when comparing this ADC architecture to other direct-conversion ADC architectures. Sparkle codes are a result of the ADC outputting digital values out of order or skipping certain digital values altogether. This is largely due to the mismatch in components, because the circuit built uses 5% tolerance resistors. This mismatch adds an offset error to the already present offset error of the operational amplifiers, causing the comparator in each subsequent stage to switch slightly above or below the correct switching level. Since components can be matched very closely in integrated designs, this problem is not as significant for integrated designs. Sparkle codes may also occur in high-speed circuits as the first pipeline stages may convert a new digital value before the input signal as propagated through the entire pipeline. For this reason it is important to have a good sample and hold circuit to ensure that the input signal propagates through each stage before it is changed.

Conclusion

There are several ADC architectures in use today, but this paper aims to show some of the major advantages of residue amplifier pipeline ADCs. As shown in this paper, they can be capable of very high speeds, they can be fabricated with much lower cost and design complexity than comparable high-speed ADCs and they can also achieve higher precision than comparable high-speed ADCs. Despite its accomplishments, this architecture has some limitations to keep in mind. Due to sparkle codes and the dynamic properties of operational amplifiers, this architecture may never reach the same level of precision as low-speed ADCs, such as the ΣΔ ADC. In many cases, however, the advantages of the residue amplifier pipeline ADC outweigh the disadvantages and make this architecture a very good choice for high-speed ADCs.