Final Project Proposals

Please select your three preferred choices and give them back to me for this Thursday by e-mail or before. These projects can be carried out by one or preferably by a team of two students. Use 0.18μm CMOS technology or other technology if you have access to the PDK.

Project 1. Design a reconfigurable LP 5th-order active filter capable of implementing a Butterworth approximation and an Inverse Chebyshev and also capable of changing power consumption according to the BW of the filter. BW = {1.1, 2.2, 5, 50} MHz and SFDR (dB) > 70 dB. You can choose the filter topology and the filter type, i.e., VCO based integrator, Gm-C, active-R, etc.

Reference:
- Le Ye; Congyin Shi; Huailin Liao; Ru Huang, "A 0.47mW 6th-order 20MHz active filter using highly power-efficient Opamp," in Circuits and Systems (ISCAS), 2011 IEEE International Symposium on , vol., no., pp.1640-1643, May 2011
Project 2. Design the configurable filtering Sigma-Delta ADC that is utilized as the analog baseband in a Wi-Fi 11ac direct conversion receiver (RX). See Fig. 4 from reference. The filtering Sigma-Delta ADC providing both 2nd-order out-of-band filtering and 3rd-order in-band noise shaping is realized with only two op amps. Use also 28nm for your implantation. Except the filter all the other ADC components can be macro modeled

Reference.-


Project 3. Switched-Capacitor Design. Design a multibit pulsewidth modulated (PWM) delta-sigma analog-to-digital converter (ADC) using a single-slope (SS) quantizer. See Fig. 6 of reference

Reference.-


Project 4. Design a discrete-time (DT) analog baseband for software defined-radio (SDR) receivers is presented. A zero-IF baseband signal at the input of a programmable gm is converted to current, which is integrated on a 5th-order DT infinite-impulse response (IIR) low-pass filter with a bandwidth ranging from 150 kHz to 80 MHz. The IIR is followed by a DT amplifier which integrates selected samples to implement active finite impulse-response (FIR) filtering while simultaneously offering variable-gain amplification. See Figs 1 and 4.

Reference.-

Project 5. Design a 4-MHz 4th order active-RC filter using VCO-OTAs. The filter prototype, fabricated in 180nm CMOS technology, shows a power reduction of 41% in the CP and 25% in the PFD, achieved by trading off in-band IIP3 from 21dBm to 19dBm and noise from 0.71mVrms to 0.75mVrms

Reference.

The important dates are:

Progress Report (November 18, 2016) with discussion of the specifications, clearly define the problem, preliminary simulations and identification of the future work and a summary of the reported related publications in the literature. No more than 10 pages. This report is worth 10% of the final project. This (word document) report must have the following form:

Title
Statement of the problem.
Background, previous work.
Potential applications of your circuit provide specific examples and references.
Basic idea of your solution. Preliminary Results.
Problems to be solved in the near future.
References, a complete list of references must be included.

Final Written Report (December 8, 2016). This final (word document) report must include:

1. Title
2. An abstract
3. Introduction
4. Background and a comparative table of previous results
5. Proposed Solution
   - Conceptual idea of solution
   - Circuit Diagram and explanation
   - Design Procedure, how to determine the (W/L)’s
   - The temperature, noise and process variation effects.
6. A Comparative Table between Hand calculation and Simulation
7. Discussion of Results with other reported results and suggested improvements
8. Layout of the Circuit if time allows
9. References

Oral Presentations in Power Point Form: December 2, and 6, 2016.
Some of these projects could be submitted for fabrication before February, 2017