Negative Impedance Converter (NIC) and Applications

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**Negative Impedance Converter (NIC)**

\[
\begin{align*}
V_+ - \frac{V_o}{Z_N} &= I_{in} \\
\frac{V_o}{kR} + \left(\frac{1}{R} + \frac{1}{kR}\right)V_- &= 0 \\
V_o &= (A)(V_+ - V_-)
\end{align*}
\]

Yields

\[
Z_{in} = -Z_N \frac{1+k+A}{k(A-1)-1} = -Z_N \frac{1+\frac{1+k}{A}}{k-\frac{1+k}{A}}
\]

\[
Z_{in} = -\frac{Z_N}{k} \frac{1+s/\omega_Z}{1-s/\omega_p} ; \quad \omega_Z = \frac{GB}{1+k} ; \quad \omega_p = \frac{GB}{1+\frac{1}{k}}
\]
Negative Impedance Implementations

Reference:
Negative Resistance Applications

Gm with negative resistor

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{G_{m1}}{sC - G_{m2} + 1/R_{\text{out}}}.
\]

Fig. 1. (a) Conceptual block diagram of the OTA-C integrator with high dc gain. (b) Small-signal macromodel including parasitic output resistance \(R_{\text{out}}\), in parallel with a negative resistance \(R_N\).

\[ I_1 = I_0 + \frac{I_{\text{out}}}{2} = k_n(V_P - V_{Tn})^2 + k_n(V_Q - V_B - V_{Tn})^2 \]  
(4)

\[ I_2 = I_0 - \frac{I_{\text{out}}}{2} = k_n(V_Q - V_{Tn})^2 + k_n(V_P - V_B - V_{Tn})^2 \]  
(5)

\[ I_{\text{out}} = I_1 - I_2 = 2k_nV_B(V_P - V_Q) = 2k_nV_BV_{id} \]  
(6)

\[ I_{\text{out}} = 2k_n[V_{Boc} + r_{\text{on,B}}(I_{d3} + I_{d4})]V_{id} \]  
(7)

\[ |V_{id}| \leq \sqrt{I_o/k_n - 3V_B^2/4 - V_B/2} \]  
(9)

which requires that the common-mode voltage \(V_{ic} \geq V_{Tn} + V_B + V_{DSSat}\), where \(V_{DSSat}\) is the minimum voltage required for the current source \(2I_o\) to operate in saturation.

Fig. 3. Simplified scheme of the proposed CMOS OTA with a voltage-variable NRL circuit.
Fig. 11. (a) Modified topology of the NRL element in Fig. 3.

\[ I_R = I_a - I_b = 2k_{\text{eff}}(V_C - V_{\text{DD}})V_{\text{out}} \]  (35)

\[ R_N = \frac{V_{\text{out}}}{I_R} = -\frac{1}{2k_{\text{eff}}(V_{\text{DD}} - V_C)}. \]  (39)

To keep this circuit working linearly, the following conditions should be satisfied:

\[ |V_{\text{out}}| \leq \sqrt{\frac{I_o}{k_{\text{eff}}} - \frac{3}{4}(V_{\text{DD}} - V_C)^2} - \frac{V_{\text{DD}} - V_C}{2} \]  (40)

\[ |V_{\text{out}}| \leq V_{TE} \]  (41)

Fig. 12. Alternative topology for an NRL element based on two CMOS double pairs.
Floating bias source: Ma1-Ma3 & Mb1-Mb3

\[ V_B = V_{p0, Ma3} + \sqrt{\frac{I_C^*}{k_{n, Ma3}}} - \sqrt{\frac{I_s - I_C^*}{k_{n, Mb3}}} \]  

(50)

Fig. 14. Complete circuit diagram of the CMOS OTA with the NRL.
The simple negative capacitance generator

\[ Z_{eq} = -\frac{1}{sC} \frac{g_m + s(C_{GS} + 2C)}{g_m - sC_{GS}} \]

Figure 2. Schematic diagrams of (a) negative resistance and (b) negative inductance generators
CAPACITANCE MULTIPLIER

\[ \omega_o = \frac{1}{NRC_F} \]

\[ \frac{V_O}{V_{in}} = \frac{1}{(1+sR(NC_F))(1+1/A)} \]
Fig. 6. Capacitance multiplier. (a) Principle. (b) Circuit implementation.
Figure 3. Linearly bidirectional current-mode capacitor multiplier

Reference:
http://users.ece.gatech.edu/rincon-mora/publicat/trade_jrnls/pmdl_0706_cx.pdf
Using negative capacitance for LDO applications

Fig. 1. Fundamental blocks of the proposed LDO regulator

If $C_{\text{NCC}}$ cancels out the parasitic capacitances $C_p$ and $C_{gd}$ as

$$C_{\text{NCC}} = -\left(C_p + C_{gd}\right),$$

then $v_g$ can be simply approximated as

$$v_g \approx \frac{C_{gs}}{C_{gs} + C_p + C_{gd} - \left(C_p + C_{gd}\right)} v_{dd} = v_{dd}. $$

Fig. 2. Small-signal equivalent circuit of the proposed LDO regulator

Fig. 3. Implementation of NCC with fundamental blocks