ECEN 607
Advanced Analog Circuit Design
Homework 1

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February 11, 2009
**Determination of the Order of the Amplifier**

Typically, when a dc gain of close to 80 dB or more is required from a multistage amplifier with simple, nancascode gain stages, people resort to using either 3 stage or 4 stage amplifiers. Any more than that would make the design very complex since there will be so many variables to so deal with. Even for the four stage amplifier, there is a relative difficulty because of the large number of variables required to optimize the design. Previous results from published works on NGCC amplifiers prove that both 3 and 4 stage amplifiers can attain very high dc gain with enough phase margins and good settling time. The 3 stage is likely to consume less power but at the cost of a very strict design to ensure that all the specifications are met, but makes stabilizing the amplifier easier. The 4 – stage although a little more complex, provides a little more freedom, relaxing a bit the design constraints for each stage while still achieving the desired specs. It is more difficult to stabilize the amplifier in this case.
Determination of Slope Factor “n”

To obtain the slope factor, first we need to determine the normalizing current of the ACM model. The circuit used is showing in the figure below.

![Circuit Diagram]

(a) PMOS                                                                 (b) NMOS

Schematic Setup for the Extraction of Is

The transistors are biased to be in the saturation region. A current with a small delta value is applied to each transistor and the corresponding change in source voltage of the transistors is measured. The normalization current (Is) is then computed as follows.

For NMOS:

\[ I_s \approx I \left( \frac{\Delta I}{I} \right)^2 \]

\[ \Delta I = 4 \mu A \]

\[ I = 40 \mu A \quad \phi_t = 25.9mV \]

\[ \Delta V = 0.5012 - 0.3529 = 0.01408 \]
\[ I_s = 307.37n \]

For PMOS

\[ I = 40\mu A \quad \phi_t = 25.9mV \]
\[ \Delta V = 252m - 230.2m \]
\[ I_s = 142.24\ nA \]

**Plot showing delta Vs used for Extraction of Is**

Next, the Vp parameter has to also be determined. From the ACM model

\[ Vp - Vs = \phi t (\sqrt{1 + id}) - 2 + \ln(\sqrt{1 + id} - 1) \]

It is observed that with id = 3, Vp =Vs. Fig 2.4 is the setup for obtaining Vp and Fig 2.5 is the result from the dc sweep of the setup. A current of 3Is is used.
With this parameter, the value of “n” can now be obtained. By ACM model definition, n is the derivative of Vg with respect to Vp. From the previous simulation, \( V_p = V_s \).

\[
n = \left( \frac{dV_g}{dV_p} \right)
\]

Plot of n and V_D for NMOS and PMOS
From the plot the value of n is extracted at $V_g = 0$ for NMOS and $V_g = V_{dd} = 2$ for PMOS be obtained.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>n</th>
</tr>
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<tbody>
<tr>
<td>PMOS</td>
<td>1.222</td>
</tr>
<tr>
<td>NMOS</td>
<td>1.266</td>
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</table>

**General Design Procedure**

A new variable which depends on the relative location of the poles of the system to each other will be used throughout the design. The general procedure for designing a 4th order system is used here. The 3 stage is obtained by assuming $f_4$ is at infinity. These are the ‘f’ variables. An N-stage NGCC has N ‘f’ variables, as such the following 4 are used henceforth, $f_1$, $f_2$, $f_3$ and $f_4$.

The transfer function for the 4 stage NGCC can be represented by the following equation

$$H(s) = \frac{A_o}{(1 + \frac{A_o}{f_1})(1 + \frac{s}{f_2} + \frac{s^2}{f_2f_3} + \frac{s^3}{f_2f_3f_4})}$$

where $A_o$ is the dc gain and $f_1$, $f_2$, $f_3$ and $f_4$ are the cut off frequencies of each stage.

The stability criteria for this circuit can be fixed by using Routh-Hurwitz stability criterion on the unity-feedback transfer function which is given by the below equation

$$HCL(s) = \frac{1}{s + \frac{s^2}{f_1f_2} + \frac{s^3}{f_1f_2f_3} + \frac{s^4}{f_1f_2f_3f_4}}$$

We obtain the following conditions for stability

$$f_4 > f_2$$

$$f_4 > \frac{f_2}{1 - \frac{f_1}{f_3}}$$

Also phase margin can be approximated by the following equation if $f_3 > f_2$ and $f_4 > f_2$

$$\phi_M = 90 - \arctan(GB/f_2)$$
• The cutoff of the first stage, \( f_1 \) is set equal to the required GBW and \( f_2 \) is obtained from the approximate expression of the phase margin.

\[
f_1 = GBW \cong 30\text{MHz}
\]

\[
\phi_m = 90^\circ - \tan^{-1} \left( \frac{GBW}{f_2} \right) = 70^\circ, \quad GBW = 30\text{MHz},
\]

\[\text{therefore,} \quad f_2 \cong 3GBW = 90 \text{MHz}\]

• \( f_3 \) and \( f_4 \) are determined from the settling time and power requirement of the amplifier. A sweep of \( f_3 \) and \( f_4 \) can be done versus normalized power and settling power and the values of \( f_3 \) and \( f_4 \) that produces the minimum power and settling time and also meet the condition for phase margin >70deg is chosen. Using the full expression for the phase margin of the system, a numerical analysis can be performed to find optimum values of \( f_3 \) and \( f_4 \) such that settling time is minimized while the phase margin is not degraded. This can be performed using MATLAB. The code used is shown in Appendix A.

• To do that we need to choose values for the miller capacitors that we will use in the compensation. We require the ratios between the miller caps and the load cap to determine the normalized power for the MATLAB plots. For this design we use a miller caps of 2.5pF.

The phase margin is computed from the expression below:

\[
\phi_m = 90^\circ - \tan^{-1} \left[ \frac{GBW}{f_2} \left( \frac{1 - GBW^2/f_3f_4}{1 - GBW^2/f_3f_4} \right) \right]
\]

Settling time is obtained using the general transfer function of a 4\(^{th}\) order NGCC, connecting it in unity feedback and taking the step response. The details are shown in the MATLAB code in the appendix. Fig 1.2 shows the results obtained.
From the plots, it is seen that when $f_3 = 2.5f_1$, which is the first plot above, the settling time and power can be optimized. The power and settling time in the other two cases are quite higher compared to the case when $f_3 = 2.5f_1$. At that point the $f_4$ is given by $3.5f_1$ and so we proceed with the design with these parameters.

Next we can determine the transconductance of each stage from the following equation:

$$f_i = \frac{gmi}{2\pi Cmi} \ldots \ldots \ldots 1$$

$f_1 = 30MHz$, $f_2 = 90MHz$, $f_3 = 225MHz$ and $f_4 = 315MHz$

Substituting these values into eqn 1 gives the following gms.
we choose $Cm1 = Cm2 = Cm3 = 2.5\text{pF}$

$gm1 = 471\mu S \quad gm2 = 1.41mS \quad gm3 = 3.5mS \quad gm4 = 4.9mS$

- The ACM model for the transistor is defined by the following equations.

1. $Id = gm \ast n \ast \Phi_t \frac{1 + \sqrt{1 + id}}{2}$

2. $\frac{W}{L} = \frac{gm}{\mu C_{0x} \Phi_t} \left( \frac{1}{\sqrt{1 + id - 1}} \right)$

3. $f_T = \frac{\mu \Phi_t}{2\pi L^2} \left( 2\sqrt{1 + id - 1} \right)$

For this design, we choose an appropriate $V_{dsat}$ for each stage and compute the corresponding inversion level, then we can compute the respective $W/L$ for each transistor.

Using this value and the $gm$, computed above, the aspect ratios of the transistors all the transistors can be obtained from the equation 2 above.

$$\frac{W}{L} = \frac{gm}{\mu C_{0x} \Phi_t} \left( \frac{1}{\sqrt{1 + id - 1}} \right)$$

4th Stage – nmos input

$$(W/L)_4^n = 91$$

Hence,

$$(W/L)_{4p} = (W/L)_{4n} \ast 1/3 = 30$$

3rd Stage – nmos input

$$(W/L)_{3n} = 79$$
Hence,

\[
(W/L)_{3p} = (W/L)_{3n} \times 3 = 237
\]

2\textsuperscript{nd} stage nmos input

\[
(W/L)_{2n} = 23
\]

Hence,

\[
(W/L)_{2p} = (W/L)_{2n} \times 3 = 69
\]

1\textsuperscript{st} Stage – pmos input

\[
(W/L)_{1p} = 124
\]

Hence,

\[
(W/L)_{1n} = (W/L)_{1p} \times 1/3 = 42
\]

These computed values are used for the first set of simulations of the amplifier, and are adjusted as necessary to meet the required specifications.

Schematic for the Four -Stage NGCC
RESULTS

Magnitude and Phase Response, Gain = 76dB

DC Response showing offset, Input referred offset = 4.9mV
Output Swing = 1.61V and CMR = 1.6V

CMRR versus frequency, CMRR @dc = 68dB
PSRR– versus frequency, PSRR @ dc = 44.3dB

PSRR+ versus frequency, PSRR @ dc = 60dB
Transient response showing the settling time, Settling time = 1.155us

Negative Slew Rate, SR+ = 1.94V/us
Positive Slew Rate, $SR^+ = 1.58\text{V/us}$

Current consumption in the design
**Fully Differential Version**

We implement two of the NGCC stages above together with a common mode feedback circuit to obtain the fully differential version of the four stage NGCC.

Schematic of the Fully Differential Block

![Schematic of the Fully Differential Block](image)

Implementation of the Fully Differential Four Stage NGCC Opamp
Results

Magnitude and Phase Response, Gain = 80.9dB GBW = 55MHz PM = 47deg

CMRR versus frequency, CMRR@dc = 117.2dB
PSRR- versus frequency, PSRR-@dc = 89dB

PSRR+ versus frequency, PSRR+@dc = 97dB
Transient Response, Settling time = 1.43u

Negative Slew Rate = -1.3V/us
Positive Slew Rate = 5.12V/us

<table>
<thead>
<tr>
<th>Specification</th>
<th>Required</th>
<th>Single output version</th>
<th>Fully Differential</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>2V</td>
<td>2V</td>
<td>2V</td>
</tr>
<tr>
<td>Load</td>
<td>5pF</td>
<td>5pF</td>
<td>5pF</td>
</tr>
<tr>
<td>GBW</td>
<td>29MHz</td>
<td>29MHz</td>
<td>55MHz</td>
</tr>
<tr>
<td>DC Gain</td>
<td>75dB</td>
<td>76dB</td>
<td>80.9dB</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>70deg</td>
<td>69.6deg</td>
<td>47deg</td>
</tr>
<tr>
<td>Settling time</td>
<td>minimum</td>
<td>1.155us</td>
<td>1.43us</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>minimum</td>
<td>1.38mW</td>
<td>2.59mW</td>
</tr>
<tr>
<td>Slew Rate (+/-)</td>
<td>10V/us</td>
<td>-1.5/1.94 V/us</td>
<td>-1.3/5.12 V/us</td>
</tr>
<tr>
<td>CMRR @DC</td>
<td>-</td>
<td>68dB</td>
<td>117.2dB</td>
</tr>
<tr>
<td>PSRR(+/-)@DC</td>
<td>-</td>
<td>60/44.3 dB</td>
<td>97/89 dB</td>
</tr>
</tbody>
</table>
COMMENTS

From the results shown in the table above, it is observed that with the implementation of the fully differential version of the opamp, we boosted the GBW of the opamp and as well the DC gain shot up by about 6dB which is consistent with theoretical deductions. However, the phase margin is very bad for the fully differential version resulting in a longer settling time. It is also clear from the table how CMRR and PSRR are generally far better for the differential opamp than for the single ended. The fully differential is ideally balanced inherently so rejects all common mode inputs. But the cost of that is about a double pay in power consumption.
PROBLEM 2: DESIGN OF DAMPING FACTOR CONTROLLED FREQUENCY
COMPENSATION AMPLIFIER (DFCFC1)

Topology of DFCFC1 Amplifier

General Design Procedure

The circuit has three gain stages with an extra two feed forward paths. The transconductances of each stage are obtained as follows. DFCFC1 is defined by the following main conditions

1. \( gmf2 = gm3 \)

2. \( Cm1 = \left( \frac{4}{\beta} \right) \cdot \left( \frac{gm1}{gm3} \right) \)

3. \( CL \cdot Cm1 \geq Cm2 > Cp \)

4. \( gm4 = \beta \cdot \left( \frac{Cp}{CL} \right) \cdot gm3 \)

5. \( \beta = \sqrt{1 + 2(CL/Cp) \cdot (gm2/gm2)} \)
• \( GBW = \left( \frac{\beta}{4} \right) \cdot \left( \frac{gm^3}{CL} \right) = \frac{gm^1}{C_1} \approx 29\text{MHz} \) Let \( Cm1 = 5\text{pF} \),

then \( gm^1 = 900\mu\text{S} \) & \( \beta \cdot gm^3 = 0.0036 \) \( \ldots \ldots 1 \)

• \( \beta \) is a constant that depends on the capacitive load and the output parasitic capacitance.

Assuming parasitic capacitance, \( C_p = 100\text{fF} \), then

\[
\beta = \sqrt{1 + 2(CL/C_p) \cdot (gm^2/gm^2)} \quad CL = 5\text{pF}, \quad C_p = 100\text{fF}
\]

Setting \( gm^1 = gm^2 \) and simplifying further gives

\[
\beta^2 = 1 + \frac{0.2}{gm^3} \quad \ldots \ldots \ldots 2
\]

• Equations 1 & 2 are solved simultaneously to give

\( gm^3 = 65\mu\text{S} \) \( \beta = 55 \)

• \( gm^4 \) is also obtained from the following expression

\[
gm^4 = k \cdot \left( \frac{C_p}{CL} \right) \cdot gm^3, \quad gm^3 = 65\mu\text{S} \quad C_p = 100\text{fF} \quad CL = 5\text{pF}
\]

therefore \( gm^4 = 71.5\mu\text{S} \)

For this design, we choose an appropriate Vdsat for each stage and compute the corresponding inversion level, then we can compute the respective W/L for each transistor.
For the various stages and the gms associated with them, we can obtain the W/L for each transistor.

### For the 3\textsuperscript{rd} Stage – nmos input

\[(W/L)_{3n} = 38\]

Hence,

\[(W/L)_{3p} = (W/L)_{3n} \times 3 = 114\]

### 2\textsuperscript{nd} stage nmos input

\[(W/L)_{2n} = 30\]

Hence,

\[(W/L)_{2p} = (W/L)_{2n} \times 3 = 90\]

### 1\textsuperscript{st} Stage – pmos input

\[(W/L)_{1p} = 109\]

Hence,

\[(W/L)_{1n} = (W/L)_{1p} \times \frac{1}{3} = 36\]

The design was done based on these aspect ratios obtained but a little fine tuning was done to meet the required specifications.
Schematic of the DFCFC Opamp

Stability Response

Magnitude and Phase Response, Gain = 101.3dB
DC Response: Output swing = 1.65V, ICMR = 1.61V

DC Response, Input referred offset = 1.94mV
CMRR versus frequency, CMRR@ dc = 60dB

PSRR- versus frequency, PSRR- @ dc = 80dB
PSRR+ versus frequency, PSRR+ @ dc = 83dB

Transient Response, Settling time = 619ns
Negative Slew Rate = -4.9V/us

Positive Slew Rate = -3.3V/us
<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
<th>SIMULATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Avo</td>
<td>75 dB</td>
<td>101.3 dB</td>
</tr>
<tr>
<td>GBW</td>
<td>29 MHz</td>
<td>29 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>70 deg</td>
<td>69 deg</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>10 V/µs</td>
<td>-4.9 V/µs (-ve)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3 V/µs (+ve)</td>
</tr>
<tr>
<td>Settling Time</td>
<td>Minimum</td>
<td>619ns</td>
</tr>
<tr>
<td>CL</td>
<td>5 pF</td>
<td>5 pF</td>
</tr>
<tr>
<td>PSRR+</td>
<td></td>
<td>83 dB</td>
</tr>
<tr>
<td>PSRR-</td>
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<td>80 dB</td>
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<tr>
<td>CMRR (0)</td>
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<td>Power Consumption</td>
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<td>Total Compensation Capacitance</td>
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<td>8 pF</td>
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</table>
## COMPARISON OF RESULTS – 3 STAGE DFCFC1 & 4 STAGE NGCC

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<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
<th>DFCFC1</th>
<th>NGCC</th>
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<td>Avo</td>
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<tr>
<td>GBW</td>
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<tr>
<td>Phase Margin</td>
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<tr>
<td>Slew Rate</td>
<td>10 V/µs</td>
<td>-4.9 V/µs (-ve)</td>
<td>1.94 V/µs (+ve)</td>
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<td></td>
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<td>3.3 V/µs (+ve)</td>
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<tr>
<td>Settling Time</td>
<td>Minimum</td>
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<td>1.155µs</td>
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<tr>
<td>CL</td>
<td>5 pF</td>
<td>5 pF</td>
<td>5 pF</td>
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<tr>
<td>PSRR+</td>
<td>-</td>
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<td>60 dB</td>
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<tr>
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<tr>
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<tr>
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<tr>
<td>Output Swing</td>
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<tr>
<td>Input referred offset</td>
<td>-</td>
<td>4.9mV</td>
<td>1.94mV</td>
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</tbody>
</table>

**COMMENTS**

It can be observed from the table the differences between the two schemes of compensation. With the three stage DFCFC we were able to achieve a gain of 101 dB and about the same GBW and phase margin as the four NGCC which has a gain of 76 dB. The two have comparable DC response but the input referred ioffset of the NGCC is better than that of the DFCFC. The DFCFC on the other hand uses much less compensation caps than the NGCC and much less power (about 40% less in this case) as well. But the main issue with this scheme is the relatively bad rejection to common mode signals.
PROBLEM 3

Design of a three Stage NGCC based on the Settling Time Optimization techniques.

The closed loop transfer function of a three stage NGCC operational amplifier is given by:

\[
H(s) = H_o \frac{1 + \frac{g_{mf}}{g_m} \frac{C_{c2}}{g_{m2}} s + \frac{g_{mf}}{g_m} \frac{C_{c1} C_{c2}}{g_{m3} g_{m2}} s^2}{1 + \left(\frac{C_{c1}}{f g_m} + \frac{g_{mf}}{g_m} \frac{C_{c2}}{g_{m3}}\right) s + \frac{g_{m2} + g_{mf}}{f g_m} \frac{C_{c1} C_{c2}}{g_{m3} g_{m2}} s^2 + \frac{C_{c1} C_{c2} C_L}{f g_m g_{m3} g_{m2}} s^3}
\]

As per the compensation network design rules:

\[
C_{c1} = \frac{g_{m1}}{g_m} \frac{1}{f} \left(1 + \frac{2}{\rho}\right) (1 + 2\rho\zeta^2) C_L
\]

and \(C_{c2} = \frac{g_{m2}}{g_m} \zeta^2 \frac{(\rho + 2)^2}{1 + 2\rho\zeta^2} C_L\)

where \(\rho = \frac{p_1}{(\zeta \omega_n)}\)

Where \(\rho \) and \(\zeta \) are parameters that will be optimized to optimize settling time.

For the optimization of the settling time for a third order system,
\[ G_{III}(s) = \frac{G_o \left( 1 + \frac{s}{z_1} \right) \left( 1 + \frac{s}{z_2} \right)}{\left( 1 + \frac{s}{\rho} \right) \left( 1 + 2 \frac{\zeta}{\omega_n} s + \frac{s^2}{\omega_n^2} \right)} \]

To deal with the minimization problem systematically, it is instead convenient to consider the following normalized system.

\[ G_{III}(s) = \frac{G_o \left( 1 + \frac{s}{X_1} \right) \left( 1 + \frac{s}{X_2} \right)}{\left( 1 + \frac{s}{\rho} \right) \left( 1 + 2\zeta^2 s + \zeta^2 s^2 \right)} \]

where \( \rho = \frac{p_1}{(\zeta \omega_n)} \) and \( X_1 = \frac{z_1}{(\zeta \omega_n)} \) and \( X_2 = \frac{z_2}{(\zeta \omega_n)} \)

represent the relative real pole and zero locations with respect to the real part of the complex poles \( \zeta \omega_n \), which is the normalizing factor.

From the above, it can be shown that the minimization problem to find the minimum settling time for the third order system can be reduced to finding optimal values for \( \zeta \) and \( \rho \).

The absolute denormalized minimum settling time (MST) can be derived from the following:

\[ t_{SMIN} = \frac{T_{S_{III\text{min}}}}{\zeta_{III\text{opt}} \omega_n} \]

To obtain the parameters; \( \rho_{opt} \) and \( \zeta_{III\text{opt}} \) and hence \( t_{SMIN} \) we need to do some sweep to obtain these values based on the level of accuracy we want.

Based on these values we can obtain the required miller caps need to compensate the circuit to achieve minimum settling time as shown in the equations Cc1 and Cc2 above.. This was done and the results are shown below.

The miller caps obtained are used on the design of the three stage NGCC and the result shows a better settling time than the previous one designed.
Schematic of the three stage NGCC

RESULTS

DC Response: Output swing = 1.58V, ICMR = 1.57V
Dc Response: Input referred offset = 5.1mV

Magnitude and Phase Response, Gain = 72dB, GBW = 27.5M Hz, PM = 74deg
CMRR versus frequency; CMRR@dc = 57dB

Transient showing settling time; Settling time = 140ns
### Comments

With the design using the settling time minimization techniques, it is very obvious the difference between the two settling times. While all other specs are comparable, the main difference between the two is that the settling time of the conventional is about 10 times that of the new technique and it consumes less power than the conventional. This certainly makes this a good choice in the design of such amplifiers.
PROBLEM 4: DESIGN USING THE 65nm CMOS TECHNOLOGY

General Design Procedure

A new variable which depends on the relative location of the poles of the system to each other will be used throughout the design. The general procedure for designing a 4th order system is used here. The 3 stage is obtained by assuming f4 is at infinity. These are the ‘f’ variables. An N-stage NGCC has N ‘f’ variables, as such the following 4 are used henceforth, f1, f2, f3 and f4.

The transfer function for the 4 stage NGCC can be represented by the following equation

\[ H(s) = \frac{A_o}{(1 + \frac{A_o}{f_1})(1 + \frac{s}{f_2} + \frac{s^2}{f_2f_3} + \frac{s^3}{f_2f_3f_4})} \]

where \( A_o \) is the dc gain and \( f_1, f_2, f_3 \) and \( f_4 \) are the cut off frequencies of each stage

The stability criteria for this circuit can be fixed by using Routh-Hurwitz stability criterion on the unity-feedback transfer function which is given by the below equation

\[ H_{CL}(s) = \frac{1}{s + \frac{s^2}{f_1f_2} + \frac{s^3}{f_1f_2f_3} + \frac{s^4}{f_1f_2f_3f_4}} \]

We obtain the following conditions for stability

\[ f_4 > f_2 \]
\[ f_4 > \frac{f_2}{1 - \frac{f_1}{f_3}} \]

Also phase margin can be approximated by the following equation if \( f_3 > f_2 \) and \( f_4 > f_2 \)

\[ \Phi_M = 90 - \arctan(GB/f_2) \]

- The cutoff of the first stage, \( f_1 \) is set equal to the required GBW and \( f_2 \) is obtained from the approximate expression of the phase margin.

\[ f_1 = GBW \cong 70MHz \]
\[ \phi_m = 90^\circ - \tan^{-1} \left( \frac{GBW}{f_2} \right) = 70^\circ, \quad GBW = 30\text{MHz}, \]

therefore, \[ f_2 \approx 3GBW = 210\text{ MHz} \]

- \( f_3 \) and \( f_4 \) are determined from the settling time and power requirement of the amplifier. A sweep of \( f_3 \) and \( f_4 \) can be done versus normalized power and settling power and the values of \( f_3 \) and \( f_4 \) that produces the minimum power and settling time and also meet the condition for phase margin >70deg is chosen. Using the full expression for the phase margin of the system, a numerical analysis can be performed to find optimum values of \( f_3 \) and \( f_4 \) such that settling time is minimized while the phase margin is not degraded. This can be performed using MATLAB. The code used is shown in Appendix A.
- To do that we need to choose values for the miller capacitors that we will use in the compensation. We require the ratios between the miller caps and the load cap to determine the normalized power for the MATLAB plots. For this design we use a miller caps of 2.5pF.
- The phase margin is computed from the expression below

\[ \phi_m = 90^\circ - \tan^{-1} \left[ \frac{GBW}{f_2} \left( \frac{1 - GBW^2/f_3 f_4}{1 - GBW^2/f_3 f_4} \right) \right] \]

Settling time is obtained using the general transfer function of a 4th order NGCC, connecting it in unity feedback and taking the step response.
Matlab Plot of variation of settling time and power versus f3 and f4

From the plots, we again choose $f_3 = 2.5f_2$ and $f_4 = 3.5f_2$ since this choice optimizes both settling time and power.

Next we can determine the transconductance of each stage from the following equation:

$$ f_i = \frac{g_{m_i}}{2\pi C_{m_i}} \quad \text{......} \quad 1 $$

$f_1 = 70\,\text{MHz}$, $f_2 = 210\,\text{MHz}$, $f_3 = 525\,\text{MHz}$ and $f_4 = 735\,\text{MHz}$

Substituting these values into eqn 1 gives the following $g_{m}$s. and again assuming $C_{m1} = C_{m2} = C_{m3} = 1\,\text{p}$
\[ gm_1 = 439\mu S \quad gm_2 = 1.319\mu S \quad gm_3 = 3.3mS \quad and \quad gm_4 = 4.6mS \]

- The ACM model for the transistor is defined by the following equations.

1. \[ I_d = gm * n * \phi_t \frac{1 + \sqrt{1 + id}}{2} \]
2. \[ \frac{W}{L} = \frac{gm}{\mu C_{ox} \phi_t} \left( \frac{1}{\sqrt{1 + id - 1}} \right) \]
3. \[ f_T = \frac{\mu \phi_t}{2\pi L^2} (2\sqrt{1 + id - 1}) \]

For this design, we choose an appropriate Vdsat for each stage and compute the corresponding inversion level, then we can compute the respective W/L for each transistor.

\[ \frac{W}{L} = \frac{gm}{\mu C_{ox} \phi_t} \left( \frac{1}{\sqrt{1 + id - 1}} \right) \]

The values for \( \mu C_{ox} \) for nmos and pmos for the 65nm technology is extracted from Cadence and the results found to be:

\( K_n = 540\mu \) & \( K_p = 120\mu \)

This is used in computing the aspect ratios for the various transistors in a similar manner as was done in Problem 1

4\(^{th}\) Stage – nmos input

\[ (\frac{W}{L})_{4n} = 43 \]

Hence,

\[ (\frac{W}{L})_{4p} = (\frac{W}{L})_{4n} * 3 = 129 \]

3\(^{rd}\) Stage – nmos input
\[(W/L)_{3n} = 35\]

Hence,

\[(W/L)_{3p} = (W/L)_{3n} \times 3 = 105\]

2\textsuperscript{nd} stage nmos input

\[(W/L)_{2n} = 12\]

Hence,

\[(W/L)_{2p} = (W/L)_{2n} \times 3 = 36\]

1\textsuperscript{st} Stage – pmos input

\[(W/L)_{1p} = 102\]

Hence,

\[(W/L)_{1n} = (W/L)_{1p} \times 1/3 = 34\]

These computed values are used for the first set of simulations of the amplifier, and are adjusted as necessary to meet the required specifications.
The schematic of the opamp is shown below

DC Response, Output Swing = 908mV and ICMR = 872mV
DC Response, Input referred offset = 3.12mV

Magnitude ad Phase Response, Gain = 66dB GBW = 70.6MHz PM = 70 deg.
CMRR versus frequency, CMRR@dc = 53dB

PSRR- versus frequency, PSRR- @dc = 46dB
PSRR+ versus frequency, PSRR+ @dc = 54dB

Transient Response showing settling behavior, settling time = 185ns
Transient Response, Negative Slew Rate = -7V/us

Transient Response, Negative Slew Rate = 5.2 V/us
Comparing Open Loop Response for a sinusoidal signal, with different DC levels.

For DC = -0.3V, 0 and 0.3 respectively from top to sown on the plot.

Current consumption
### SUMMARY OF RESULTS

<table>
<thead>
<tr>
<th>Specification</th>
<th>Required</th>
<th>Single output version</th>
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</thead>
<tbody>
<tr>
<td>Power Supply</td>
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<td>1V</td>
</tr>
<tr>
<td>Load</td>
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<td>5pF</td>
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<tr>
<td>GBW</td>
<td>70 MHz</td>
<td>70.6 MHz</td>
</tr>
<tr>
<td>DC Gain</td>
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<td>66 dB</td>
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<tr>
<td>Phase Margin</td>
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<td>70 deg</td>
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<tr>
<td>Settling time</td>
<td>minimum</td>
<td>185 ns</td>
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<tr>
<td>Power Consumption</td>
<td>minimum</td>
<td>1.2 mW</td>
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<tr>
<td>Slew Rate (+/-)</td>
<td>10 V/µs</td>
<td>5.2/-7 V/µs</td>
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<tr>
<td>CMRR @DC</td>
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<td>53 dB</td>
</tr>
<tr>
<td>PSRR(+/-)@DC</td>
<td>-</td>
<td>54/46 dB</td>
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<tr>
<td>CMR</td>
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<tr>
<td>Output Swing</td>
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<td>908 mV</td>
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<tr>
<td>Input referred offset</td>
<td>-</td>
<td>3.12 mV</td>
</tr>
</tbody>
</table>

### COMMENTS

We observe from the results here that almost all the specifications for the design were met except for the slew rate specification. This is due to the very small amount of current used in the tail. To increase the SR, more current should be pumped and that is also expensive. We realize that with this small sized technologies, it is much easier to achieve very frequencies than with the long channel technologies. But it comes at the cost of extra power.
REFERENCES

1. Edgar Sanchez-Sinencio, ECEN 607 Lecture 2: Nested Gm-C Amplifiers


