Advantages and Disadvantages of Active Inductors on Chip over Monolithic Inductors

Kevin Bellows
ECEN 457, Prof. Edgar Sánchez-Sinencio
Department of Electrical and Computer Engineering
Texas A&M University
College Station, TX, USA

***Abstract*—The potential benefits and pitfalls of using active inductors instead of monolithic spiral inductors for on-chip filtering are investigated. In particular, the metrics of power consumption, required area, inductor quality factor, and frequency of operation are taken into consideration.**

***Index terms*—Active inductor, monolithic inductor, peaking, filter.**

I. INTRODUCTION

Inductors serve multiple purposes in electronic circuits, namely in filters designed for a particular frequency response and in amplifiers as a means to provide peaking to enhance the bandwidth. Despite the utility of inductors, they are rarely fabricated on chip. The reasons for this are many: they take consume large amounts of area, manifest poor quality factors (typically in the range of five to eight [1]), have many parasitics associated with them, and have the propensity to become coupled with other on-chip inductors. The two main solutions that work around these issues are the use of off-chip inductors and the use of on-chip active inductors. In this paper, the results of using on-chip active inductors versus using on-chip monolithic inductors will be examined.

II. TERMS OF COMPARISON

The comparison conducted in this report between monolithic inductors and on-chip active inductors is not a perfectly fair comparison for three reasons. First, the measurements to characterize the operation of an active inductor were taken with discrete, i.e. off-chip, components. Owing to the time constraints of this project, this is a reasonable adjustment to have made. Second, the operation of monolithic inductors has been simulated rather than measured on a fabricated integrated circuit. Third, the discrete active devices used to measure the active inductor have unity-gain frequencies of approximately 1 *MHz*, which limits the active inductors' characterizations to this frequency. With an on-chip active inductor, however, the active devices can be designed specifically to meet the performance metrics required by the overall circuit. These terms of comparison must be kept in mind throughout the analysis conducted in this paper.

III. QUALITATIVE CHARACTERIZATION OF MONOLITHIC INDUCTOR

The aforementioned parasitics inherent to a spiral inductor on chip can be attributed to several electrical phenomena, whose effects diminish the performance of the inductor. To truly understand these effects, it is important to know their underlying causes.

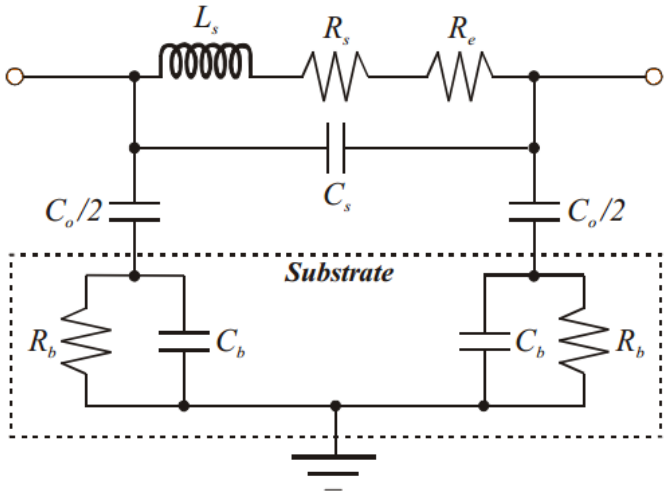

Figure 1: Circuit-level characterization of the monolithic inductor [1-2].

In the model shown in fig. 1, R_s is the winding resistance associated with the metal used to forge the inductor [1]. The electromagnetic field in the metal winding couples to the substrate and thus induces so-called eddy currents, whose losses are represented by the eddy resistance R_e [1]. The substrate resistance, R_b, describes high-frequency loss in the substrate due to capacitive coupling between the metal winding and the bulk [1].

The capacitance C_o is simply the capacitance established between the metal conductive layer and the substrate, with an oxide dieletric [1]. C_s is the distributed shunting capacitance manifested between the metal turns of the inductor and the crossunder wire [1]. Finally, C_b is the capacitance found within the bulk [1]. Despite all these parasitics, though, the monolithic inductor remains a linear element.

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IV. CHARACTERIZATION OF ACTIVE INDUCTOR

A. Algebraic Analysis of Active Inductor

The active inductor topology being used in this investigation is shown below in fig. 2.

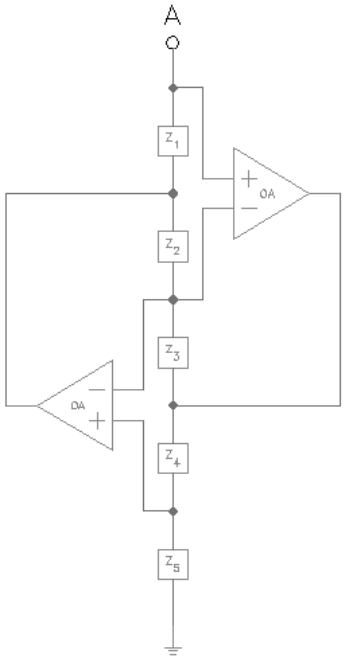


Figure 2: Generalized impedance converter used to emulate an inductor, comprised of two operational amplifiers and five impedances [3].

Under the assumption of ideal op-amps, nodal analysis yields the equation for the impedance seen at node *A* to be

$$Z_{in} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}. \quad (1)$$

Thus, choosing impedances Z_1, Z_3, Z_4, and Z_5 to be resistances and impedance Z_2 to be a capacitor will yield an inductive input impedance of value

$$L_{eff} = \frac{R_1 R_3 R_5 C_2}{R_4}. \quad (2)$$

However, it is important to note that this topology requires one terminal of the network to be grounded [3]. Thus, ladder *RLC* networks are not viable options for filtering using this active inductor configuration, except for in the case of a highpass filter.

Now, assuming the operational amplifiers have finite, frequency-dependent open-loop gain but are otherwise ideal, the relationship given by (1) becomes much more convoluted:

$$Z_{in} = \frac{\left[\begin{array}{l} A^2 Z_1 Z_3 Z_5 + A(Z_1 Z_3 Z_4 - Z_1 Z_2 Z_4 - Z_1 Z_2 Z_5 \\ +Z_1 Z_3 Z_5) - Z_1 Z_3 Z_4 - Z_1 Z_2 Z_5 - Z_1 Z_3 Z_5 \end{array}\right]}{\left[\begin{array}{l} A^2 Z_2 Z_4 + A(-Z_2 Z_4 - Z_2 Z_5 + Z_3 Z_4 \\ +Z_3 Z_5) + Z_2 Z_4 + Z_2 Z_5 + Z_3 Z_4 + Z_3 Z_5 \end{array}\right]}, \quad (3)$$

where $A \approx \frac{GB}{s}$ is the approximate frequency-dependent open-loop transfer function of the two (identical) op-amps, and *GB* is their gain-bandwidth product. The impedance seen looking into node *A* is now a complicated biquadratic function of frequency and, frankly, quite messy to analyze. Accounting for input node capacitances, finite input resistances, and finite output impedances of the op-amps makes it clear that this active inductor has a number of parasitics on par with that of the monolithic inductor, as shown in fig. 1. Additionally, the amplifiers used to forge the inductive impedance are nonlinear devices, which will have some effect on the linearity of the circuit as a whole.

B. Simulation of Active Inductor

To verify proper operation of the active inductor in practice as opposed to simply relying on equations, it is necessary to characterize its impedance across frequency. Since conventional laboratory equipment does not allow for a frequency-swept measurement of impedance, simulations were instead carried out using LTspice IV. The plots in fig. A-1 show the frequencies for which the active inductor behaves as desired.

Z_1	10.1 Ω
Z_2	49 *pF*
Z_3	10.1 Ω
Z_4	46.2 *k*Ω
Z_5	10.3 Ω
op-amps	LM 741
Z_{in}	1.1144 *pH*

Table 1: Parameters for the active inductor's impedance simulation, whose results are shown in fig. A-1.

Fig. A-1(a.) shows reactance that increases approximately linearly with frequency until about 300 *kHz* (a value dependent on the active inductor topology chosen, the amplifiers used, and the component values utilized), at which point, the relationship seems to rise with the square of frequency. This square-law relationship, combined with the peak around 950 *kHz* and subsequent drop-off, suggest that this active inductor should not be used above 300 *kHz* (or, with a bit more lenience, 500 *kHz*). Fig. A-1(b.) shows the low resistance associated with the active inductor, whose value approaches zero at two distinct points. It is likely that at the two frequencies in question, the inductance being created is resonating with parasitic capacitances of the op-amps.

The quality factor shown in fig. A-2 was computed by dividing the reactance in fig. A-1(a.) by the resistance in fig. A-1(b.). The quality factor seems to be linearly dependent on frequency up to 300 *kHz*, at which point its value is approximately 1.45, which is extremely poor. Even at 500 *kHz*, where the quality factor begins a rapid nonlinear increase, the value is only about 4.75. Of course, as the gain-bandwidth product of the amplifiers used increases, so does the frequency at which the active inductor operates, which allows the maximum quality factor to also increase. However,

in addition to the active inductor's parasitic resistance in fig. A-1(b.), the DC power used to operate the op-amps further adds to the losses sustained by the active inductor. Monolithic inductors, on the other hand, consume power only due to their parasitic resistances—there is no additional power overhead.

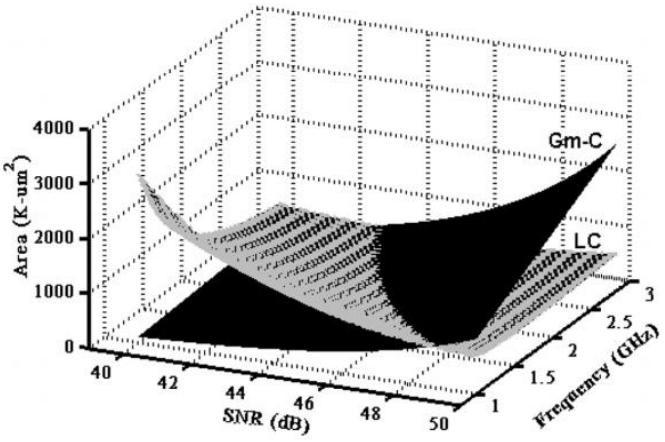


Figure 3: Area required for an on-chip inductor-capacitor network versus a transconductor-capacitor topology [4].

The area required for physical inductors and active inductors varies with regards to the frequency of operation and desirable SNR. Fig. 3 shows the necessary area, though the active inductor architecture used to generate the displayed data is not the same architecture being investigated in this paper. However, it remains clear that as frequency and SNR increase, the size of a monolithic inductor decreases, while that of a transconductor-capacitor interconnection increases. These variations are essential to consider when deciding whether to use a monolithic or active inductor for a particular circuit or application.

V. *RLC* FILTER USING AN ACTIVE INDUCTOR

A. *Design*

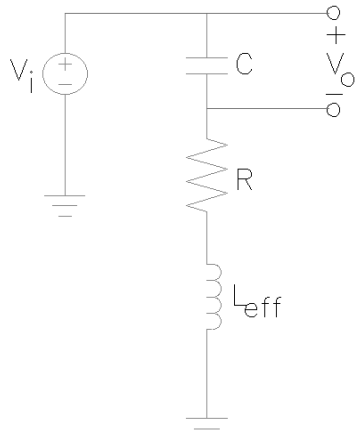


Figure 4: Lowpass *RLC* filter with the output taken across the capacitor [5].

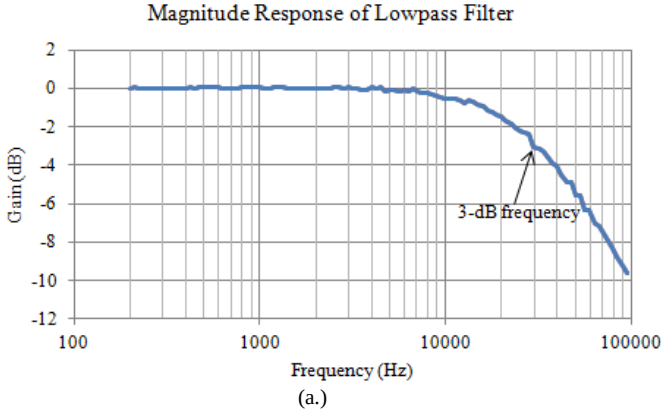
The circuit in fig. 4 has its input applied across a series combination of a capacitor, a resistor, and an (active) inductor. The output, taken across the capacitor, gives rise to a gain of

$$\frac{V_o}{V_i} = \frac{1}{s^2 L_{eff} C + sRC + 1}, \qquad (4)$$

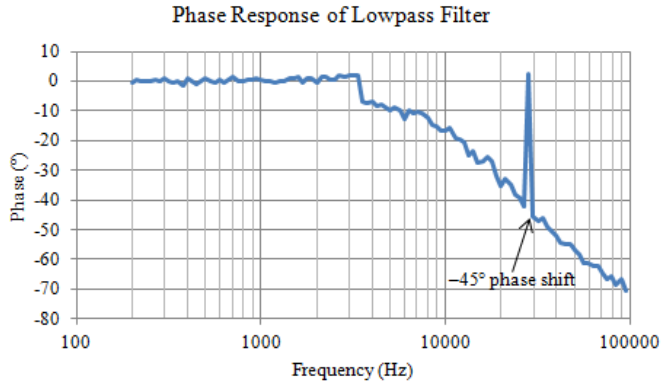
indicating this is a lowpass filter. Keeping the values from table 1, the active inductor has a value of 1.1144 *pH*. Using a series capacitor of 472 *pF* and a resistor of 7.47 *k*Ω should result in a 3-*dB* bandwidth of approximately 45 *kHz* (**NOTE**: in the lab demo, this value was quoted as being a 30 *kHz* theoretical bandwidth, but it now seems that was an incorrect statement).

B. *Laboratory Measurements*

The following data were taken for the circuit shown in fig. 6 with dual supply voltages of ±10 *V* applied to the op-amps. 40 data points were taken per decade, and the stimulus voltage had a peak amplitude of 1 *V*.



(a.)



(b.)

Figure 5: Measured frequency response of the lowpass filter. The measured 3-*dB* frequency is approximately 30 *kHz*. (a.) Magnitude response. (b.) Phase response.

The measured bandwidth of 30 *kHz* does not match the theoretical value of 45 *kHz*. Despite this error in bandwidth (which is either due to mismeasurement of component values or incorrect wiring of the circuit), though, the measured frequency response does have the expected shape (with the exception of the jump in phase around 30 *kHz*).

VI. CONCLUSION

In order to decide between using a monolithic inductor or an active inductor, several key differences must be taken into consideration. Active inductors will not pose the problem (or

have the potential advantage) of being coupled with each other, yet they consume much more power than their monolithic counterparts. It has been explained that both have many parasitics associated with them, though a technology-specific analysis of these effects, including the resulting quality factor, would provide essential clarifying information. The frequency range of operation, as well as the required noise and linearity performance, will determine the necessary area for each type of inductor. Finally, an active inductor may require a more involved and slower design process than a monolithic inductor, though the latter may require some complicated electromagnetic field analysis before the design can be considered finalized. All in all, neither choice is clearly superior to the other, and it is ultimately up to the designer to choose which is more suitable for a given circuit.

ACKNOWLEDGMENT

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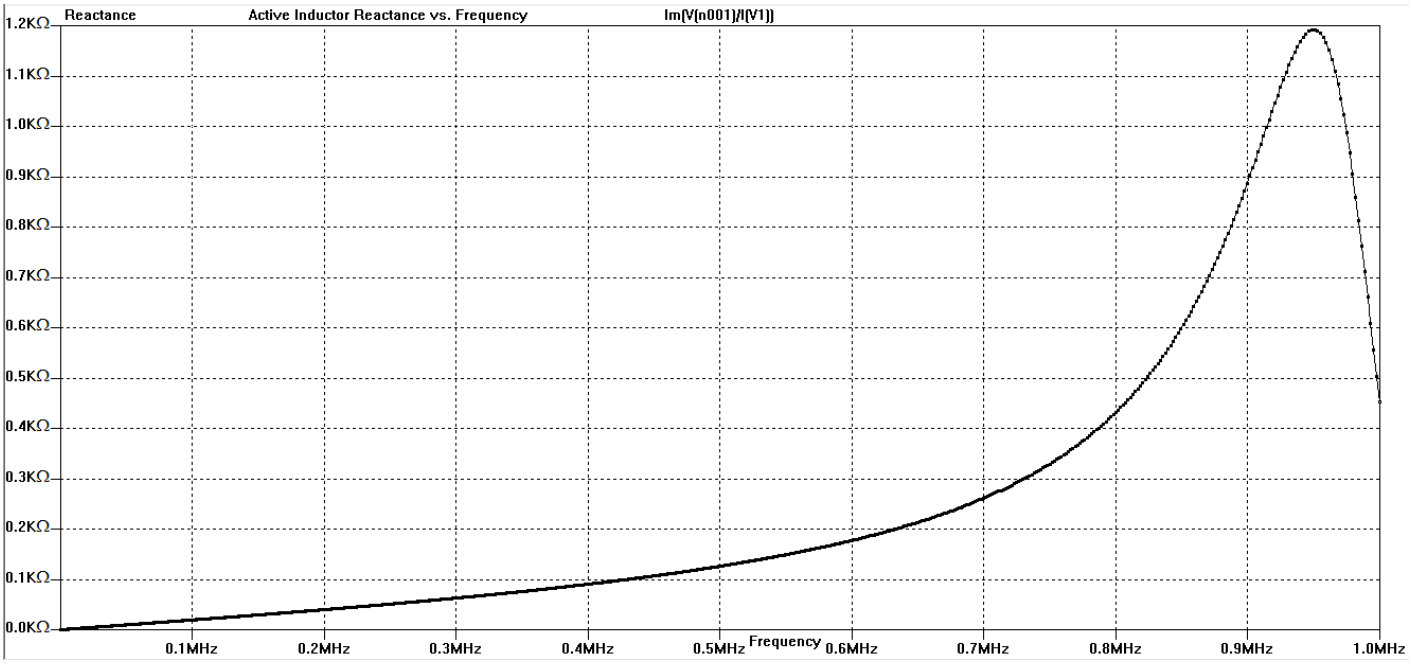
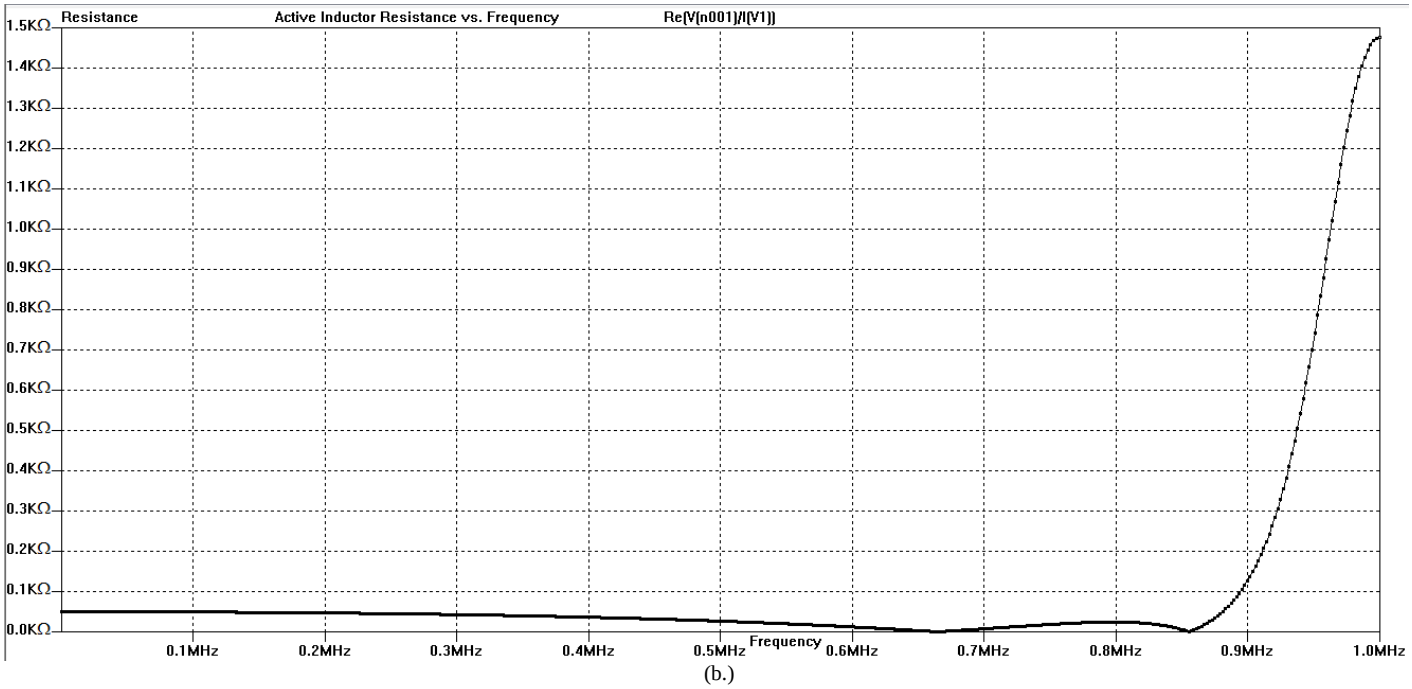
VII. APPENDIX



(a.)



(b.)

Figure A-1: Simulated (a.) reactance and (b.) resistance of an active inductor with the component values shown in table 1.

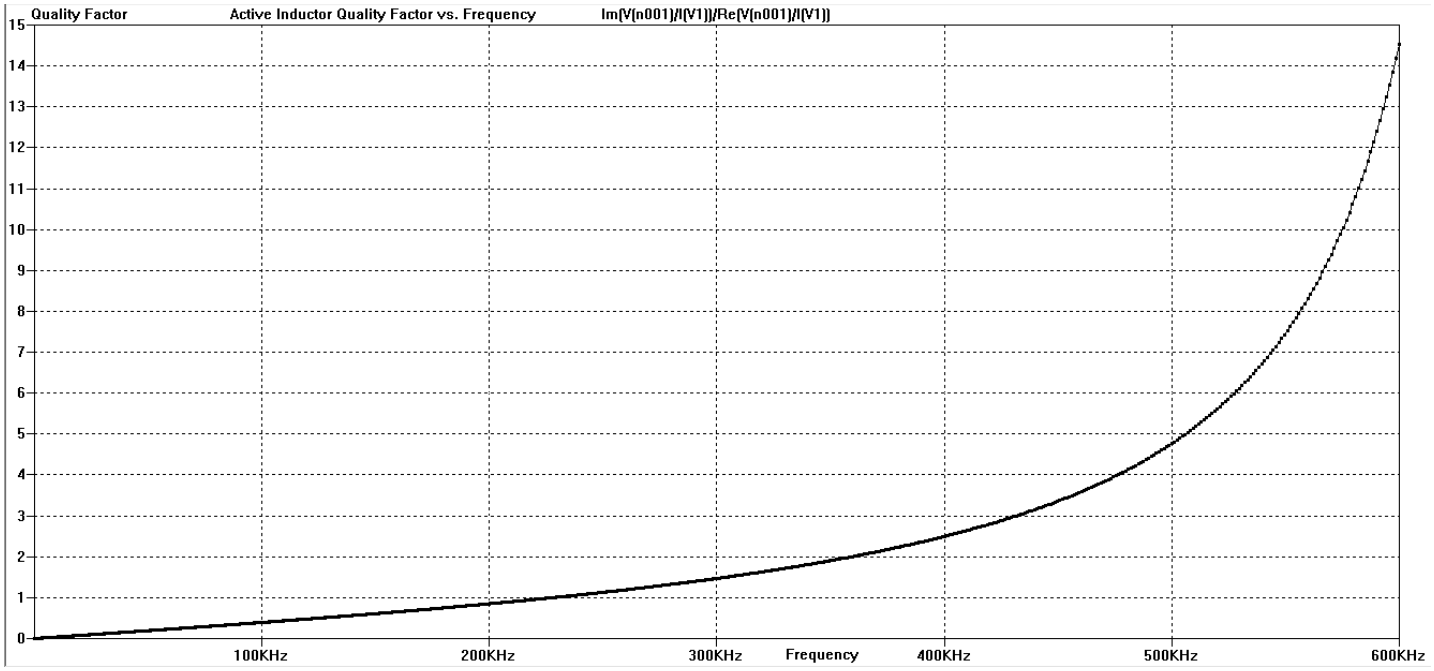


Figure A-2: Simulated quality factor of the active inductor described in table 1 against frequency. The upper frequency limit is 600 *kHz* in order to facilitate a readable scale.